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# PERFORMANCE ANALYSIS OF 60 GHZ LOW NOISE AMPLIFIERS USING MULTI-GATE MOSFETs

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**ABSTRACT**

Short-channel devices are preferred for realizing millimetre circuits, but these are affected by the short-channel effects (SCE). Multi-Gate (MG) MOSFET is found to be an alternative to overcome this drawback. In this paper, study and analysis of DC and AC parameters of MG MOSFETs have been attempted and small signal gain ($y_{21}$) of multi-gate structure is analytically derived. Design of low noise amplifier (LNA) at 60 GHz using the channel charging resistance model has been done.Small signal gain and noise figure using the channel charging resistance model has been derived and analysed. The proposed LNA circuit uses various multi-gate MOSFET structures and the results are compared with conventional MOSFET based design. The designed LNA using a Quadruple Gate structure exhibited the noise figure improvement of 24.4% and 42.79% when operated at 1 V and 1.5 V respectively. Also the corresponding gain increases by 2.38 times and 4.9 times compared with conventional single gate MOSFET design.

**Keywords**: *60 Ghz, Low Noise Amplifier, Multi-Gate (MG) MOSFET, Small Signal Gain, Channel Charging Resistance Model*

## 1. INTRODUCTION

Advancements in millimeter wave (mm wave) technology combined with low cost silicon devices make transmission of gigabit multimedia content faster and easier. Several applications are explored in this regime, specifically around 60 GHz, where the signal transmission is greatly attenuated due to oxygen absorption [1]. This drawback is exploited by establishing communications for short range wireless point-to-point links. Typical applications include multi-gigabit wireless local area network (WLAN), personal area network (PAN) systems, Gigabit Ethernet communication system, SONET, iHDMI (Wireless HD), vehicular radars etc., [2]. Compared to other frequency bands, 60 GHz communications have advantages like frequency efficiency, inherent interference reduction, frequency reuse and abundant unlicensed bandwidth. These allow us to extend its application from scientific and industrial use to commercial gadgets, like mm identification (MMIDs) systems.

However, 60 GHz communication system, despite of its huge potentials, faces a series of technical challenges that needs to be resolved before its deployment. These challenges include the design of high gain and high speed RF transceivers, channel propagation issues, antenna technology, and choice of modulation. Among these, RF transceiver design, particularly LNA design is crucial, since it involves integration of active and passive elements to work at 60 GHz. Moreover, it has to overcome the path loss and noise present in the environment and in the device itself. LNA primarily decides the overall noise figure (*F*) of the receiver. Ensuring enough gain in LNA stage helps to suppress the noise affecting the succeeding stages.

To satisfy the demand of mm wave applications, LNA should possess the following characteristics i.e., high gain, input-output impedance matching, low noise figure, low power dissipation and linearity. Using conventional CMOS device for the design of mm wave LNA is an exorbitant task since it suffers from substrate loss, high gate resistance, high channel charging resistance and moderate transconductance. Moreover, scaling problems like short channel effects (SCEs) and inaccurate compact models at mm wave frequency add to its demerits. These make CMOS a dubious choice in the design of mm wave LNA. Alternatively few mm wave LNA design uses III – V semiconductors like GaN/GaAs devices [3], compound semiconductors like SiGe devices [4] and FINFETs

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[5]. These are not considered as better alternatives due to their high integration cost, power consumption and IC handling issues. Hence the exploration of CMOS started to continue, expecting transit frequency ($f_T$) of CMOS to reach around 280 GHz in 45 nm technology [6]. Other advantages like low fabrication cost, low power consumption and compact structured design strongly recommend CMOS a better choice for RF/MMIC design.

In this scenario, more work is focused on gain enhancement techniques for CMOS based LNA design. For example, on-chip inductors are designed to resonate with parasitic drain capacitors to improve gain, but larger die area is required to realise it. Alternatively, inductor free models like resistive type feedback is attractive for gain boosting stage [7]. But more number of stages is required to achieve high gain and hence area and power consumption increase because of resistive loss. Additionally, current-steering techniques like gate-inductive gain-peaking technique and current reuse technique suffer from severe parasitic effects, leading to noise figure degradation at mm wave frequencies [8]-[9]. These problems necessitate the use of highly compact CMOS structure with reduced SCEs and channel charging resistance, higher transit frequency ($f_T$) and higher transconductance, which leads to the evolution of MG MOSFETs. Thus MG MOSFETs which possesses all the above features are identified as future generation devices with promising low power characteristics. This forms the scope of the paper.

First of all, studying the DC and AC characteristics of MG MOSFETs are needed to identify the following: threshold voltage, range of input bias to be given, drain current, channel charging resistance, to determine the voltage gain, to calculate the source and load impedance for matching and to determine noise figure. These parameters are necessary for designing RF circuits like LNAs using the MG MOSFET device.

The organisation of this paper is as follows: Section II deals with the the extraction of DC and AC parameters of MG MOSFET using core model. Section III involves analytical derivation of small signal gain ($y_{21}$) of MG MOSFET. Design of LNA using various MG MOSFETs along with channel charging resistance is dealt in section IV. Section V presents the results and discussion and finally the conclusion is presented in section VI.

## 2. MG MOSFET

Due to continuous scaling of CMOS, SCEs become prominent which deteriorates the performance of the device, particularly lowering the device transconductance. Measure of SCE is given in Eq. (1) as per [10].

$$S = 0.64\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{bi} \quad (1)$$

$L_{el}$ is the electrical (effective) channel length,
$V_{bi}$ is the source or drain built-in potential,
$t_{ox}$ is the gate oxide thickness,
$x_j$ is the source and drain junction depth and
$t_{dep}$ is the depletion region thickness of active regions with respect to substrate.

To reduce SCEs either decrease the oxide thickness or increase the substrate doping which in turn reduces $t_{dep}$. The former is preferable but causes carrier tunneling towards the gate while the later decreases the depletion layer thickness which increases the active-bulk capacitance and affects the carrier mobility also. So the use of multi-gate (MG) structure surrounding the channel [10]–[11] is identified as the preferred solution, particularly for RF/mm applications. To achieve better electrostatic control over channel and to reduce SCEs, various gate structures like double gate (DG), triple gate (TG), quadruple gate (QG) and surrounding gate (SG) MOSFETs shown in figure.1 are designed. DG MOSFET has top and bottom gates between the channel, TG MOSFET has gate on three sides of the channel region while SG MOSFET has gate wrapped around the channel region as a cylindrical wall; whereas the QG MOSFET has gate around the channel region, which is assumed to be a square section.

The extraction of DC and AC parameters of MG MOSFETs are as follows. Parameters of interest are current drive, threshold voltage roll-off, sub-threshold slope and transconductance.

High current drive is an attractive factor which depends on the strength of gate voltage on the channel. More the number of gates, more the electric field lines that are getting aligned on the channel, which makes channel inversion to takes place in quick time, even if considerable SCEs are present. Figure 2 shows the dependence of drain current ($I_D$) as a function of channel length for various MG MOSFET.

It is observed that for any selected channel length, as the number of gate increases, the control on the channel by gate voltage increases and hence its drain current. QG MOSFET has $I_D$, that is, 571 μA at channel length of 10 nm which is the largest compared to other types. It is also noted that TG

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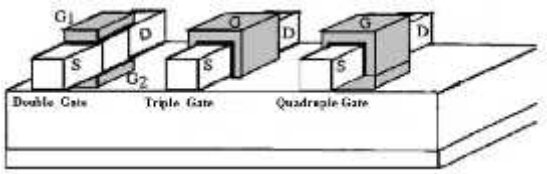


*Figure1: Various Gate Structures of MG MOSFET*

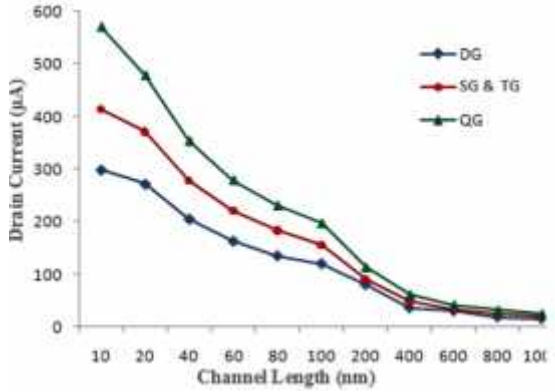


*Figure 2: Variation of Drain Current for Different Channel Lengths for Various MG MOSFETs*

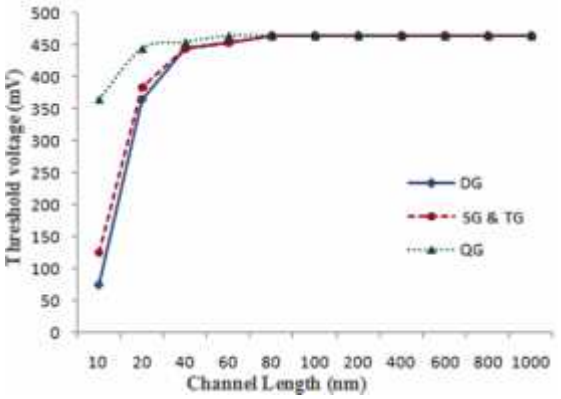


*Figure 3: Threshold Voltage Roll-off in MG MOSFET*

and SG show similar characteristics because of similarity in the geometry of SG and TG[12].

Threshold voltage ($V_t$) is the gate voltage that determines the 'ON' state of the device. To extract $V_t$, second derivative method [13] is performed on $I_D$ - $V_{gs}$ curves. Based on this, the extracted threshold voltages for various MG MOSFETs are plotted in figure 3. Due to SCEs, $V_t$ drops down from its nominal value if channel length decreases. In figure 3 it is noted that if the channel length is 80 nm and below that, then $V_t$ roll-off begins. It is noted that roll-off is less for QG than the other types. That is, QG MOSFET has 21.5% $\Delta V_t$ whereas DG MOSFET has higher roll-off of 83.87% for the channel length variation of 1000 nm to 10 nm.

Next DC parameter chosen is sub-threshold slope (S). The drain current that flows when $V_{gs}<V_t$, is the sub-threshold current and it significantly

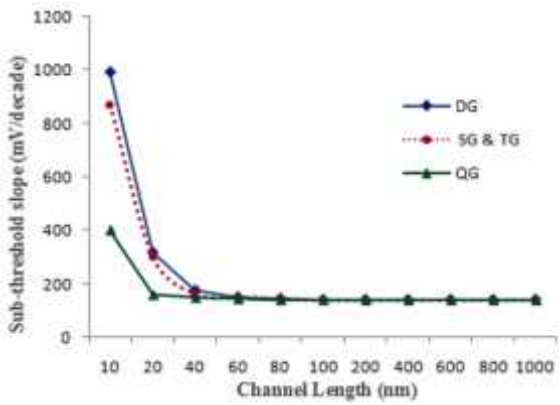


*Figure 4: Variation of Sub-Threshold Slope*

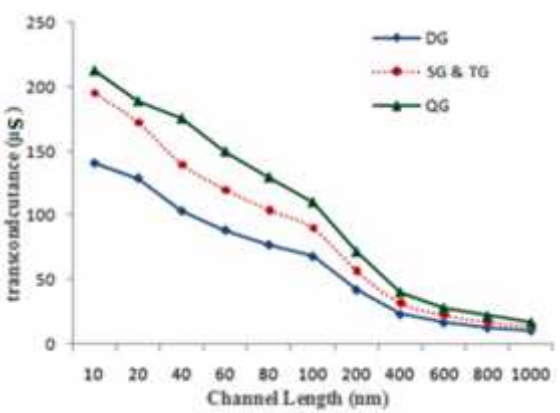


*Figure 5: Variation of $g_m$ for MG MOSFETs*

contribute to power dissipation in VLSI circuits in OFF state. Sub-threshold slope ($S$) is the measure for sub-threshold current and in other way, it indicates the change in $V_{gs}$ needed for a decade change in $I_D$. So lower the value of $S$, faster the transistor in switching from off-state to on-state and is given by,

$$S = \left(\frac{d(\log I_D)}{d V_{gs}}\right)^{-1} \quad (2)$$

The ideal value of S should be zero but for MOSFET it is limited to 60mV/decade. The extracted values of sub-threshold slope for various MG MOSFETs are shown in figure 4. It is observed that $S$ increases as the channel length decreases due to SCE. Typically QG MOSFET has $S$, 400 mV/decade at 10 nm channel length, which is much lesser when compared to DG MOSFET that results in 993 mV/decade. This shows that QG MOSFET has less leakage current.

Transconductance ($g_m$) is a measure of gain which is obtained through the first derivative of the $I_D$ - $V_{gs}$ curve. The variations of $g_m$ with respect to channel length for various MG MOSFETs are shown in figure 5. It is observed that $g_m$ of QG

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MOSFET has 213 μS at channel length of 10 nm, the largest value compared to other types.

All the above analyses are done using HSPICE using BSIM-CMG (Level = 72) model as core. Vital model parameters, like silicon thickness and gate oxide thickness are chosen to be 20 nm and 1.5 nm respectively and maintaining the aspect ratio of 4.2 throughout the analyses is ensured.MG MOSFET's technology files are obtained from the predictive technology model which is approved by ITRS [6] and accessible in open source [14].Results show that QG MOSFET yields the best results among the other types. This is due to field lines of each gate which act vertically with respect to channel that result in better electrostatic control on the channel. This is in contrast to SG which has curved or bending field lines that lose its effective strength in controlling the channel charge. In a nutshell, more the number of gates covering the perimeter of the channel, higher the gate field, thus curbing the SCEs.

## 3. ANALYSIS OF SMALL SIGNAL GAIN

First the analytical model of drain current for SG MOSFET based on gradual channel approximation [12] is presented. SG MOSFET is chosen because of its simple construction that results in easier level of modeling. So this model is observed to be the fundamental for developing the other analytical models of multi-gate structures. For a long-channel, undoped (or lightly doped) symmetric SG MOSFET, $Q_m$, the total accumulated charge per unit gate length is given by

$$Q_m = 8\pi\varepsilon_s\,(kT/q)\left(\frac{1-\alpha}{\alpha}\right) \qquad (3)$$

The derivative of Eq. (3) gives the drain current

$$I_D = \mu\frac{8\varepsilon_s}{L}\left(\frac{k}{q}\right)^2[f(\alpha_d) - f(\alpha_s)] \quad (4)$$

$$f(\alpha) = \left(-\frac{2}{\alpha} - \ln\alpha\right) + s\left(-\frac{1}{\alpha^2} + \frac{2}{\alpha}\right) \quad (5)$$

f(α) is a polynomial that depends on applied voltage and the structural parameter s.

$$s = \frac{2\varepsilon_s \ln\left(1+\frac{t_{ox}}{R}\right)}{\varepsilon_{ox}} \qquad (6)$$

Here $R$ is the radius of silicon cylinder, $t_{ox}$ is the oxide thickness, $\varepsilon_s$ and $\varepsilon_{ox}$ are the permittivity of silicon and oxide, and $\mu$ is the effective mobility. Parameters, $\alpha_d$ and $\alpha_s$ are the solutions to Eq. (3) corresponding to $V = V_D$ and $V = V_S$ respectively, where $V_D$ and $V_S$ are the voltages applied to the drain and source respectively. α is determined by the boundary condition which has a final form[15] as

$$\frac{q(V_g-\Delta\emptyset-V)}{2k} - \ln\frac{2L_D}{R} = \ln\sqrt{1-\alpha} - \ln\alpha + s(1-\alpha/\alpha) \qquad (7)$$

Using Newton iteration method, the implicit equations, $\alpha_d$ and $\alpha_s$ are obtained by applying boundary condition given in [15]. Substituting

$$\alpha = \sqrt{z/(z+1)} \qquad (8)$$

into Eq. (7) and solving iteratively gives z1, z2 ,z3, etc.,. This resulted in determination of $\alpha$ during the third iteration (i.e., the intermediate variable ($z_3$)) giving the least error of $3.2 \times 10^{-13}$ with Eq.(7). Thus Eq.(4) gives the drain current model of SG MOSFET.

### 3.1Analytical $y_{21}$ of MG MOSFET

MG MOSFET's transconductance ($y_{21}$) is derived analytically based on the drain current model by assuming the device as a two port network. Significance of $y_{21}$ is that it determines the small signal gain and in this section, it is derived for a typical SG MOSFET. From Eq.(4), $I_{dso}$ can be obtained as

$$I_d = \mu\frac{8\varepsilon_s}{L}\left(\frac{k}{q}\right)^2 \qquad (9)$$

Differentiating Eq. (4) w.r.t. $V_{gs}$ yields

$$\frac{dI_D}{dV_g} = I_d\left(f'(\alpha_d)\frac{d\alpha_d}{dV_g} - f'(\alpha_s)\frac{d\alpha_s}{dV_g}\right) \qquad (10)$$

From Eq. (5), f'(α) is given as

$$f'(\alpha) = \frac{-1}{\alpha} + \frac{2}{\alpha^2}\left(1 + \frac{s}{\alpha} - s\right) \quad (11)$$

($d\alpha/dV_{gs}$) is obtained iteratively using Eq. (8)

$$\frac{d\alpha}{dV_g} = \frac{1}{2}\left(\frac{1}{(1+z)^2}\right)\sqrt{\frac{z}{1+z}}\frac{dz_3}{dV_g} \qquad (12)$$

Thus $g_m$ of SG MOSFET is calculated using Eq. (10) – Eq. (12) and the result is simulated using MATLAB. The tranconductance characteristics is shown in figure 6 which has sharp positive peak and resembles the ideal nature. Due to theoretical analysis, 3.5 x $10^{47}$, a huge gain is observed. Thus this part of the work is particularly important as the transconductance of the device is analytically derived. That is, analysis of small signal gain, $y_{21}$, of MOS device based on gradual channel approximation is done. This is considered as an extension of device modelling which is different from conventional research works which either focus on device modelling or circuit design.

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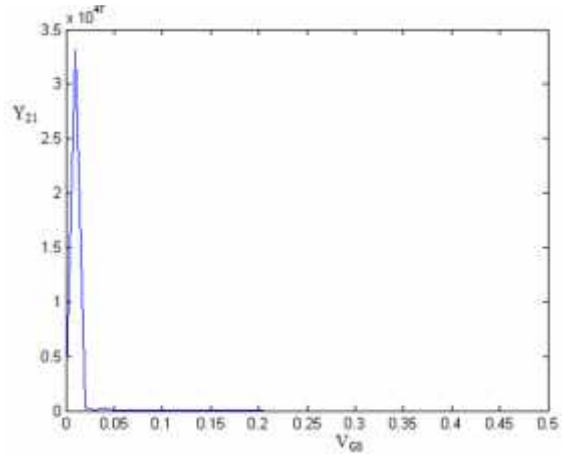


*Figure 6: Analytical $y_{21}$ of SG MOSFET*

This forms an intermediate step between the above two mentioned. From figure 6, huge gain confirms that MG MOSFETs forms an optimal choice for the design of 60 GHz transceiver.

## 4. LNA DESIGN USING MG MOSFETS

### 4.1 LNA Analysis

The circuit of single stage cascode LNA design is shown in figure.7 [16]. It is known that this configuration has high gain and substantial reverse isolation. The inductance used in the input side matches with the input impedance of MOSFET, thus providing indirect resistance component to match with signal source resistance, $R_S$.

Design of LNA using conventional MOSFET in mm/RF frequencies normally uses multi-finger gate structures. These structures increases the $f_m$ of the device and hence they are preferred. Here instead of multi-finger structures, MG MOSFET is used as it is proved as an optimal choice through the theoretical analysis of $y_{21}$ ($g_m$) shown in figure 6.Due to high $g_m$, the channel charging resistance of MG MOSFET, $r_t$, reduces.

$$r_t = \frac{1}{k g_m} \quad (13)$$

where $k$ is the constant whose value is 1 for short channel and 5 for long channel [17]. This work uses k=1 for manipulations. $g_m$ is the transconductance of the device. Results from figure 5 shows that values of $g_m$ of MG MOSFETs varies from (140-214) μ-S at channel length of 10 nm and the corresponding $r_t$ falls around 4.672 $K\Omega$ . Whereas in conventional single gate transistor, transconductance is observed to be (<20) μ-S, using the same identical device parameters as like MG MOSFETs. This yields the corresponding channel charging resistance, $r_t$ as 50 $K\Omega$. Almost 90.65 % reduction of $r_t$ takes place if MG MOSFETs are used. Thus the Non Quasi-Static (NQS) behavior of channel gets reduced. Therefore MG MOSFETs are the optimal choice for realization of RF/mm wave applications.

The analysis of inductive source degeneration based cascode LNA [16] is as follows: The input impedance of transistor, $C_{gs}$, is cancelled by the summation of input inductances, ($L_s$ + $L_g$) at the oscillation frequency $\omega_o$.

$$\omega_o = \frac{1}{\sqrt{L_g (L_s + L_g)}} \quad (14)$$

$$C_g = \frac{2}{3} W_o L_e C_o \quad (15)$$

where $W_{opt}$ is the optimum width of MOSFET, $L_{eff}$ is the effective channel length, $L_s$ and $L_g$ represents the source degenerated inductance and gate inductance. Source resistance ($R_s$), Quality factor of input matching circuit and $W_{opt}$ are given by

$$W_o = \frac{1}{3\omega_c L_e C_o R_S} \quad (16)$$

$$R_S = L_S \omega_T \quad (17)$$

$$Q_{in} = \frac{1}{2\omega_c R_S C_g} \quad (18)$$

For figure 7, the small signal equivalent of $M_1$ and $M_2$ considering along with the channel charging

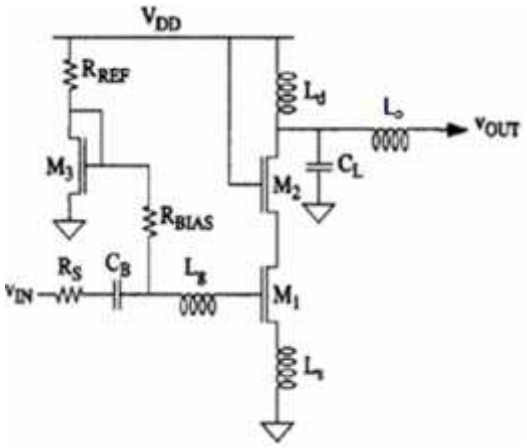


*Figure 7: Inductive Source Degeneration Based Cascode LNA[15]*

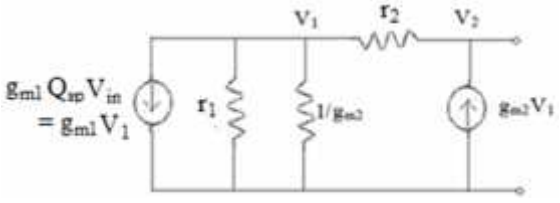


*Figure 8: Equivalent Noise Model Augmented in Source Degenerated Cascode LNA*

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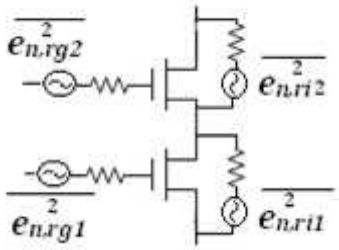


*Figure. 9: Noise Representation in Cascode Transistors*

resistances is shown in figure. 8. This is drawn as per [18]. Here $r_1 = (r_{i1} \parallel r_{o1})$; $r_2 = (r_{i2} \parallel r_{o2})$; The open circuit voltage gain is derived for figure 8. By considering the channel charging resistance,

$$V_2 = V_1(1 + g_{m2}r_{i2}) \quad (19)$$

$V_1$is obtained at node 1 and substituting in Eq. (19) and re-arranging, the open circuit voltage gain obtained is as follows:

$$A_v = -g_{m1}Q_s \ (r_{i1} \parallel r_{i2}) \quad (20)$$

From Eq. (20), it is evident that the voltage gain is greatly affected by parallel combination of $r_{i1}$and $r_{i2}$ of $M_1$ and $M_2$.

The next desirable parameter is Noise factor ($F$) which is given by [15]

$$F = \frac{T_1}{o} \quad (21)$$

At higher frequencies, in addition to drain current noise, gate resistance and channel charging resistance contribute significant noise output. Most of the research works have not considered channel charging resistance noise, so an attempt to include it in noise figure calculations has been made. So the effect of Non Quasi-Static (NQS) behavior of channel is considered in this work. Figure 9 represents the equivalent noise model for the cascaded transistors shown in figure 7.

The customized noise figure calculation is as follows: Generally noise equivalent voltage is calculated as mean square value. Noise voltage due to channel charging resistance of $M_1$ is

$$\overline{e_n^2} = 4K \ \Delta f(r_{i1}) \quad (22)$$

Where K is Boltzmann's constant
T is Temperature in Kelvin
Δf is Bandwidth

For LNA shown in figure 7, derived equivalent noise parameters are represented as $\overline{e_{r\ 1}^2}$ ,$\overline{e_{r\ 2}^2}$ , $\overline{e_{r\ 1}^2}$ and $\overline{e_{r\ 2}^2}$. These parameters represent equivalent noise voltage present at gates and the channels of $M_1$ and $M_2$.

Noise factor of cascode LNA considering channel charging resistance, gate resistance and drain current noise is given by

$$F = 1 + \frac{e_{n\ ,a1}^2 + e_{n\ ,a2}^2 + e_{n\ ,r\ 1}^2 + e_{n\ ,r\ 2}^2 + e_{n\ ,r\ 1}^2 + e_{n\ ,r\ 2}^2}{e_{n_s,R_s}^2} \quad (23)$$

Where $\overline{e_{n\ ,a1}^2}$, $\overline{e_{n\ ,r\ 1}^2}$ and $\overline{e_{n\ ,r\ 1}^2}$ are the output noise voltage due to drain current noise, gate resistance noise and channel charging resistance of $M_1$. Similarly $\overline{e_{n\ ,a2}^2}$, $\overline{e_{n\ ,r\ 2}^2}$and $\overline{e_{n\ ,r\ 2}^2}$ holds for $M_2$.

On substituting equivalent output noise values in Eq.(23), the expression reduces to

$$F = 1 + \frac{r_{g1}+r_{g2}+r_{i1}+r_{i2}}{R_S} + \frac{\gamma\, r_{i1}^2}{(r_{i1} \parallel r_{i2})Q_S^2\, R_s} \quad (24)$$

where $\gamma$ is 2/3 for long channel devices and $A_0$ is intrinsic gain of transistor $M_2$.

To increase the accuracy, the above analysis can be extended by including the substrate resistance that are present in $M_1$ and $M_2$.But as the operating frequency ids 60 GHz, the effect of parasitic resistance on noise figure can be neglected [16].

### 4.2 Design Methodology

The following steps are used for the circuit design shown in figure 7. Source and load impedance are chosen as 50 Ω and the value of $L_s$ is fixed.

1. Set the desired values for $F$ and $L_{eff}$.
2. Compute $L_g$ according to the fixed $L_s$.
3. Compute $\omega_T$, $C_{gs}$ and output inductance $L_o$.
4. Compute $g_m$ and its respective bias current.

The above calculations are done according to Eq.(14) to Eq.(18).

*Table1: MG MOSFET Based LNA Design*
*Legends: DG-Double Gate, TG-Triple Gate, QG-Quadruple Gate, SG-Surrounding Gate*

| Type of MOSFET | $L_g$(nH) $V_{DD}$= 1V/1.5V |
|---|---|
| Single Gate | 0.538/0.538 |
| DG | 1.05/1.05 |
| TG | 0.93/0.915 |
| QG | 0.85/ 0.831 |
| SG | 0.71 / 0.74 |
| Other elements | $R_S$ = 50 Ω, $R_{REF}$ = 100 Ω, $R_{BIAS}$ = 2 KΩ, Blocking Capacitor ($C_B$) = 10 pF,$L_d$ = $L_o$ = 3.53 pH, $C_L$ = 2 pF |
| (W/L) ratio | (10 µm/30 nm)=Amplifier; (10 µm/2 µm)=current mirror; |

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*Table 2(a):Output Parameters of LNA at 60 GHz Using MG MOSFETs ($V_{DD}$ = 1.0 V)*

| $V_{DD}$ | 1 V | | | | |
|---|---|---|---|---|---|
| | QG | SG | DG | TG | Single gate |
| $S_{11}$ (dB) | -14 | -14.2 | -12.5 | -13.6 | -7.9 |
| $S_{12}$ (dB) | -52.4 | -39.4 | -48.9 | -49.4 | -39.6 |
| $S_{21}$ (dB) | 3.7 | 2.87 | 3.07 | 3.49 | 1.32 |
| $S_{22}$ (dB) | -23.1 | -21.1 | -23.1 | -23 | -15.5 |
| F(dB) | 3.19 | 3.42 | 3.31 | 3.22 | 4.22 |
| K | 130 | 31.9 | 91.9 | 93.5 | 33.5 |

*Table 2(b): Output Parameters of LNA at 60 GHz Using MG MOSFETs ($V_{DD}$ = 1.5 V)*

| $V_{DD}$ | 1.5 V | | | | |
|---|---|---|---|---|---|
| | QG | SG | DG | TG | Single gate |
| $S_{11}$ (dB) | -15 | -14.9 | -11.7 | -13.2 | -7.95 |
| $S_{12}$ (dB) | -48.5 | -39.2 | -46.3 | -46.7 | -41.5 |
| $S_{21}$ (dB) | 6 | 4.98 | 5.15 | 5.65 | 1.11 |
| $S_{22}$ (dB) | -22.5 | -20.5 | -22.6 | -22.4 | -15.8 |
| F(dB) | 2.7 | 2.92 | 2.81 | 2.74 | 4.72 |
| K | 64.5 | 24.5 | 53.2 | 53.4 | 42.6 |

Based on the above procedure, table 1 gives the designed LNA components corresponding to figure 7 which operates in 1V/1.5V at 60 GHz. In this design, *F* is assigned and the rest of the parameters are designed accordingly for various MG MOSFETs. The corresponding design values for conventional single gate MOSFET are also tabulated.

## 5. RESULTS AND DISCUSSION

S-parameters are observed at 60 GHz for the proposed design by simulating it in HSPICE RF. Table 2(a) and Table 2(b) shows S-parameters, F and Stability Factor K for MG MOSFETs based LNAs which are designed using $V_{DD}$ as 1 V and 1.5 V respectively. The parameters corresponding to conventional single gate MOSFET is also tabulated. It is noted that $S_{21}$ of SG based proposed design is 2.87 dB, almost twice the value that yielded in single gate LNA design when operated at 1V. Similarly $S_{11}$ and $S_{22}$, the input reflection coefficient and output reflection coefficient of SG based LNA are twice than conventional design. It is also observed that the same parameters are far improved in case of QG based LNA design. The S-parameter profile for the SG and QG MOSFETs are given in figure 10 and figure 11 which shows that the proposed design resonate sharply at 60 GHz and hence ideally suits for narrow band amplifier.

The stability factor, K, when compared to conventional design, improves by 51% in QG based design operating at 1.5 V. This reveals that the proposed QG based LNA is suitable for varying load application including unconditional loads. But in SG based LNA, K is decreased which is due to non-directional gate field lines interacting with variable field lines at drain which when connected to variable loads.

In general, QG MOSFET gives excellent results when compared to other structures. It is due to the fact that, quadruple gate structure controls the channel (charge accumulates) as straight, directional fields in all four directions. Rather the other types of MG MOSFETs have tendency to bend the gate field lines in unidentified angular direction.

Table 3 gives the comparison of the proposed work with [19], [5] and with the conventional single gate MOSFET. Although the results of the proposed work depends on the number of gates surrounding the MOSFET, DG MOSFET alone is
.

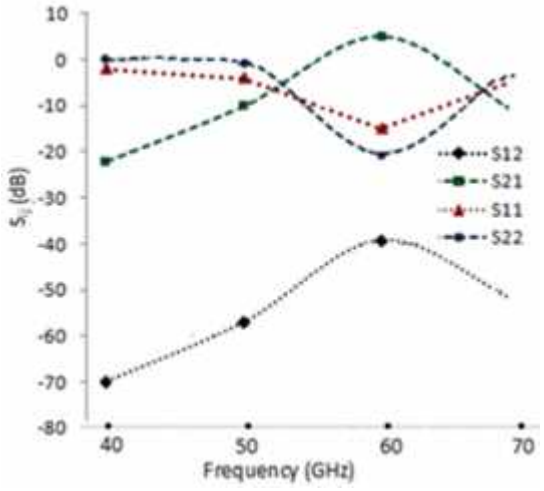


*Figure 10:S-Parameter Profiles for SG MOSFET*

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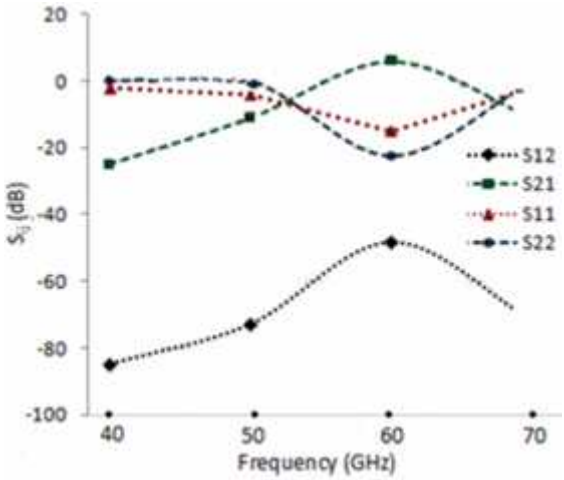


*Figure 11:S-Parameter Profiles for QG MOSFET*

*Table 3: Output Parameters of LNA at 60 GHz Using MG MOSFETs ($V_{DD}$ = 1.5 V)*

| | [19][1] | [5][2] | Single gate | This work[3] |
|---|---|---|---|---|
| Frequency (GHz) | 65 | -- | 60 | 60 |
| $S_{21}$ (dB) | 15 | 9.21 | 1.11 | 5.15 |
| Noise Figure (dB) | 7 | 1.675 | 4.72 | 2.81 |
| Circuit topology | Two stage, CS with cascode | Single stage, cascode | Single stage, cascode | |
| Voltage (V) | 1.2 | 1 | 1.5 | 1.5 |
| Description | *1 depends on back gate bias | *2 effect of underlap in FINFET | -- | *3 Depends on number of gates surrounding the channel |

chosen which is to be compared with the other literature. This is because of the availability of the design of LNA using similar kind double gate MOSFETs and FINFETs in [19] and [5]. Paper [19] is based on nanoscale double gate(DG) MOSFET and [5] deals on effect of gate overlap on source/drain FINFET devices. The number of fins in [5] determines the stability, control of drain current and transconductance of the device. So Table 3 gives a wide variation of results that seems to appear but in-spite of it, main parameters like $S_{21}$, NF and the circuit topology are taken for comparison. It is found that the proposed work involves single stage cascode design, so the voltage gain is slightly lesser than the other work. Whereas the noise figure is excellent for the proposed design when compared with [19] and single gate results. This conveys that SCE is totally suppressed in MG MOSFETs which is an appealing factor. Thus the characteristics of the proposed work are to reduce SCEs, increase the transconductance and involve the modeling of channel charging resistance in RF circuit design.

## 6. CONCLUSION

To curb SCEs on device performance, MG MOSFET is considered as better alternate device instead of conventional device. DC and AC parameters of various MG MOSFETs are extracted and analysed which forms the basis for designing RF circuits. Small signal gain ($y_{21}$) of a typical SG MOSFET is analytically derived based on gradual channel approximation and the transconductance curve is extracted. The high and sharp peak of $g_m$ shows that MG MOSFETs are suitable for mm/RF applications. This is an extension of device modelling that is needed for RF circuit design. Small signal modelling, design and simulation of MG MOSFETs based LNA circuit using simple procedural steps are done. The importance of channel charging resistance is considered and compared with single gate MOSFET in this work in addition to the gate resistance. The impact of channel charging resistance on noise figure calculations is attempted. It is observed that *F* improves by 24.4% for 1 V operating voltage and by 42.79% in 1.5 V operating voltage with respect LNA using conventional MOSFET.*S*-parameter profiles at 60 GHz are reported for the proposed design. This study gives an insight of LNA design using MG MOSFETs and perhaps the promising future area in MMIC transceiver design.

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