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LOW POWER IN NANO-SCALE CMOS MEMORY

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ABSTRACT

Future technologies required nano-scale CMOS memory to be operating in low power consumption. The minimum operating voltage of the nano-scale CMOS played as a main factor to reduce the power consumption. Consequently, there are some limitations and obstacles to achieve the objective for several design, material and novel structural solutions, which are promising and reliable. In this research, the noticeable limits, possible annexes and applications of CMOS technologies in the nanometer regime is discussed. This paper mainly describes the limitations that conventional MOSFET is faced. In addition, the solutions to low power in nano-scale CMOS memory are presented. Therefore, analysis of the attainable performance and potential restrictions of CMOS technologies from the point of design, material and structural solution techniques are illustrated.

Keywords: *Nano-Scale, CMOS, Low Power, Memory*

1. INTRODUCTION

In modern world, Integrated circuit (IC) is an advanced electric circuit by patterned diffusion of trace elements into the thin surface of a semiconductor material. All electronic equipment today is used IC and it has revolutionized the world of electronics [1-8]. Due to the introduction of complex metal oxide semiconductor (CMOS) technology, semiconductor devices spread through every discipline of engineering and CMOS memories become core component [9-15]. Memory cells are the essential part of semiconductor memory ICs. The features of memory cells are extensively affect the chip size, operational speed and power dissipation of memory devices. In very large scale integration (VLSI) technology, memories developed in CMOS process are utilized in a number of applications as the sources of store data in RFID applications [16-23]. Basic examination of the memory cells comprises structural, storage-mechanism, write, read, and design and improvement issues. Generally, a memory cell, which is applicable to CMOS memory designs, comprises a data storage circuit; one or more data access devices. Additionally, some designs have additional circuit elements. Almost all CMOS memories, one storage circuit or element is capable to hold one bit of binary information, but some storage elements are able to store a multiplicity of binary or non-binary data. Additional circuit elements may be used to improve environmental tolerance and to accommodate a variety of functions in a single memory cell.

In nano-scale CMOS memory, reducing minimum operation voltage V_{dd} is becoming very difficult to do in conventional bulk CMOS. The limitation in low-voltage V_{min} is one of the major problems [23-26]. As the technology of device minimization is increased, various effects such as delay, voltage margin of circuit, significantly increased in soft error rates, V_{min} etc also increased, V_{dd} must be increased with device scaling to offset such effects, which causes an increase in the power dissipation, as well as degrades the device reliability due to increased stress voltage [27-30]. Due to such inherent features of V_{t0} and V_{th}, V_{dd} is facing a 1V wall in the 65 nm generation, and is expected rapidly increase with further scaling of poly-Si bulk MOSFETs as shown in Figure 1 [24, 26]. To reduce the operating voltage V_{dd}, the minimum operating power supply V_{dd} (i.e V_{min}) as determined by V_{t0} and V_{th} must be reduced. This is because V_{dd} is the sum of V_{min} and ΔV, and V_{min} becomes much higher than ΔV in the nano-scale era. Here, $\Delta V$is the sum of the power-supply droop and noise in the power supply lines and substrate, the voltage needed to compensate for the extrinsic ΔV_tdue to short-channel effects and line-edge roughness, and the voltage needed to meet the

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speed target. In any event, for the LSI industry in order to flourish and proliferate, the 1V wall must be breached in the nano-scale era.

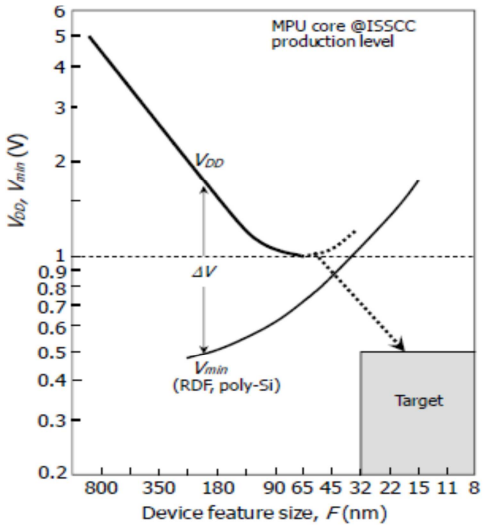

Figure 1. Trends In V_{dd} And V_{min} Of High-Performance Mpus [24,26]

The lowest necessary threshold voltage $V_T(V_{T0})$ of MOSFETs and the ever-increasing V_T variation are factors that cause V_{mins} to increase.Due to the variations in V_T, various problems occur, such as delay or wider variations in circuit speed, degradation of voltage margins of flip-flops and increased soft-error rates (SER) in RAM cells and logic rates [31-32]. Therefore, clarifying and solving the increasingly critical V_{min} problem is extremely important in our future.

This paper mainly describes the limitations that conventional MOSFET had and the solutions to low power the CMOS memories. These can be divided into three points of view. The first one is circuit design continue by material and finaly is the new structure of MOSFETs.

2. BACKGROUND

If V_{min} is defined as V_{DD}, which is necessary for achieving a tolerable speed variation $\Delta\tau_0$, is given as[1-9]:

$$V_{min} = V_{to} + (1+\gamma)\Delta Vtmax,$$

$$\gamma = 1/(\Delta\tau_0{}^{\frac{1}{1.2}} - 1,$$
$$\Delta V_{tmax} = m\sigma(V_t) \quad (1)$$

$$\sigma(V_t) = A_{vt}(LW)^{-0.5}, \text{and} A_{vt} \propto t_{ox} \quad (2)$$

where, V_{t0} is an average V_t with a maximum deviation in $V_t$fromV_{t0}, $\sigma(V_t)$ is the standard deviation of $V_t$distribution, and the speed variation is defined as the ratio of the slowest speed at thehighest $V_t$to the average speed at the average$V_t = (\cong V_{t0})$. For a conventional, bulk MOSFET

$$\sigma(V_t) = B_{vt}[t_{ox}(V_{t0} - V_{FB} - \Phi_S/LW]^{0.5} \propto t_{ox}N_A{}^{0.25}(LW)^{-0.5} \quad (3)$$

where m depends on the circuit count in the block, $A_{vt}$and $B_{vt}$are the Pelgrom and Takeuchi constants, respectively, $t_{ox}$is the inversion electrical gate-oxide thickness, $V_{FB}$is the flat-band voltage, $\Phi_S$is the surface potential, N_A is the impurity concentration of the channel, and LW is the MOSFET size [33-34].

In order to reduce minimum voltage $V_{min}$with smaller V_{t0}especially for low-power designs, the resultant leakage must be reduced dramatically. Therefore, two ways has been discussed in term of design technique solution, which are low minimum voltage $V_{dd}$and structural of operation. These solutions were applied on 6T SRAM type that is one type of CMOS memory.

By applying low minimum voltage V_{dd} the power consumption of the whole cell can be reduce [35-36]. The required voltage, which indicated as, $V_{min}$is very sensitive to the threshold-voltage variationsV_t . It significantly related with device scaling, and to the lowest threshold voltage,V_{t0}, of the cell. For example by reducing the supply voltage $V_{dd}$of the 6T, SRAM cell leads to the low leakage currents [37-38]. These leakage currents occur due to the electric fields that contains inside the cell. Consequently, the lower minimum voltage V_{dd} applied to the cell the lesser voltage V_{min} that the cell required [39].

A novel 6T Low power SRAM Cell with Synchronized Read and Write Circuitry has been designed and is shown in Figure 2. The numbers of High threshold voltage transistor (HVT) are contained in the cell to reduce the power dissipation [40]. During the Read and write Operation, timing has been set in this way to reduce dynamic power dissipation [41-42]. The Memory Cell is designed purposely for high value of Read and Write Margin and SNM so that the Cell has high stability level. Therefore, the total power dissipation can be reduced without any Area and Delay overhead.

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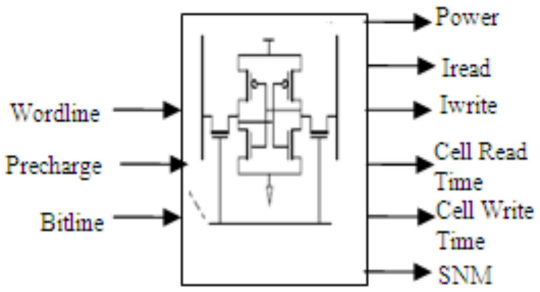

Figure 2. Memory cell with read and write circuitry [40]

There are also some other solution which by replacing the material of the CMOS. Hybrid-Graphene-Nanoribbon CMOS and Josephson-CMOS Hybrid memory has been widely discussed by researchers lately. These future technologies seem promises to reduce the power consumption as well as high-speed operation system.

Graphene produce special electrical properties seem to replace conventional CMOS material as Silicon technology move towards scaling limitation [44]. Previously several Graphene mainly electronic devices and interconnects have been proposed.

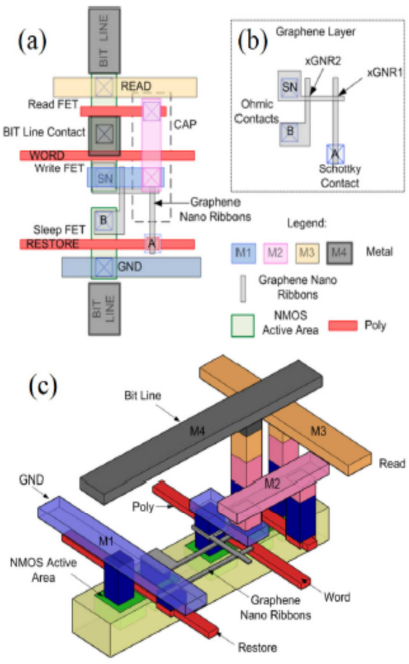

Figure 3. Proposed Graphene-CMOS Fabric (a) Layout Top View (b) Graphene Layer (c) 3D Integration between CMOS and Graphene [44]

The possibility of a hybrid fabric between CMOS and Graphene by implementing a novel Graphene Nanoribbon crossbar (xGNR) based volatile tunneling RAM (GNT RAM) and integrating it with the 3D CMOS stack and layout has been designed and is shown in Figure 3. Evaluation detailed of GNT RAM circuits show that they have reliable advantages in terms of power consumption, area and write performance over 16nm CMOS. This effort enlightens new idea other possibilities including multi-state memory fabrics and even an all-graphene fabric promises future technology.

A 64-kb Josephson–CMOS hybrid random-access memory (RAM) has been designed using ultrafast hybrid interface circuits, which is shown in Figure 4. The milli volt-level Josephson signals are amplified to volt-level CMOS digital signals by a hybrid interface amplifier. By minimizing the parasitic capacitance load, the performance of this amplifier is improved [45]. The 4-K operation of short-channel CMOS devices and circuits show some promises consequences. The memory bit-line output currents are detected by ultralow-power high-speed Josephson devices. As results the first high-frequency access time measurements on the full critical path showing 600 pS for a single bit. Therefore, the design can reduce the crosstalk and improve margins leads the reduction power dissipation and latency.

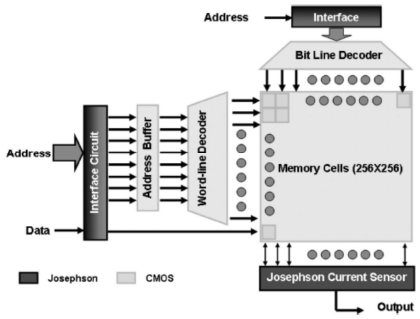

Figure 4. Hybrid memory system of 64 kb for measuring delays including overall access time for single cell [45]

Even though the hybrid technology become considerable and promises, some disadvantages disturb the evolution. The power dissipation for Josephson-CMOS can further be improved with special technology that target to be use at 4-K operation level. For Graphene technology to be mature, further work that focus on multi-state memory and fabric with all-Graphene seem potential and benefit. These new technology needs

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a number of further research and as well as manufacturing cost.

In our challenges to reduce voltage (V_{mins}), we realize that there is a limitation in a bulk-MOSFETs. An ultra-small voltage will not be achieved if we keep using the bulk-MOSFET. Thus, for compensation circuit and new device with small variation ofV_{mins} is required. The new device must be suitable for low-voltage operation, such as small-$A_{vt}$for small σV_t and scalable MOSFETs. For these challenges, FD-SOI and FinFET will be indispensable even though it is high in cost.

In order to minimizeV_{mins}, FD-SOI MOSFETS is the most important device [46]. Figure below shows the structure of FD-SOI MOSFET.

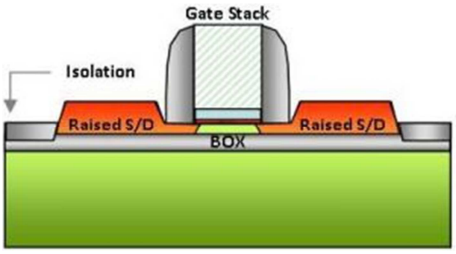

Figure 5. Planar of FD-SOI MOSFET [46]

FD-SOI is expected to reduce the variation of V_t to half or more. For example, if only the FD-SOI is used, the V_{min}in the 32-nm generation is reduced from 1.47 V to 0.93 V for SRAMs, 0.85 V to 0.58 V for logic gates, and 0.50 V to 0.35 V for DRAMs[47]. This device has small A_{vt} and can reduced short channel effect (SCE), body effect, afford a small SER etc. effectively [47-48]. Besides that, we can control the value of V_{t0} by changing the doping of the substrate under the UT-BOX layer. Moreover, FD-SOI with high-k metal gate will enable smaller variation of V_t [46].

Instead of using FD-SOI as a solution, FinFET also enable to reduceV_{min}. Figure 6 show the FinFET structure. A FinFET transistor is forming a double-gate structure. This device is called "finfets" because the source/drain region forms fins on the silicon surface. Generally, Double gate FET can reduce short channel effects and FinFET is the easiest one to fabricate [49]. What makes FinFET special is because we can use of an ultra low-dose channel and a wide-channel built-in structure [23, 26, 49].

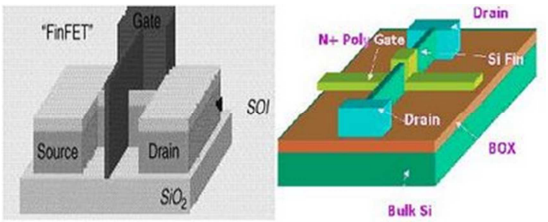

Figure 6. FinFET structure

Thus, it achieves not only a higher density and higher drive current but scalable *(V_t)* with up-scaling of the fin height (that is, channel width *W*) despite channel length *L* being scaled down. For an example, in 11-nm device generation(DRAM), basis on the MOSFET scaling, we can predict the V_{min} for HP design using FinFET manage to reduce until 0.22 V and for LP designs FinFET afford to reduce around 0.46 V[50].

However, the use of FD-SOI and FinFETs may also have some disadvantages. Besides the cost problem, the incremental of V_{to} variation among dies is occurring as well. This would impose a need for stringent control of shape uniformity on the FinFET, which will make the process of fabrication more complex.

3. DISCUSSION

Conventional MOSFETs will soon reach the limit of low-voltage owing to the increasing V_t variation. Several techniques have been proposed in term of design, material and structure solution. Nevertheless, these approaches have some limitation and suppose to be investigated in the future. Furthermore, it is essential to use the new MOSFET such as FD-SOI and FinFETs in CMOS memory. These new MOSFETs have advantages in having low V_{min}despite being miniaturized. This characteristic is important and very useful in low-power nano-scale devices. However, the new MOSFET is not able to compete with the conventional MOSFET because of high cost in production.

4. CONCLUSION

The low power in nano-scale CMOS memory is investigated in an effort to reduce the power consumption as well as device scale. By using, several design method and hybrid structure shown, that V_min, which is the key factor possible to be reduce and control. Some novel MOSFET

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structural include FD-SOI and FinFETs as a good alternative solution moving towards the future technologies.

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