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DESIGN OF LOW POWER LINEAR FEEDBACK SHIFT REGISTER

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ABSTRACT

Chip manufacturing technologies have been a key to the growth in all electronics devices over the past decades, bringing added convenience and accessibility through advantages in cost, size, and power consumption. Linear feedback shift register (LFSR) is key component to provide self-test of an integrated circuit (IC). This research is implemented LFSR until layout level which will be a key component for low power application. The research explores the LFSR as well as D flip flop using different architecture in a 0.18µm CMOS technology so that the layout area will be minimized as well as the power consumption will be lower. Three types of architectures are implemented into LFSR, which are NAND gates, pass transistor and transmission gates. Mentor graphics tools are used for comparing those LFSR design in terms of CMOS layout, hardware implementation and power consumption. The research showed that, pass transistor has smallest power consumption which is 3.1049 nano watts. Moreover, it required smallest number of transistor and layout area, which is 74 and 1137.76 micro square meter respectively.

Keywords: *LFSR, NAND Gate, Pass Transistor, Transmission Gate, CMOS*

1. INTRODUCTION

In Over the past decade, power consumption of very large scale integration (VLSI) chips has constantly been increasing. Moore's law drives VLSI technology to continuous increases in transistor densities and higher clock frequencies. The trends in VLSI technology scaling in the last few years show that the numbers of on-chip transistors increase about 40% every year and operation frequency of VLSI systems increases about 30% every year [1-4]. In modern societies, computers, mobile, phones, radio frequency identification tags and other digital appliances were intended to use for low power applications [5-7]. Although capacitances and supply voltages scale down meanwhile, power consumption of the VLSI chips is increasing continuously. On the other hand, cooling systems cannot improve as fast as the power consumption increases. Therefore in the very close future chips are expected to have limitations of cooling system and solving this problem will be expensive and inefficient [8]. VLSI low-power design automation will be guide to satisfy the power consumption requirements of modern IC. In order to apply the built in self-test (BIST) of an IC shift registers are required [9].

Linear feedback shift registers (LFSR) are a fundamental function in applications such as pseudo-random noise (PN) generators, Reed Soloman (RS) code generators and BIST [10]. BIST is a technique that enables an IC to test itself. BIST reduces test and maintenance costs for an IC by eliminating the need for expensive test equipment and by allowing fast location of failed ICs in a system. BIST also allows an IC to be tested at its normal operating speed, which is very important for detecting timing faults. Despite all of these advantages, BIST has seen limited use in industry because of area and performance overhead and increased design time. LFSR systems are typically designed either using field programmable gate arrays (FPGAs) or digital signal processors (DSPs). While this leads to a working system that is flexible, the achievable speed is limited by the fact that FPGAs and DSPs are general-purpose designs [11]. By using VLSI techniques to design an LFSR, the throughput can be increased and the LFSR is easily integrated into a system design since the area needed is minimal. This research presents three different automated techniques for implementing LFSR as well as D flip flop so that the layout area will be minimized as well as the power consumption will be lower.

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2. METHODOLOGY

LFSR counter required 4 block D flip-flop, XOR gate (with 2 input and 1 output) and or gate (with 2 input and 1 output). Seed are important and had been used as input pattern for LFSR counter. Based on hardware requirement, the most essential parts are D-flip flops [12]. Different D flip-flop methodology will give difference power consumption and layout sizing. The maximum length sequence of an LFSR is the longest number of cycles in the LFSR until the generated pattern repeats itself. One major characteristic of the maximum length sequence is that every state will only be entered once between repetitions. Thus, for an *N*-bit LFSR with appropriate feedback taps selected, the sequence will take 2^n-*1* clock cycles to repeat. The missing cycle is due to the lockup state of the feedback pattern [13]. Figure 1 shows the block diagram of a four-stage Fibonacci implementation. Since only two taps are required to configure the LFSR for maximum sequence length, a single XOR are used in the feedback path to perform the modulo-2 summation.

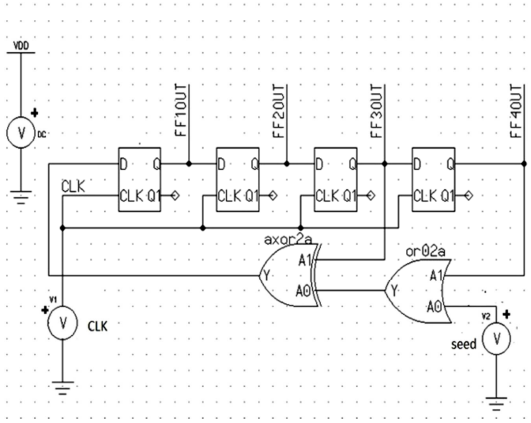

Figure 1: Block diagram of a 4-bit LFSR

In this 4-bit LFSR shown, there are 2^4-*1* or *15* states in the sequence. XOR gate were used in the feedback path, which does not allow them all *0* state, the unique values of the resulting sequence with a starting seed of 1,0,0,1 is shown in table 1. As the number of stages in the LFSR increases, it will affect the number of possible configurations of the feedback network to achieve a maximum length sequence. Each of these different configurations results in a different sequence generation [14]. If more feedback taps are used, then the equation to model the sequence becomes more complicated and thus the resulting maximum length sequence will be more complicated. The number of possible ways to configure the feedback as well as the number of taps used varies especially enlarger LFSRs [15].

Table 1: Unique values for a 4-bit LFSR

Clock	FF1_OUT	FF2_OUT	FF3_OUT	FF4_OUT
1	1	0	0	1
2	1	1	0	0
3	0	1	1	0
4	1	0	1	1
5	0	1	0	1
6	1	0	1	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1
10	0	1	1	1
11	0	0	1	1
12	0	0	0	1
13	1	0	0	0
14	0	1	0	0
15	0	0	1	0
16	1	0	0	1

In this research LFSR layout was designed by using *3* differences D-flip-flop technique and components such as NAND gates, Pass Transistor and Transmission gates. Mentor Graphics tools are used to design layout for D flip-flop and LFSR. In this research CEDEC KIT is used which is an IC design tools that enable to prepare an IC design which qualifies to be fabricates using Silterra 0.18µm CMOS process.

2.1 D Flip-Flop Design using NAND Gate

A master slave D flip-flop is created by connecting two gated D latches in series, and inverting the enable input to one of them. It is called master slave because the second latch in the series only changes in response to a change in the first (master) latch [16]. A D flip-flop takes only a single input, i.e. D (data) input. The master-slave configuration has the advantage of being edge-triggered, making it easier to use in larger circuits, since the inputs to a flip-flop often depend on the state of its output. Master slave D flip-flop construction using Mentor graphics design architecture IC (DA-IC) is shown in figure 2. The circuit consists of two D flip-flops connected together. When the clock is high, the D input is stored in the first latch, but the second latch cannot change state.

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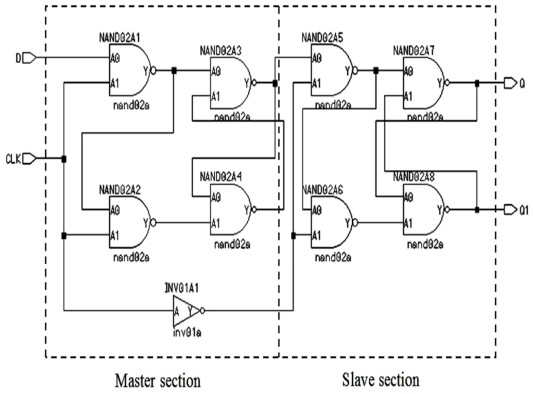

Figure 2: D Flip-Flop schematic using NAND gates

When the clock is low, the first latch's output is stored in the second latch, but the first latch cannot change state. The output can only change state when the clock makes a transition from high to low. Based on this theory, this research is designed several type of D-flip-flop. By designing it, comparison and analysis can be sustained in order to find circuits with less MOS for low power application. Layout of this D flip-flop using NAND gates before implemented at LFSR is shown in figure 3.

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Figure 3: D Flip-Flop layout using NAND gate

2.2 D Flip-Flop Design using Transmission gate

This flip-flop is realized by using four transmission gate based latches operating on complementary clocks [17]. Several varieties of the transmission gate based are available. For example, the feedback transmission gate may be eliminated or even PMOS transistors may be removed for transmission gates. However, in this research the simulation will only consider typical transmission gate based latch as shown in figure 4. The edge-triggered flip-flop is built from two D-type level-triggered latches. Both latches are enabled with opposite polarity of the clock signal. The second (or *slave*) latch is controlled by the clock signal, while the first (or *master*) latch is enabled by the negated clock [18].

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Fig 4: D Flip Flop schematic using transmission gate

As a result of this wiring of the clock signal, the first latch is transparent while the clock signal is low, and the current value of the D input is propagate to the input of the second latch. However, the input t-gate of the slave latch is non-conducting. Therefore, the flip-flop stores its current value (regenerated via the feedback loop of the slave latch). On the rising edge of the input clock, several things happen. First, the input t-gate of the master latch becomes non-conducting, while the feedback t-gate of the master latch becomes conducting. That is, the master latch stores its current value - the value it had immediately before the rising-edge of the clock signal. At the same time, the slave latch becomes transparent (its input t-gate is now conducting) and therefore outputs the value stored in the master latch. The new output value arrives at the Q output about three transistor delays (slave input t-gate, two inverter stages) after the rising edge of the clock signal [19].

When the clock signal turns low again, the input t-gate of the slave latch becomes non-conducting, while the feedback t-gate becomes conducting. That is, the slave latch keeps storing its current value, namely the value loaded during the preceding rising-edge of the clock signal into the master latch. At the same time, the master latch becomes transparent again and the D input value is propagated through the master latch onto the (now non-conducting) input t-gate of the slave latch [20]. Layout of this D Flip-Flop using transmission gate before implemented at LFSR is shown in figure 5.

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Figure 5: D Flip-Flop layout using Transmission gate

2.3 D Flip-Flop Design using Pass Transistor

Figure 6 show the most ideal of edge trigger latch that designed using pass transistor and inverter. This is done by configuring two D latches in master slave configuration. A master slave D flip-flop is created by connecting two gated D latches in series, and inverting the clock input to one of them. It is called master slave because the second latch in the series only changes in response to a change in the first (master) latch [21].

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Figure 6: D Flip Flop schematic using pass transistors

When *clk* is *0* the input D passes through the first level of pass transistor logic and held there because the second level does not pass on the value of D. When the clock input becomes 1, D is transferred to the output. Thereafter output Q does not change when D changes because D is not passed through the first level of pass transistor logic. Now when the clock changes back to *1*, Q still remains

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unaffected by the changes in D because it is now hindered by the second level of pass transistor. Thus, we observe that Q remains unchanged for the entire clock cycle and changes only at the positive edge [22]. Hence, the above transistor level diagram implements positive edge triggered flip-flop. Layout of this D flip-flop using pass transistor before implemented at LFSR is shown in figure 7.

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Figure 7: D Flip-Flop layout using pass transistors

3. RESULTS AND DISCUSSION

Conventional Integrated circuit design is becoming more complex every day. IC station is used to create the layout for the D flip-flops. These processes have been done after designing schematic and verified it using Mentor Graphics DA-IC. Layout versus Schematic (LVS) is a tool in IC Station that links an IC layout to a DA schematic sheet. The layouts of D flip-flop using difference architecture were implemented in this research.

By using mentor graphics tools, layout size can be measured. This software also applied for calculate power consumption and quantity of transistor in the layout. The comparison chart of the D flip-flop in terms of number of transistor, power consumption and layout area are shown in table 2. According to table 2, it is being shown that both the layout area and power consumptions are minimal while pass transistor is used.

Table 2: D flip-flop comparison using difference architecture

Component	No. of Transistor	Power Consumption (piko watt)	Layout Area (micro sq. meter)
NAND gates	34	1463.1	409.5
Transmission Gate	18	742.6332	312
Pass transistor	14	570.5188	241.8

The layouts of D flip-flop have been combined to make LFSR and the comparison between LFSR using NAND gate, transmission gate and pass transistor is shown in table 3. All these layouts are implemented using 0.18µm CMOS technology. Number of transistors, power consumption and layout area of D flip-flop and LFSR is varied in difference technologies. According to table 2 and table 3 the power consumption is much lower if pass transistor is used to design DFF and LFSR. The layout area also minimized if pass transistor is used for designing D flip-flop and LFSR.

Table 3: LFSR comparison using difference architecture

Component	No. of Transistor	Power Consumption (nano watt)	Layout Area (micro sq. meter)
NAND gates	154	683.50	1808.04
Transmission Gate	90	1523.7	1430
Pass transistor	74	3.1049	1137.76

4. CONCLUSION

This paper describes how D flip-flop design is important to get low power application for LFSR. By comparing LFSR design using NAND gate, transmission gate and pass transistor, the research showed that, pass transistor have smallest power consumption which is 3.1049 nano watt. This also applies to number of transistor and layout area, which is 74 and 1137.76 micro square meter respectively. Thus, pass transistor is the most efficient method that can be used to design LFSR.

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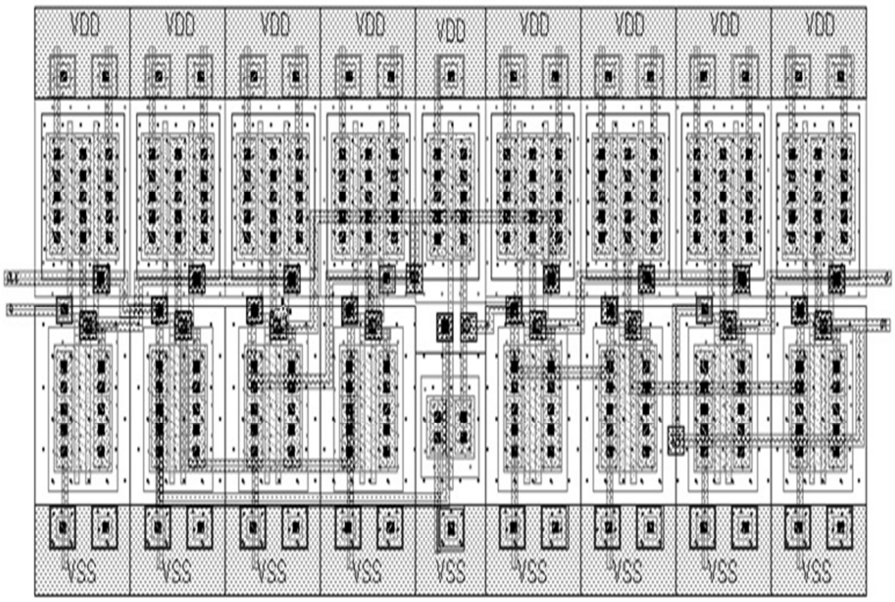

Figure 3: D Flip-Flop layout using NAND gate

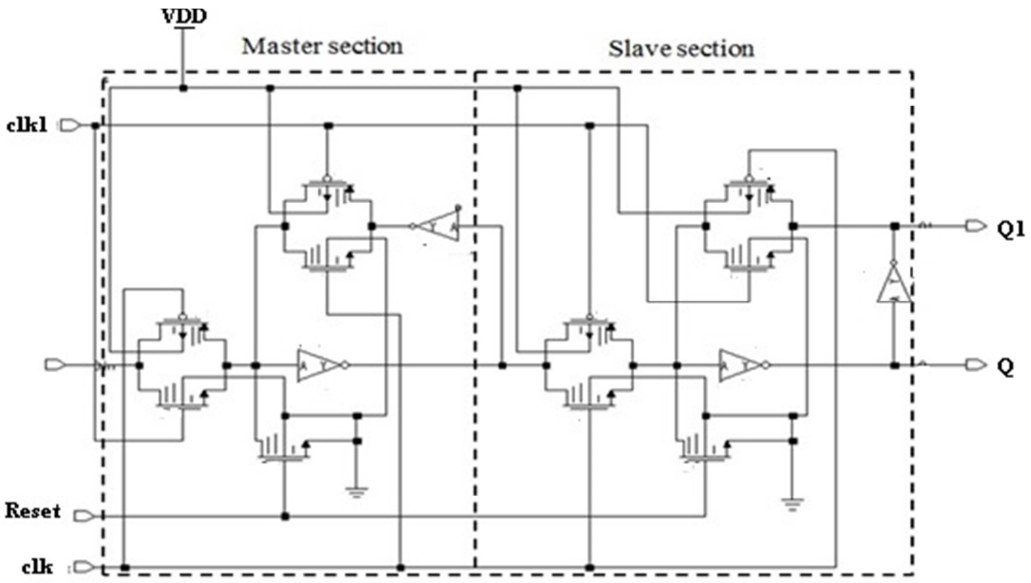

Figure 4: D Flip Flop schematic using transmission gate

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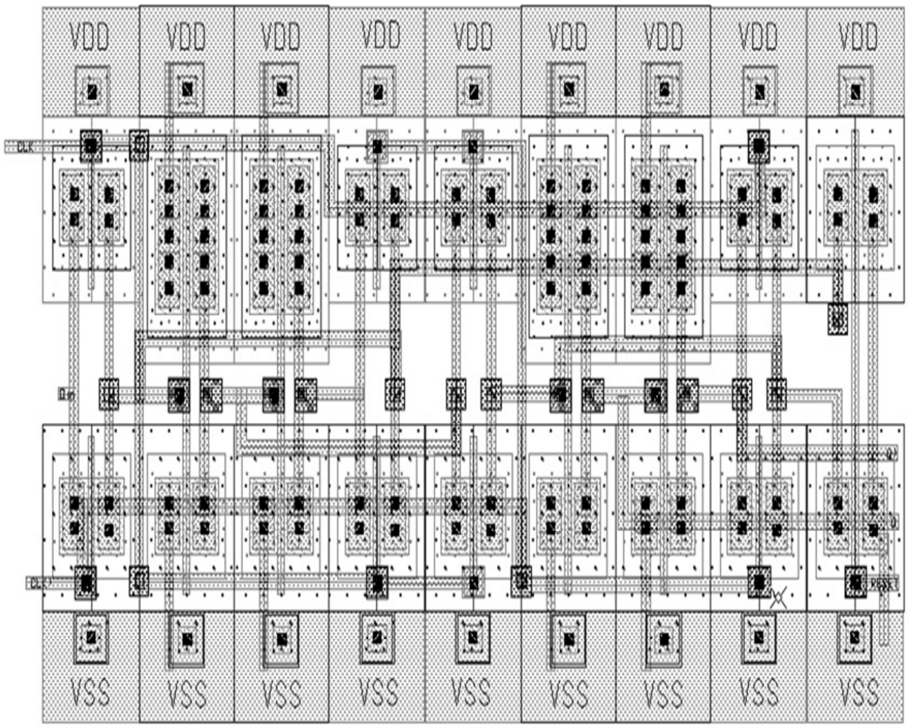

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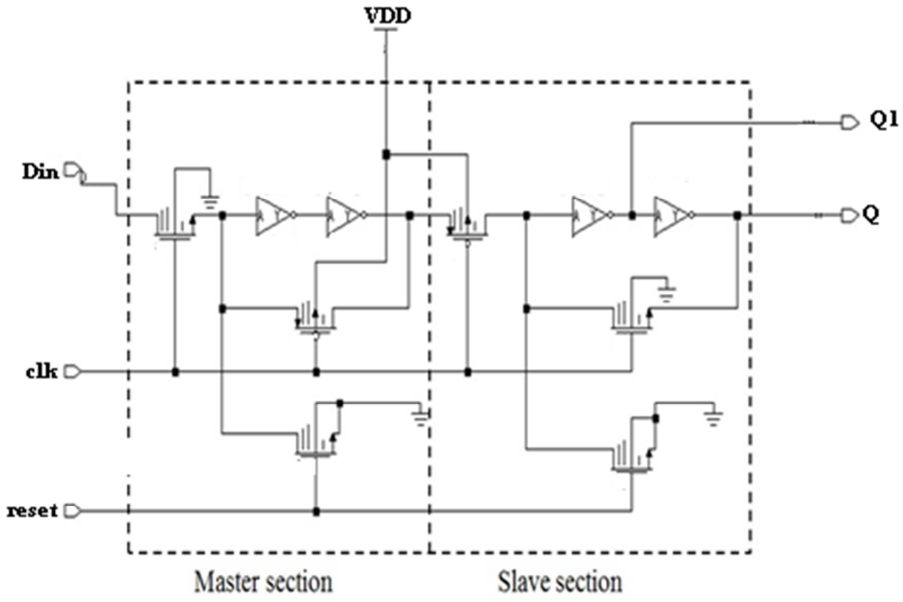

Figure 6: D Flip Flop schematic using pass transistors

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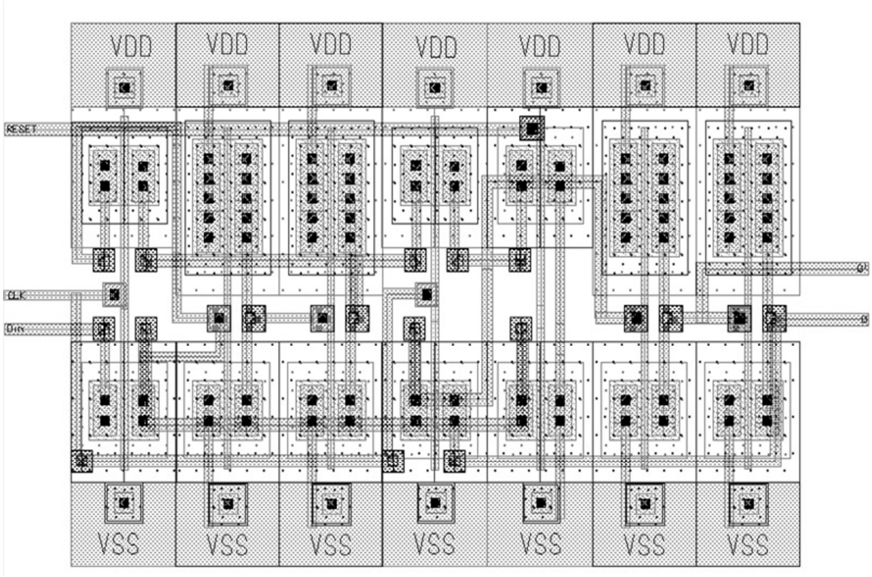

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