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NEW MODIFIED ELMORE DELAY MODEL FOR RESISTANCE-CAPACITANCE-CONDUCTANCE (RCG) INTERCONNECT NETWORK SCHEME

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ABSTRACT
This study presents a simple close-form delay estimate, based on first and second order moments that handle arbitrary voltages and conductance effects for a lumped and distributed line. This model introduces a simple tractable delay formula by incorporating conductance (G) into RC network by preserving the characteristics of the Elmore delay model. The accuracy of the interconnect delay estimates can be improved by deploying the conductance effect. This study proves that the proposed model attains quick steady state condition by incorporating the conductance in a RC network thereby reducing the delay in interconnects. The analysis is validated through extensive simulations on a 250 nm CMOS technology. The SPICE simulation shows the overall figure of merit has an improvement of at least 28% when compared to RC Elmore Model and existing RLC interconnect scheme.

Keywords: *Elmore Delay, RCG Interconnect, RLC Network, Figure Of Merit, Damping Ratio*

1. INTRODUCTION

Interconnects are used to connect components on a chip and it constitute to be a dominant source of circuit delay for modern chip designs. They are typically modeled as RC circuits and RLC circuits based on the studies of the delay models all of which aim at more accuracy with less computational effort.

The traditional approach to determine the signal delay for both analog and digital circuits has been estimated using Elmore delay (also called classical delay model). But this model provides limited accuracy and limited to estimate the delay of the circuit for only step inputs. These issues has been surmounted by incorporating a compound interest problem to the existing Elmore delay to improve the efficiency of the RC interconnect scheme.

The RC interconnect approach has been reported by [1], this approach improves the signal delay, albeit this scheme has been applicable for RC network alone. In [2] reported a closed transfer function method to find the delay estimates using an arbitrary RC with classical Elmore model. This model provides delay accuracy to the first order RC network.

The model proposed in [3] developed a simple closed-form delay estimate, based on first and second moments, which considers the effect of inductance. Using this model significant accuracy in delay can be obtained but applied only for step type signals. The primary issue in this model is; inefficient in calculating the time response of under damped conditions when the interconnect network grows linearly. This issue has been surrogated by the model developed by Y.I. Ismaiel [4]. Their model deals with closed form of RLC network which finds the delay for both damping and under damping response of RLC network when there is linear progression in the interconnection occurs. But the primary constraint in this model is second order approximation is complex for RLC nodes.

Moment matching approach has been developed by Alioto [5] which includes the analysis of input admittance of RC interconnects. This model determines first and higher order moments of RC networks. Their approach incorporates fully analytical and lacks certain constraints for CAD issues. Aysmptotic Waveform Evaluation (AWE) proposed by [6] provides a generalized approach to waveform estimation for RLC circuits. This approximation model will not be suitable for larger and higher order moment interconnects.

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Abou-Seidoet [7] proposed a new interconnect delay model named Fitted Elmore Delay (FED) using curve fitting technique. Determinations of curve fitting coefficients are much complicated for larger RC networks. Interconnects are also modeled using S-parameter by estimating series impedance and parallel admittance using telegraph equations has been proposed by [8]. This approach finds suitable only for smaller interconnects.

The model proposed by [9] evaluates the performance of interconnect by deploying the property of conductance to improve the characteristics properties of delay. It is limited for lumped model and step input. A delay model for RLC trees based on algebraic equations and an algorithm has been proposed based on the lie formula Sourajeet Roy [10]. Though the model can be applied to step and ramp input type of signals, it is inefficient for second order delay modeling and limited to only first two circuit moments.

Moment based Delay Modeling for On-Chip RC Global VLSI Interconnect were also introduced by developing Two pole RC model based on first, second and third moment effect into the delay estimate for interconnect lines [11]. This model takes higher order circuit moments for accuracy in delay, but it is not applicable for second order systems. ABCD matrix delay model has been developed by [12] which are used for calculating the Delay by finding first two circuit moments with ABCD matrix. Each interconnect lines is modeled with ABCD matrix. The total delay is divided into two: transport delay and interconnect rise time delay. As Transport delay is included, the delay and rise time delay is more accurate than other model and inductance effect is also considered but in terms of circuit moments it is not more efficient.

The literature survey reported in this study focus only on the interconnect delay model involving resistance, capacitance and inductance effects. But as the technology scales down the significant of conductance plays a vital role for improving the device performance as well as in delay aspect. This study presents a new modified Elmore model (MEDL) which incorporates the effect of conductance to improve the delay for lumped and distributed interconnect networks.

2. MATERIALS AND METHODS

Elmore delay model (EDM) has been widely employed to approximate the interconnect delays in the performance driven analog and digital very large scale integration (VLSI) devices. This delay model estimates the first moment of the impulse response using a simple closed form expression in terms of design parameter like resistance and capacitance used in the interconnect scheme. This interconnect delay models a wire as a segment of resistance and capacitance which is connect in series as shown in Fig. 1. For lumped model the delay of the circuit is directly proportional to its resistance (R) and capacitance (C). For distributed network with a segment i, the resistance R_i proportional to its length, width of the wire and ρ resistivity of the sheet.

The delay for a lumped RC interconnects is modeled as the time constant (τ) of an RC interconnect. So the delay for a lumped RC interconnect is

$$\tau = RC \quad (1)$$

The delay for the distributed RC interconnect is modeled as the total sum of the delay in each node

Delay at node 1 (N1) : $\tau_1 = R_1C_1$ (2)
Delay at node 2 (N2) : $\tau_2 = (R_1 + R_2)C_2$ (3)
Delay at node 3 (N3) : $\tau_3 = (R_1 + R_2 + R_3)C_3$ (4)

In general the delay for the distributed RC network is calculated as

$$\tau_n = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + (R_1 + R_2 + ...R_n)C_n \quad (5)$$

If $R_1=R_2....R_n=R$ and $C_1=C_2...C_n=C$, then the delay is modeled as

$$\tau_n = RC + 2RC + ...nRC \quad (6)$$

The Elmore delay equation explains the delay from input to output of the input signal, which is of a step function type. If the step response of the RC circuit is h (t), 50% point delay of the monotonic step response is the time τ_n that satisfies the above equation. There are three major problems associated with this approach. The first problem is obtaining the poles and residues for practical size interconnect circuits. The second problem associated is, this model is inaccurate and it is applied for first order moment system. The third problem, delay model cannot capture the effect of inductance of interconnect, to estimate the delay and the accuracy would be deteriorated when clock frequency increases.

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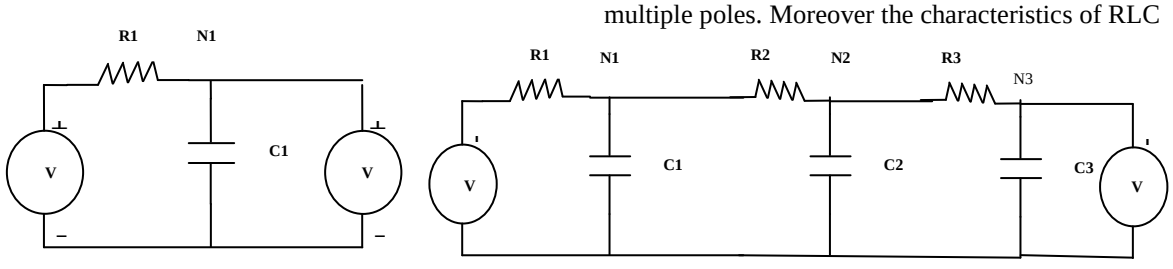
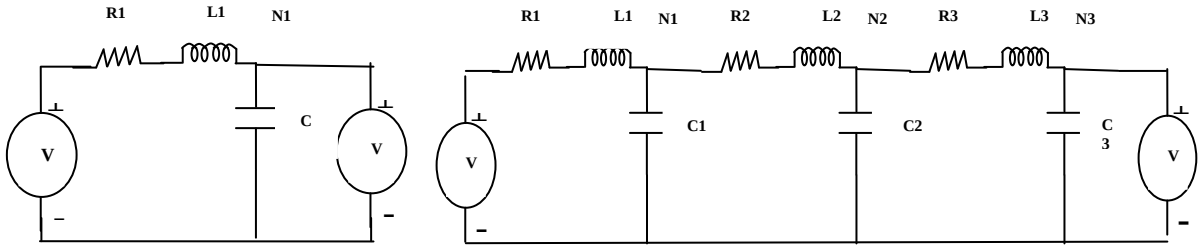
multiple poles. Moreover the characteristics of RLC



(a)

Figure 1: Elmore interconnect scheme. a. Lumped model b. Distributed



(a)

Figure 2: RLC interconnect scheme. a. Lumped model b. Distributed network

To achieve higher accuracy, a two-pole model which is based on RLC interconnects are employed to estimate the delay. The model is based on the first two moments. The delay model gains higher accuracy than RC due the second moment capturing effect of the inductance. Recently, metrics for RLC interconnects have been proposed based on the first three central moments [R. Gupta et al; 1997] [13]. These three central moments are used to detect underdamping condition and control of inductance effects. The lumped and distributed RLC model is shown in Fig. 2.

The delay for a lumped RLC interconnects is modeled as the time constant of an RLC interconnect. So the delay for a lumped RLC interconnect is

$$\tau = 2L/R \quad (7)$$

The delay of the distributed RLC interconnect is modeled as the total sum of the delay in each node

$$\tau_n = \frac{2L}{R} + \frac{R^2 + RL + 2L}{R} + \frac{2R^2 + 2RL + 2L}{R} + ... \frac{nR^2 + nRL + 2L}{R} \quad (8)$$

The major drawback of RLC models are: these interconnect schemes responds to step input and does not characterize the overshoots and settling time of an under damped response. Furthermore, three different equations has to be formulated to calculate the real, complex and model does not focuses to closed-form solutions for the moments of a interconnect tree. The other draw backs of inductive RLC circuit are: extracting the inductance is in general a 3-D problem and is extremely time consuming for complex geometry. Generally inductance depends on the entire current loop therefore it is impractical to extract the inductance from the chip layout. The primary focus of this study is to introduce a simple tractable delay formula for RCG network preserving the characteristics of the Elmore delay model with improved accuracy in the interconnect delay scheme (model).

3. PROPOSED RCG DELAY MODEL

This study presents a simple close-form delay estimate, based on first and second order moments that handle arbitrary voltages and conductance effects for a lumped and distributed line. This model introduces a simple tractable delay formula by incorporating conductance (G) into RC network by preserving the characteristics of the Elmore delay model. This Modified Elmore Delay Model (MEDL) with RCG interconnect considers a uniform wire that is schematized as lumped or distributed RCG network whose total resistance Rtotal = ρL/W and capacitance Ctotal= βLW which is proportional to its length L. The general property of the RCG network is portrayed as:

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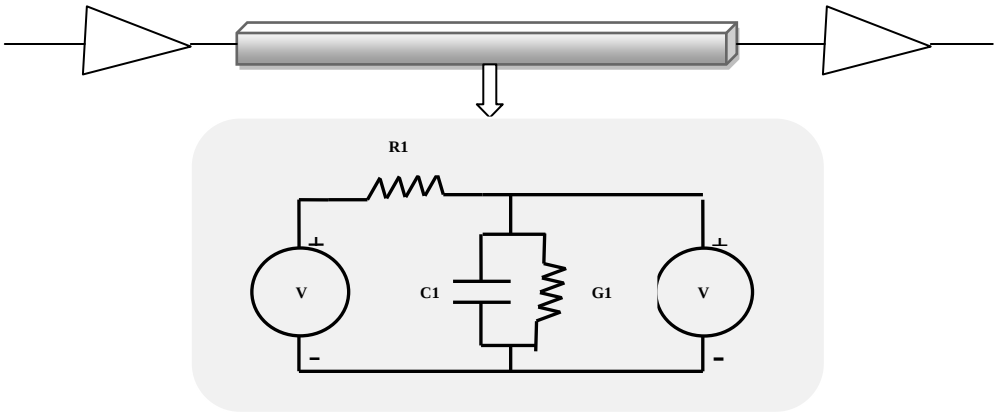

Figure 3: Proposed RCG lumped

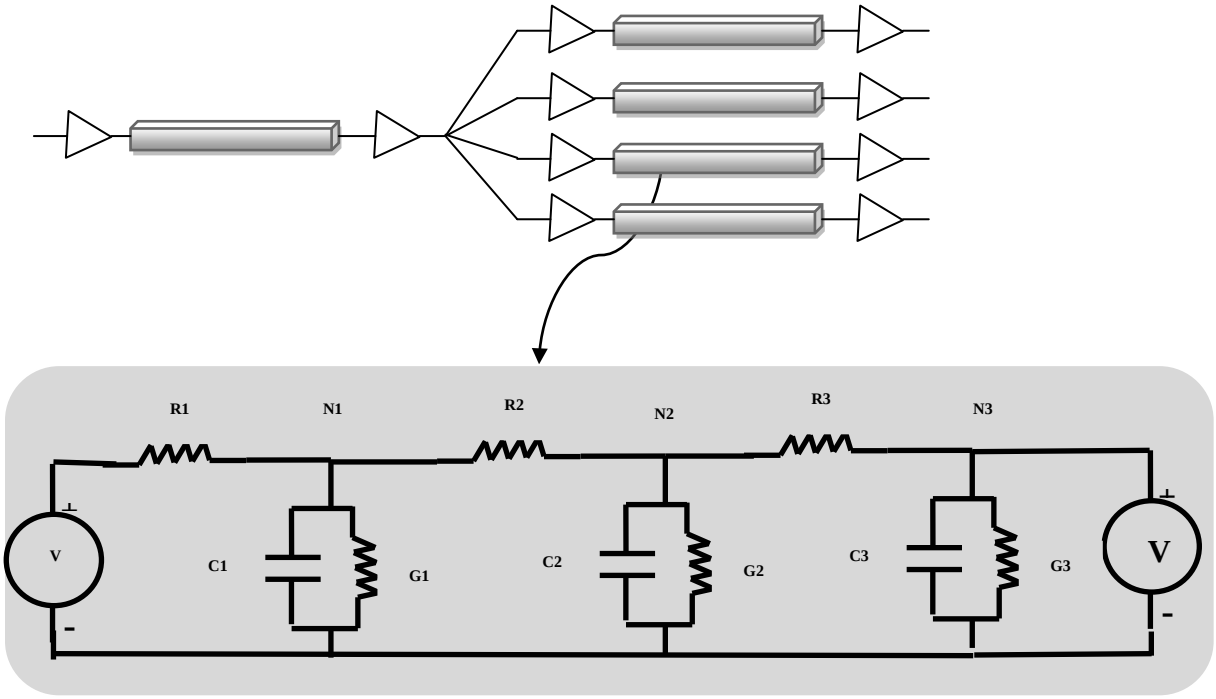

Figure 4: Proposed RCG distributed model

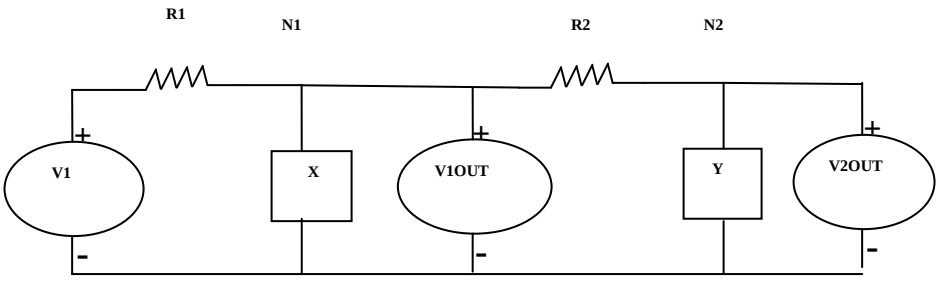

Figure 5. Second order proposed RCG model

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- In this proposed model the root node is connected through drivers (buffers) and there may be several loading capacitances connected along the interconnect network.
- The first moment and the second moment of transfer function from source to sink is calculated using recursive approach (iteration formula)
- The interconnect network is divided into several segments. Each segment is associated with a series resistance and parallel connected capacitance and conductance.
- Resistance along each segment i related to, $R_i \propto 1/w_i$, where $w_i \rightarrow$ width of the wire along i^{th} segment.
- Capacitance along each segment i related to, $Ci \propto w_i$, where $w_i \rightarrow$ width of the wire along i^{th} segment.
- Conductance along each segment i related to, $G_i \propto w_i/L_i$, where $w_i \rightarrow$ width of the wire along i^{th} segment, $L_i \rightarrow$ length of the wire along i^{th} segment.

The delay estimates for lumped network is shown in Fig. 3. To estimate the delay of lumped model the transfer function of simple RCG ladder is calculated. The delay equation is derived by taking input voltage (V_I) and output voltage (V_O) is time dependent function which is of linear differential equation.

From output side equation we obtain the transfer function as

$$V_O(S) = \frac{(1/CS)11G}{R + (1/CS)11G} V_I(S) \quad (9)$$

$$\frac{V_O(s)}{V_I(S)} = \frac{1}{(1 + (R/G) + RCS)} \quad (10)$$

$$H(S) = \frac{1}{(R/G + 1)(RCSG/R + G) + 1} \quad (11)$$

Taking inverse Laplace for the transfer function results in

$$H(j\omega) = \frac{1}{\sqrt{RC\omega^2 + 1}} \quad (12)$$

$$H(j\omega) = \frac{1}{\sqrt{\frac{\omega}{\omega 1}^2 + 1}} \quad (13)$$

Where $\omega 1 = \frac{(R+G)}{RCG}$

$\tau = \frac{RCG}{(R+G)}$ is the change in output voltage $V_O(t)$ is delayed by the time constant.

$$\tau = \frac{RCG}{(R+G)} \quad (14)$$

Fig. 4. Shows the proposed distributed model. For distributed network the entire interconnect is divided into various segments. Each segment consists of series resistance and parallel connected capacitance and conductance. First the transfer function of the ladder is estimated with single resistance (R), capacitance (C) and conductance (G). Then using the recursive node approach, the next segment delay is calculated using the preceding and successive node. This process is continued till the last segment of interconnect network and the transfer function is applied between the source and the sink. The delay estimate for the distributed network is shown below In second order model Fig. 5, G1 is parallel to C1

$$X = G_1 \parallel \frac{1}{SC_1} \Rightarrow X = \frac{\frac{G_1}{SC_1}}{G_1 + \frac{1}{SC_1}} \Rightarrow X = \frac{G_1}{SC_1G_1 + 1} \quad (15)$$

G_2 is parallel to C_2 , so Y is modeled as

$$Y = G_2 \parallel \frac{1}{SC_2} \Rightarrow Y = \frac{\frac{G_2}{SC_2}}{G_2 + \frac{1}{SC_2}} \Rightarrow Y = \frac{G_2}{SC_2G_2 + 1} \quad (16)$$

v_{1out} ,the output voltage at node1 is calculated using the voltage divider rule with respect to input voltage applied

$$V_{1out} = \frac{XV_1}{R_1 + X}$$

$$V_{1out} = \frac{\left(\frac{G_1}{SG_1C_1 + 1}\right)V_1}{R1 + \frac{G_1}{SG_1C_1 + 1}} \quad (17)$$

$$V_{1out} = \frac{G_1V_1}{SG_1C_1R_1 + R_1 + G_1}$$

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V_{2out} , the output voltage at node2 is calculated using the voltage divider rule with respect to input voltage applied

$$V_{2out} = \frac{YV_{2in}}{R_1 + Y}$$

$$V_{2out} = \frac{\left(\frac{G_2}{SC_2G_2 + 1}\right)\left(\frac{G_1V_1}{SG_1C_1R_1 + R_1 + G_1}\right)}{R_2 + \frac{G_2}{SC_2G_2 + 1}} \quad (18)$$

The closed loop transfer function of a second order system can be written as

$$\frac{V_{2out}}{V_1} = \frac{G_1G_2}{\left(SR_2C_2G_2 + R_2 + G_2\right)\left(SG_1C_1R_1 + R_1 + G_1\right)}$$

$$H(S) = \frac{G_1G_2}{S^2G_1C_1R_1G_2C_2R_2 + SR_2C_2G_2(R_1 + G_1) + SG_1C_1R_1(R_2 + G_2) + (R_2 + G_2) + R_1 + G_1)}$$

$$H(S) = \frac{\frac{1}{C_1R_1C_2R_2}}{S^2 + \frac{S(R_2C_2G_2(R_1 + G_1) + R_1C_1G_1(R_2 + G_2))}{R_2C_2G_2R_1C_1G_1} + \frac{(R_1 + G_1)(R_2 + G_2)}{R_2C_2G_2R_1C_1G_1}} \quad (19)$$

By comparing the above equation with the characteristic equation, which is given in the form

$S^2 + 2\xi\omega_n + \omega_n^2$

We obtain the values of ω_n & ξ

$$\omega_n = \sqrt{\frac{(R_1 + G_1)(R_2 + G_2)}{R_2C_2G_2R_1C_1G_1}} \quad (20)$$

$$\xi = \frac{1}{2}\frac{R_2C_2G_2(R_1 + G_1) + R_1C_1G_1(R_2 + G_2)}{\sqrt{R_2C_2G_2R_1C_1G_1(R_1 + G_1)(R_2 + G_2)}} \quad (21)$$

Where ω_n is the natural frequency

ξ is the damping ratio, is a parameter characterizes the frequency response of a second order ordinary differential equation and it is a measure of how rapidly the oscillations decay from one bounce to the next. When ξ value is zero the system remains undamped and when it is less than 1 the system is said to be underdamped , whereas the value is greater than 1 , then the system said to be overdamped condition when it is equal to 1 it is in critically damped condition.

The delay can be calculated from the below equation

$$\tau = \frac{1}{\xi\omega_n}$$

$$\tau = \frac{2R_2C_2G_2R_1C_1G_1}{R_2C_2G_2(R_1 + G_1) + R_1C_1G_1(R_2 + G_2)} \quad (22)$$

The above derived equation is the delay equation of the second order MEDL model. The damping ratio and delay expression for the proposed RCG MEDL, RC and RLC interconnect scheme is shown in Table 1.

Table 1: Damping ratio and Delay for RC , RLC and Proposed RCG

DR	RC	$\frac{1}{2}\frac{R_1C_1 + R_2C_2}{\sqrt{R_1C_1R_2C_2}}$
	RLC	$\frac{1}{2}\frac{RC}{\sqrt{LC}}$
	Proposed RCG	$\frac{1}{2}\frac{R_2C_2G_2(R_1 + G_1) + R_1C_1G_1(R_2 + G_2)}{\sqrt{R_2C_2G_2R_1C_1G_1(R_1 + G_1)(R_2 + G_2)}}$
D	RC	$\frac{2R_1C_1R_2C2}{R_1C_1 + R_2C_2}$
	RLC	$\frac{2LC}{RC}$
	Proposed RCG	$\frac{2R_2C_2G_2R_1C_1G_1}{R_2C_2G_2(R_1 + G_1) + R_1C_1G_1(R_2 + G_2)}$

DR : Damping Ratio D: Delay

4. SIMULATION RESULTS

The proposed model is simulated using simulation tool TANNER ASIC-EDA tool in order to compare the results in terms of delay and power. The model is simulated by taking typical values of resistance R= 10k, capacitance C=1pf and conductance G=0.1M for lumped and distributed interconnects. Buffers are inserted into RCG lines to partition an interconnect line into shorter sections and for signal integrity, thereby reducing the total propagation delay and the corresponding rising time, fall time are calculated. Input signal is unit step signal and the delay estimates refer to 50% threshold voltage. In this experiment, simulations are performed for RC and RLC for distributed and lumped and its performance are compared with proposed model. The interconnect dimension are taken for 0.250 µm technology with

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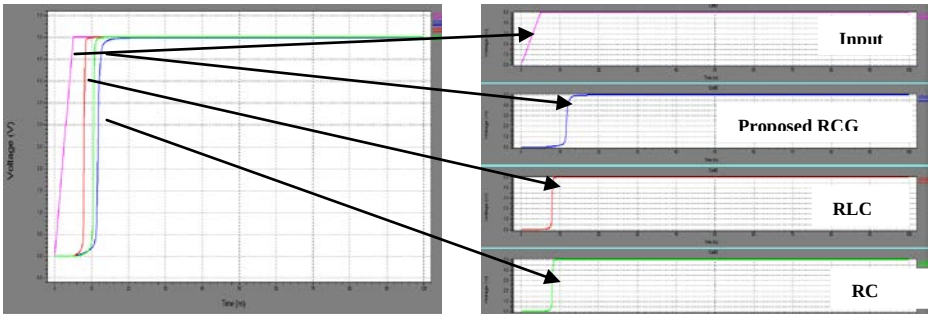

Figure 6: Simulation results proposed RCG lumped model

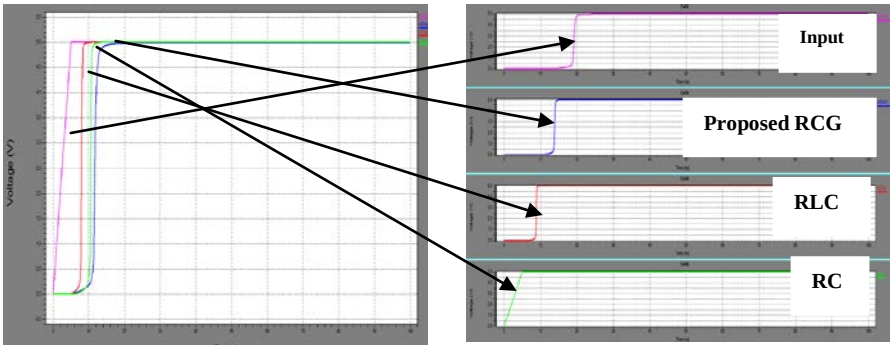

Figure 7: Simulation results proposed RCG distributed model

Table 2: Delay obtained for Various R, C and G for lumped model

R (kΩ)	C (pf)	G (mS)	Theoretical Delay (nS)	Simulated Delay (nS)
10	1	0.1	5	5.5769
8			4.44	4.6071
6			3.75	3.3251
4			2.8571	3.0656
2			1.666	1.8939
1			0.9090	1.1197
10	2	0.1	10	10.819
	4		20	21.350
	6		30	29.447
	8		40	36.710
	10		50	47.024
10	1	0.09	5.26	5.5997
		0.08	5.55	5.6252
		0.07	5.88	5.3587
		0.06	6.24	5.3839
		0.05	6.66	5.5531

Remarks: Simulated delay time=time difference between input transition (50% level) and the 50% output level .The theoretical values are obtained through equation (14)
R= Resistance, C=capacitance, G=conductance

Table 3: Delay obtained for Various R, C and G for distributed model

$R_1=R_2$ (kΩ)	$C_1=C_2$ (pf)	$G_1=G_2$ (mS)	Theoretical Delay (nS)	Simulated Delay (nS)
10	1	0.08	5	10.688
8			4.44	8.6561
6			3.75	6.6673
4			2.85	5.3331
2			1.666	3.7349
1			0.9090	2.9631
10	2	0.08	10	19.086
	4		20	38.367
	6		30	51.333
	3		40	29.786
	5		50	46.515
10	1	0.07	5.88	10.133
		0.06	6.24	10.461
		0.05	6.66	10.268
		0.04	7.05	10.927
		0.03	7.29	11.605

Remarks: Simulated delay time=time difference between input transition (50% level) and the 50% output level .The theoretical values are obtained through equation (22) R= Resistance, C=capacitance, G=conductance

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Table 4: Simulated results for power and figure of merit obtained for various voltages.

Interconnect scheme	Type of interconnect	Voltages (v)	delay (ns)	Rising time (ns)	Fall time (ns)	Power (µw)	Figure of merit x10^{-6}
lumped model	RC [1]	2	7.6074	0.7351	0.5078	0.477	3.628
		2.5	7.3844	0.5960	0.4238	0.479	3.537
		3.3	7.8278	0.5961	1.2514	0.474	3.710
		4.2	7.5788	0.4742	2.1319	0.469	3.554
		5	8.5908	1.2430	2.5253	0.456	3.917
	RLC [3]	2	7.6066	0.7286	0.5068	0.477	3.628
		2.5	8.0121	0.5961	1.2514	0.474	3.797
		3.3	7.8809	0.7625	1.8254	0.468	3.688
		4.2	7.5768	0.4714	2.1312	0.469	3.553
		5	8.5446	1.2353	2.5249	0.456	3.896
	RCG[prop]	2	6.0466	2.7260	0.2420	0.473	2.860
		2.5	4.6493	2.2437	1.0272	0.464	2.157
		3.3	5.2921	1.4797	0.2300	0.464	2.455
		4.2	4.5972	2.1390	0.2595	0.474	2.179
		5	5.5769	2.6508	2.1005	0.455	2.537
distributed model	RC [1]	2	16.225	0.6935	0.9249	0.476	7.723
		2.5	15.613	0.5661	1.1233	0.473	7.384
		3.3	15.502	0.6918	1.6364	0.467	7.239
		4.2	15.315	0.6740	1.8890	0.470	7.198
		5	16.712	0.6837	1.1882	0.476	7.954
	RLC [3]	2	16.280	1.1090	0.9210	0.477	7.765
		2.5	15.580	0.5791	1.1212	0.473	7.369
		3.3	15.911	0.5184	0.3181	0.475	7.557
		4.2	15.304	0.6659	1.8864	0.469	7.177
		5	16.060	1.1624	1.1162	0.476	7.644
	RCG[prop]	2	9.7487	1.8991	0.9536	0.457	4.455
		2.5	9.9506	0.8327	0.2690	0.470	4.676
		3.3	10.646	0.8682	0.2096	0.468	4.982
		4.2	9.645	1.3236	0.2594	0.473	4.562
		5	10.688	1.1482	0.6042	0.455	4.863

Remarks:
rising time=time for a waveform to rise from 10% to 90% of its steady-state value.
falling time= time for a waveform to fall from 90% to 10% of its steady-state value.
Power reported is an average power
Figure of Merit has been calculated by the taking the product term of delay and average power consumption.
The interconnect scheme is simulated for fixed values of R, C and G. R=10kΩ, C=1pf, G=0.1mS

minimum cross-section of 0.33µm and 0.18µm. The time response for lumped and distributed interconnect scheme is shown in Fig. 6 and 7 . The time response is analyzed for the step response of 200ns with input voltage of 5v and output response obtained is an exponential curve. From this experimental setup it is noticed that the output response is faster for the proposed RCG interconnect scheme. Table 2 and 3 shows the delay parameter obtained through simulation and theoretical values for different values of R, C and G for lumped and distributed model

Table 4 presents the simulated results for power and figure of merit obtained for various voltages keeping R, C and G as constant. For this observation R value is taken as 10kΩ and C value is 1pf and conductance is 0.1mS. The figure of merit defines the relative utilization to characterize the performance of a device. This parameter is obtained by taking the product term of propagation delay and the average power dissipation. In this experiment the minimum voltage

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Table 5: Percentage improvement in delay, power and figure merit for the proposed RCG interconnect scheme with respect to existing RC and RLC interconnect scheme

Interconnect scheme	Voltages (v)	Overall improvement with respect to Proposed RCG in terms of different voltages		
		% improvement in delay	% improvement in power	% improvement in figure of merit
Lumped model w.r.t RC	2	20.51	0.83	21.16
	2.5	37	3.13	39
	3.3	32.39	2.1	33.82
	4.2	39.34	**-1.06**	38.68
	5	35	0.2	35.23
Lumped model w.r.t RLC	2	16.53	0.83	21.16
	2.5	41.97	2.1	43.98
	3.3	32.84	0.4	33.43
	4.2	39.32	**-0.5**	38.67
	5	34.73	0.21	34.88
Distributed model w.r.t RC	2	39.91	3.99	42.31
	2.5	36.26	0.63	34.56
	3.3	31.32	**-0.21**	31.17
	4.2	37.04	**-0.63**	36.62
	5	36.04	4.41	38.86
Distributed model w.r.t RLC	2	40.11	4.19	42.62
	2.5	36.13	0.6	36.54
	3.3	33.09	1.47	34.07
	4.2	36.97	**-0.85**	36.43
	5	33.44	4.41	36.38

taken for this analysis 2V and the maximum of 5V. The rise time is calculated for a waveform to rise from 10% to 90% of its steady-state value. The fall time is calculated for a waveform to fall from 90% to 10% of its steady-state value. Table 5 elucidates the percentage improvement in delay, power and figure merit for the proposed RCG interconnect scheme with respect to existing RC and RLC interconnect scheme.

5. DISCUSSION

A new interconnect scheme RCG model and is its performance issues are presented. The percentage of improvement in delay, power and figure of merit of proposed interconnect with respect to RC and RLC for lump and distributed models. The analysis of the proposed study illustrates progressive improvements with RC and RLC in terms of delay, power and figure of merit. From Table 5 it is noticed that the percentage of delay is much improved for RC model than RLC interconnect model. For the lumped RC model with minimum voltage of 2V, the delay factor has improved to 21% and 40% improvement when the supply voltages reaches 4V keeping all the values of R, C and G as constant. Similarly for distributed network there is 40% improvement attained for the input voltage of 2V to 5V. For RLC lumped model

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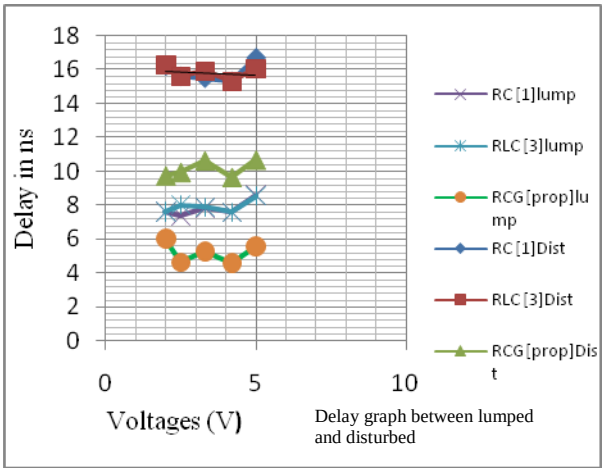

Figure 8: Delay comparison chart

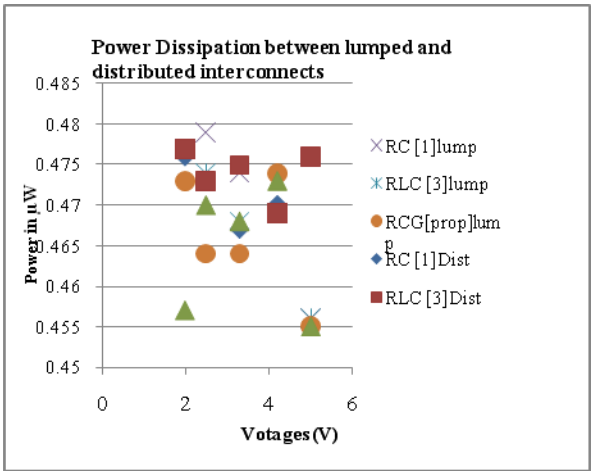

Figure 9: Power comparison chart

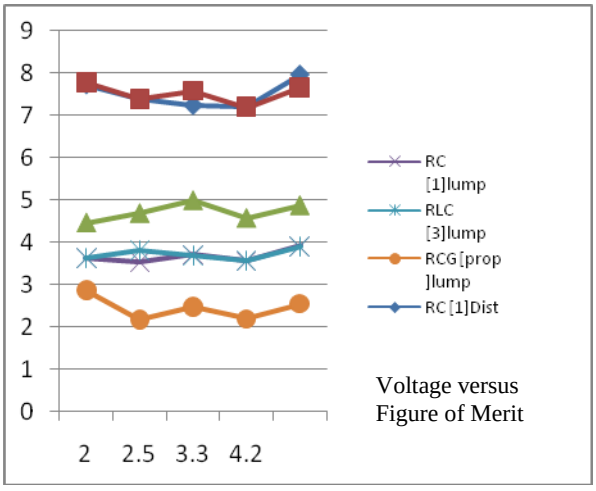

Figure 10: Figure of merit comparison chart

the minimum improvement is 16% to a maximum of 40%. When comparing the power aspect, for certain voltages there was no improvement which is indicated in negative sign. For figure merit the minimum improvement is 21% which is obtained for lumped RC with the voltage of 2V and maximum improvement of 43% for lumped RLC model for the supply range of 2.5V.

Fig.8 shows the delay chart for proposed and existing interconnect scheme for different voltages. For the minimum supply voltage of 2V the delay factor for RC [1] lumped is 7.6074ns, for RLC [3] lumped is 7.6066ns and for the proposed model the delay factor is 6.0466ns. Similarly for the maximum of 5V the delay is observed to be 8.5908ns for RC [1] lumped, 8.5446ns for RLC [3] and 5.557ns for the proposed model. So from this analysis it is well tactic that the proposed model performs better than its existing counterparts for the lumped and distributed networks. Fig. 9 depicts the performance of power consumption between RC, RLC and proposed model. Fig. 10 presents the figure of merit comparison chart for the proposed and existing interconnect model.

6. CONCLUSION

This analysis systematically derives closed form delay equation for the proposed RCG interconnect scheme by taking second order moments into account. The simulation results shows the proposed interconnect scheme performance is better than the existing in terms of delay, power and the figure of merit. The performance analysis shows the proposed RCG interconnect scheme has improved in reducing the delay to the maximum of 42 % and 43 % improvement in the figure of merit. The analysis has been done for different voltages by taking different values of R, C and G values. Comparisons on performance analysis shows the RCG interconnect scheme to be more efficient than the existing counterparts. The model proposed suitable for applying in larger circuit will show significant improvement in delay and power.

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