

# ENHANCED ERROR CORRECTION FOR MEMORY CELLS IN SPACE: A DUAL APPROACH TO RANDOM AND BURST FAULT DIAGNOSIS

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## ABSTRACT

This paper presents a novel method of fault diagnosis in memory cells that can be employed for space applications. The method presented here capable of diagnosing both random faults as well as burst errors. The proposed method is composed of two techniques one of the technique aims at targeting the random faults while the other aims at diagnosing the burst errors. The diagnosis of random faults is obtained by employing the extended decimal matrix coding whereas the burst errors diagnosis is done by Flexible Unequal Error Method. This method gains an adequate advantage in increasing the length of burst errors coverage based on the probability of distribution of the random faults. In addition to these little overhead bits were added to increase the diagnosis of burst errors. Experimental results conclude that the proposed error correction code achieves 100% of error correction rate for 5bit adjacent errors and six-bit random errors and better error correction rates up to 8-bits compared other ECC's that are considered for experimental purpose. However, this enhancement in error correction rate is achieved at a cost of slight increment in overhead of redundant bits.

**Keywords:** *Random errors, Burst errors, Encoder, Decoder, Modified Decimal Matrix code, Flexible Unequal Error control (FUEC).*

## 1. INTRODUCTION

The scaling of CMOS technology provides memory systems with great storage. This also created significant impact on critical charge required to store in memory cell for their corresponding identification. This reduction of critical voltage has increased the chances of occurrences of errors. Random errors and burst errors are the two major types of errors that are commonly observed in the memories. In general, random errors are a single bit of error whereas burst errors multibit in nature. Random errors are the errors that are expected to occur at any part of the memory in the available space. Whereas, burst

errors are those that are expected to occur in successive memory cells. Some of these errors may be very critical such that they may damage hardware. Hence there is huge necessity to develop techniques that increase the reliability of the memory devices by adopting error detection and correction methodologies. The concept of increasing reliability by adopting error detection and correction techniques is not a new one, this has been successfully employed for various decades. The modern architecture for error correction codes is given in fig.1

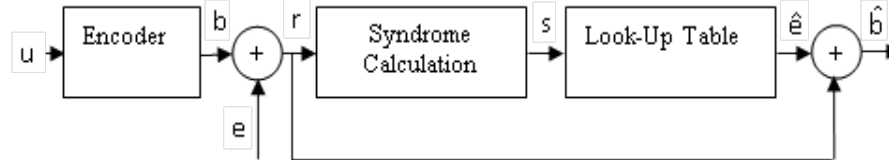


Fig 1. Architecture of Modern ECC's

The general principle involved in modern architecture Error Correction Code is depicted in fig.1. Here 'u' represents the input data and 'b' represents encoded form of input data by adding redundant bits. In general, these redundant bits are referred to as code bits. The number of code bits appended depends on the principle of ECC. The coded data 'b' is allowed to pass through unreliable channel and as the channel is unreliable there is every chance for error 'e' to creep into coded form of data. The received data 'r' can be erroneous or error free depending on whether the encoded data is exposed to noise or not. The integrity of the received data can be verified by computing XoR operation between 'b' and 'e'. In other words, if the value of 'r' is equal to zero then the data is free else it is erroneous. The received data is given for syndrome calculation. The calculation of syndrome is governed by the principles of type of Error Correction Code that is being employed. It must be noted that there must be a different syndrome (s) for each correctable error (e). The value of syndrome gives presence or absence of error. We can assume that if  $s=0$ , then there is no error, else error is present in the received data. The syndrome decoding is done by relating syndrome(s) with decoded error ( $\hat{e}$ ) in lookup table. Finally, the decoded codeword ( $\hat{b}$ ) is given as  $r \text{ XoR } \hat{e}$ .

In broad many of the ECC's target detection and correction of either random errors or burst errors. Here, we aim to present a novel method of error correction mechanism that can correct both random errors as well as burst errors. The proposed methodology objective is to integrate MDMC with FUEC. The performance of the error correction is optimized for both random and burst errors. The latency and handling complexity is significant. The existing methods like hamming, matrix and DMC can't handle burst errors effectively and the latency time is more. These reasons motivated us to propose hybrid methodology to handle both random and burst errors at higher performance. Multi-dimensional errors, faults and specifically burst errors, handling capacity are good with FUEC. With this integrated approach, efficiency and latency time is improved. Optimize each memory bit for correcting both random and burst errors. Improve the redundancy

and performance specifically, for heterogeneous memory systems. The proposed hybrid error correction mechanism enhances the error correction rate. Decoding is addressed in this study to minimize its complexity.

The hybrid methodology is designed to handle multi-dimensional matrices. Critical bit protection is considered with FUEC. The developed memory models are simulated and tested to implement MDMC+FUEC by adding random and burst errors. Metrics are evaluated considering the ability of error correction, redundancy overhead and latency. The proposed hybrid error correction code enhances the flexible redundancy and reliability

## 2. RELATED WORK

The initial seed for error correction using ECC's is laid by Richard W. Hamming [1] by introducing Hamming code. In general hamming codes allow only a single bit error correction, however a modified hamming [2-4] codes able to detect short burst errors. Hamming code using replication [5] effective against handling triple soft errors in memories. Hamming codes along with redundancy techniques [6] can effectively handle soft errors in memories that are employed for space applications. A new CLC algorithm [7] using extended hamming code can detect and correct multiple errors in memories that are employed for space applications.

Reed Muller [8] codes are being effectively employed in wireless communication more particularly in deep space communications and optical communications [9]. Symmetric Reed Muller codes [10-12] are effective in correcting errors locally. Berger codes [13] is successful in detecting all unidirectional errors that have been flipped from zero's one's or one's to zeros. These codes find its application in the design of BIST technologies [14] for combinational circuitry and ROM memories more particularly in DRAMs [15, 16] and CAM's [17] for detecting, correcting, and localizing unidirectional errors. Reed- Solomon code [18] is popularly employed for correcting burst errors in mass storage find its application in

Satellite Communications and image processing techniques for space applications. A method of automatic polynomial selection for RS codes has been given in [19] to improve fault tolerance in embedded memories

Cyclic Redundancy Check [20] is popularly employed for detecting error errors in telecommunication networks and storage devices. This can also correct double bit [21] and single burst error [22] errors effectively. Further it can be effectively employed for error detection in high-speed semiconductor memories [23, 24]. Single Device Data Correction decoding scheme [25] can achieve 100% error detection rate for DRAM.

The mix codes or hybrid codes that combine one or more error detecting codes are successfully employed for protecting the memories from the cell upsets. The combination of LDPC and hamming code [26], BCH and LDPC [27] and LDPC with majority logic along with difference set codes [28] were quite successful in protecting the memories from cell upsets to a great extent. Another class of mix code combining error correction capabilities DMC and PMC codes has been designed [29] to detect multiple cell upsets that can yield better performance with respect to maximum error correction with complete error detection.

In modern architecture, the memories are generally protected with SEC codes due to their simplicity in architecture. Pedro Reviriego et, al [30, 31] difference set codes can successfully correct triple bit errors with reasonable hardware requirements. The [32, 33] presents a matrix coding mechanism that makes use of hamming and parity codes to assure reliability. These codes were also successful in detecting adjacent errors [34]. Improved Redundant matrix code [35] is also successfully employed to detect and correct cell upsets is SRAM's. Further, a much significant step in protecting the memories is laid by Decimal Matrix [36 and 37, 38].

### 3. PROPOSED METHOD

The proposed architecture of fault diagnosis mechanism is composed of two architectures. One architecture is mainly employed to target the diagnosis of the random faults where as the other aims at diagnosis of the burst errors. The fault diagnosis of random faults is obtained by employing Modified Decimal Matrix Coding [39] (MDMC) whereas the diagnosis of burst errors is obtained using Enhanced FUEC [40]. Bit flips and transient errors occur due to electrical noise, and

these errors are called soft errors. Soft errors means these can be detected and corrected. Random error faults are detected with MDMC mechanism and burst error faults are detected with FUEC procedure. Error protection is provided at every level and specifically at priority bit level with FUEC. This is not achieved with existing methods. Read Solomon is another mechanism for random error faults. For correcting localized errors, Reed Solomon detects entire block, and syndromes and then computed with pre-determined log and antilog tables. But MDMC intersect each row and column and apply the correction immediately without relying on tables. The proposed methodology is addressed the hardware challenging by minimizing the complexity.

#### 3.1 Modified Decimal Matrix Coding (MDMC):

The block diagram of modified Decimal Matrix encoder is given in fig.2. It uses hamming encoder for formulating horizontal and vertical check bits. After formulating the check bits the modified code is stored in SRAM along with data bits and the same is recalled during decoding process to verify whether the data being is read is in original form or erroneous form.

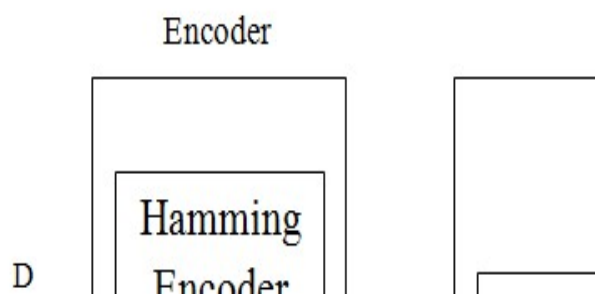


Fig 2. Block diagram of Modified DMC (MDMC)

#### 3.2 Modified Decimal Matrix Code (MDMC) ENCODER

The modified DMC encoder employs hamming code for calculated overhead data bits. The circuit employed for formulating check bits composes of hamming encoder and XOR gates is shown in fig.3. The 'N' bit data taken from source is divided into 'k' symbols, each symbol is of m-bit length that yields  $N=kXm$  and these symbols are arranged analytically in a  $k1Xk2$  matrix form such that  $k=k1Xk2$ , where  $k1$  indicates rows and  $K2$  indicates columns. The horizontal check bits are formulated by using hamming codes for each symbol of first row and thus each symbol is measured as decimal integer. The vertical check bits

are formulated by using xor operation for every column.

**3.3 Modified Decimal Matrix Code (MDMC) Decoder:**

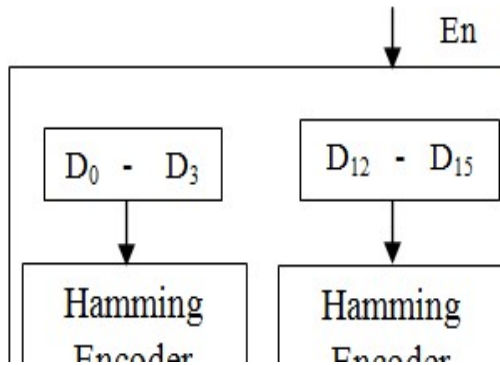


Fig. 3. Architecture of Modified DMC Encoder

The decoder shown in fig.4. is used to detect and correct the errors consequently. The received data bits 'D' are applied to the inbuilt encoder block in the decoder block to obtain horizontal check bits 'P<sub>0</sub>' to 'P<sub>11</sub>' and vertical check bits 'V<sub>0</sub>' to 'V<sub>15</sub>'. The decoding process is made to navigate through syndrome calculator, error locator and error corrector. The decimal integer subtraction is employed to formulate horizontal syndrome bits and XOR operation is executed for formulation vertical syndrome bits. The non-zero horizontal syndrome bits indicates error detection where as vertical syndrome bits give the location of the error.

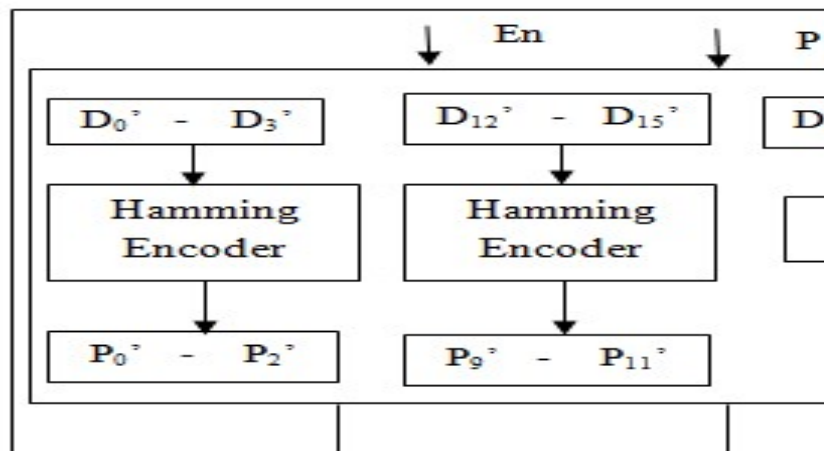


Fig. 4. Architecture of Modified DMC Decoder

**3.4 Flexible Unequal Error Control (FUEC):**

Here an extension of FUEC [40] is provided that can increase the fault correction rate of burst errors. The general structure of the code is given in below

Fig.5. which includes code bits and data bits. The code bits are just an overhead to the data bits that can be employed in the process of evaluating whether data is erroneous or not and the data bits contain actual data.

C <sub>0</sub>	...	C <sub>n-1</sub>	X <sub>0</sub>	X <sub>1</sub>	X <sub>2</sub>	X <sub>3</sub>	X <sub>4</sub>	X <sub>5</sub>	X <sub>6</sub>	X <sub>7</sub>	X <sub>8</sub>	X <sub>9</sub>	X <sub>10</sub>	X <sub>11</sub>	X <sub>12</sub>	X <sub>13</sub>	X <sub>14</sub>	X <sub>15</sub>
	..	1																

Fig 5. Structure of code word

By employing the algorithm of extended FUEC can correct single bit error, two bit adjacent error and so on upto five bit adjacent error. This needs only an 8bit code word for 16 bit word for the detection of burst error of length up to 5bits. The below

figure shows parity check H matrix for the designed code where C<sub>i</sub> represents code bits whereas X<sub>i</sub> represents data bits. The designed H-matrix consists of 10 code bits and 16 data bits is given below.

	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	X0	X1	X2
1	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0

Fig 6. H-Matrix code for proposed FUEC

The formula's that are employed to obtain code bits are given below.

- C(0)= X(0) ⊕ X(4) ⊕ X(5) ⊕ X(6) ⊕ X(7) 1
- C(1)= X(1) ⊕ X(5) ⊕ X(9) ⊕ X(10) ⊕ X(14) 2
- C(2)= X(2) ⊕ X(6) ⊕ X(8) ⊕ X(11) ⊕ X(15) 3
- C(3)= X(3) ⊕ X(7) ⊕ X(11) ⊕ X(12) 4
- C(4)= X(5) ⊕ X(10) ⊕ X(13) ⊕ X(15) 5
- C(5)= X(1) ⊕ X(6) ⊕ X(10) ⊕ X(13) 6
- C(6)= X(2) ⊕ X(7) ⊕ X(10) ⊕ X(11) ⊕ X(15) 7
- C(7)= X(3) ⊕ X(8) ⊕ X(12) ⊕ X(14) 8
- C(8)= X(4) ⊕ X(9) ⊕ X(12) ⊕ X(13) 9
- C(9)= X(4) ⊕ X(7) ⊕ X(10) ⊕ X(13) ⊕ X(15) 10

On the other hand syndrome formulae obtained from H-Matrix are given below

- S0 = C (0) ⊕ X(0) ⊕ X(4) ⊕ X(5) ⊕ X(6) ⊕ X(7) 11
- S1 = C (1) ⊕ X(1) ⊕ X(5) ⊕ X(9) ⊕ X(10) ⊕ X(14) 12
- S2 = C (2) ⊕ X(2) ⊕ X(6) ⊕ X(8) ⊕ X(11) ⊕ X(15) 13
- S3 = C (3) ⊕ X(3) ⊕ X(7) ⊕ X(11) ⊕ X(12) 14
- S4 = C (4) ⊕ X(5) ⊕ X(10) ⊕ X(13) ⊕ X(15) 15
- S5 = C (5) ⊕ X(1) ⊕ X(6) ⊕ X(10) ⊕ X(13) 16
- S6 = C (6) ⊕ X(2) ⊕ X(7) ⊕ X(10) ⊕ X(11) ⊕ X(15) 17
- S7 = C (7) ⊕ X(3) ⊕ X(8) ⊕ X(12) ⊕ X(14) 18
- S8 = C (8) ⊕ X(4) ⊕ X(9) ⊕ X(12) ⊕ X(13) 19
- S9 = C (9) ⊕ X(4) ⊕ X(7) ⊕ X(10) ⊕ X(13) ⊕ X(15) 20

#### 4. RESULTS and DISCUSSIONS

The results were summarized under two categories. The first category of results presents in detail description of error efficiency correction by considering the length of the error. The second categories of results were summarized based on redundancy incurred by different ECC's.

The table.1 below summarizes different types of error correction capabilities of different ECC's with respect to adjacent errors as well as random errors. Here the length of data word considered is of 16 and assuming 50% of the word is erroneous. Different types of errors were injected that includes single errors as well as burst

errors. The length of the burst errors is varied from 2 to 8. The types of burst errors were chosen based on fact that occurrence of burst errors length ‘8’ are less frequent than that of burst errors [41-42] of length and hence errors are injected accordingly to estimate percentage of error correction. The results presented in table.1 clearly convey that the

proposed ECC is capable of achieving very high correction rate up to five-bit adjacent error and gradually minimizes its performance for the errors of seven and eight bit adjacent errors. The analysis is shown in fig. 7. For better interpretation and understanding.

Table.1. Adjacent Error Correction Capabilities of the proposed technique

Codes	Double Bit Error	Triple Bit Error	Quadruple Bit Error	Quintuple Bit Error	Sextuple Bit Error	Septuple Bit Error	Octuple Bit Error
CLC	100	80	62	56	40	34	18
Matrix [32]	88	52	42	28	18	8	4
DMC [36]	100	56	48	18	8	2	2
MDMC [39]	100	58	50	20	6	2	2
FUEC QAEC [40]	100	100	100	6	2	0	0
Proposed	100	100	100	100	46	4	2

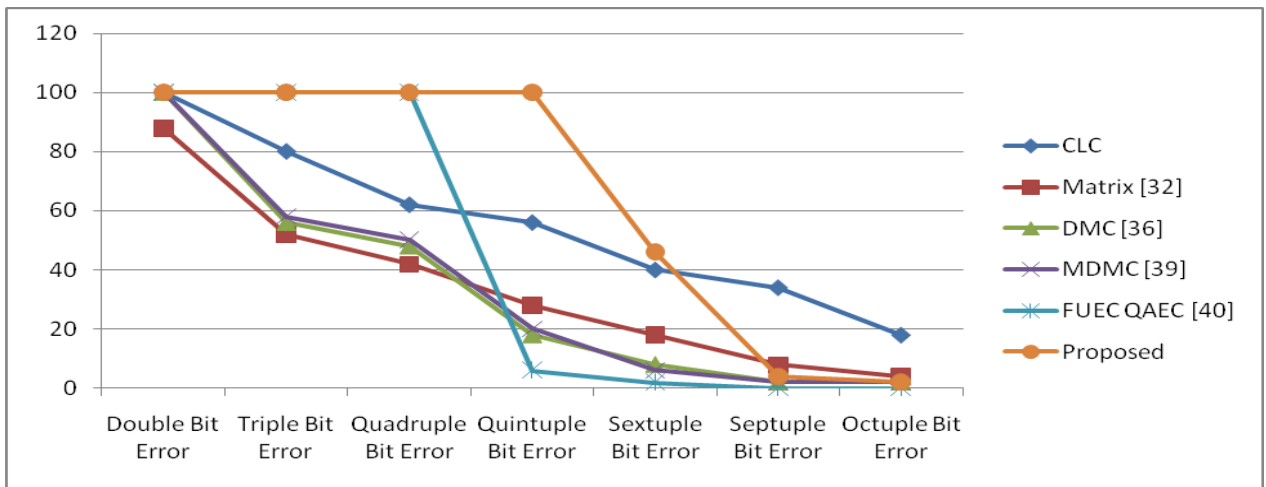


Fig 7. Adjacent Error Correction Capabilities of proposed Error Correction Code

The results presented in table.2 clearly convey fact that the proposed ECC is capable of achieving very high correction rate up to six-bit random error and gradually deteriorates its performance for the errors of seven and eight bit

random errors. The same analysis is presented in fig for better understanding. From the results of fig. and fig. it very clear that the proposed ECC’s achieves very high error correction rate for both adjacent errors as well as random errors.

Table.2. Random Error Correction Capabilities of the proposed technique

Codes	Single Bit Error	Double Bit Error	Triple Bit Error	Quadruple Bit Error	Quintuple Bit Error	Sextuple Bit Error	Septuple Bit Error	Octuple Bit Error
CLC	100	91.86	71	58	42.4	28.6	12	0
Matrix [32]	100	100	76.4	54.3	35.1	14.2	6.7	0.6

<b>DMC [36]</b>	100	100	100	100	100	92.6	84.7	76.0
<b>M-DMC [39]</b>	100	100	100	100	100	94.23	86.76	78.42
<b>FUEC-QUAEC[40]</b>	100	29	23.8	16.92	10	4	2	0
<b>Proposed</b>	100	100	100	100	100	100	80.76	68.43

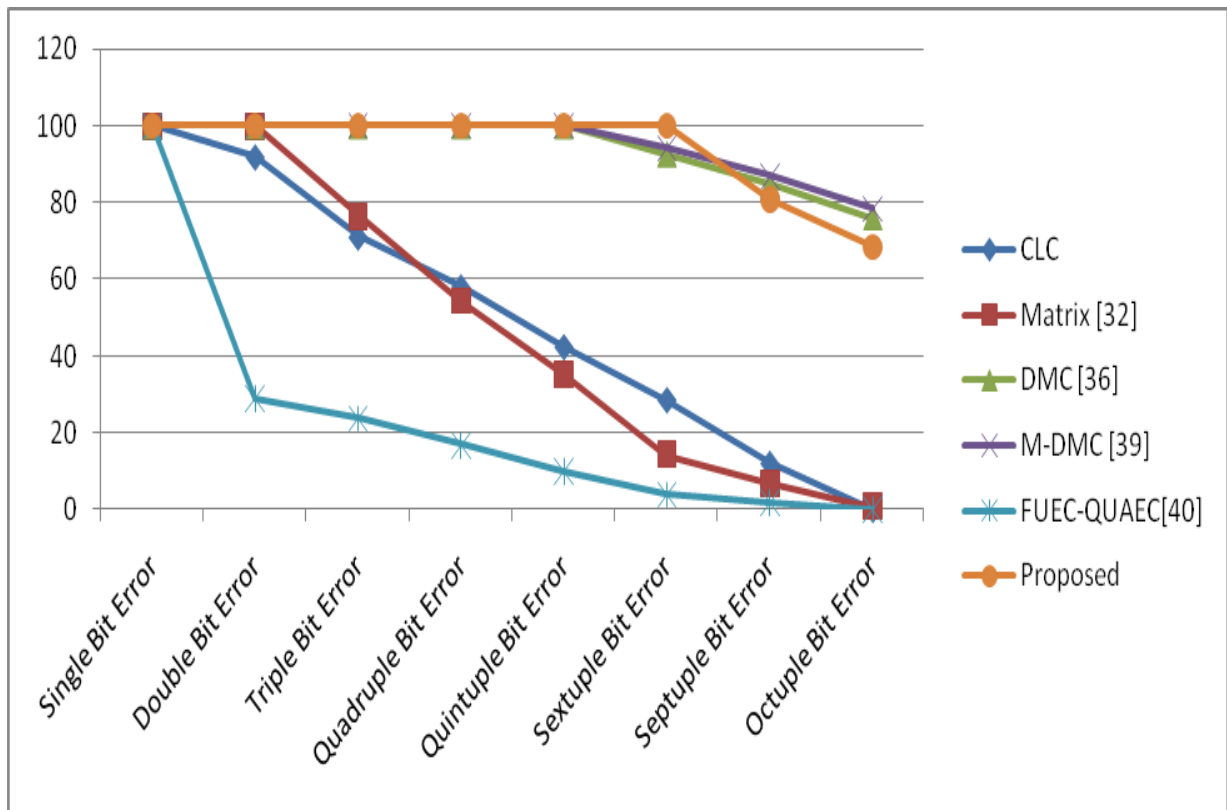


Figure 8. Random Error Correction Capabilities of proposed Error Correction Code

The comparison of redundancy bits and their percentage is given in table.3. The values presented in the table clearly shows that the proposed ECC methodology is slightly increased redundant overhead bits due to which, it has attained higher correction rate. For better

understanding, Comparison of redundancy overhead is depicted in fig.9. FUEC mechanism provides error protection for higher protection data. This is not achieved with existing LDPC (low density parity checker) codes methods [9].

Table.3. Redundancy of Various ECC's

code	Redundancy bits employed	Redundancy Percentage
MC[32]	28	46.7
DMC [36]	32	50
M-DMC [39]	28	53.33
FUEC-QUAEC[40]	9	56.25
Proposed	10	62.5

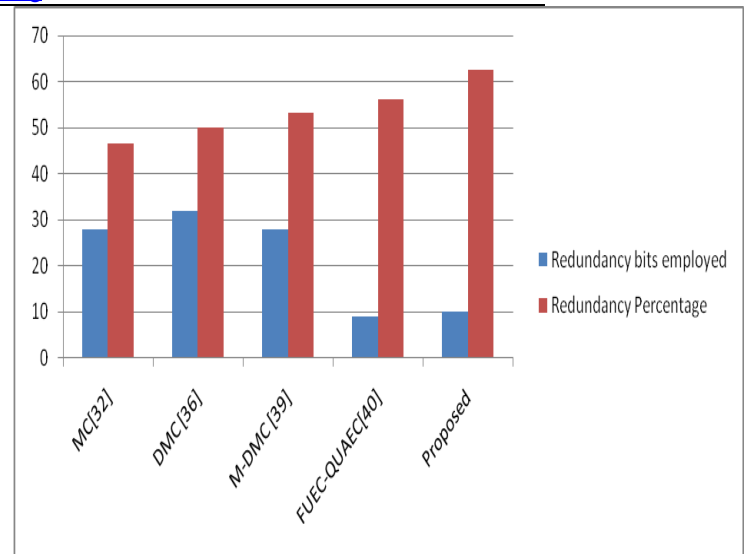


Figure 9. Redundant Bits of employed by different ECC's to achieve desired correction rate

## 5. CONCLUSIONS

The novel type of hybrid type error correction code is presented here to ensure the reliability of SRAM memories. The proposed type of error correction code is obtained by integrating the inherent properties of Modified Decimal Matrix Code and the Flexible Unequal Error Correction that can detect single bit upsets, multiple bit upsets and as well as burst errors up to length of eight bits. This can achieve 100% of error correction up to six bits and offers correction rate of 80.76 and 68.43 for burst errors of length 7 and 8 respectively. The error correction capabilities for random error is found to be 100% for Quintuple Bit Error and there after we observed slight decrement in error correction capability for Sextuple Bit Errors, Septuple Bit Errors and Octuple Bit Errors. The percentage of error correction rate for Sextuple Bit Errors, Septuple Bit Errors and Octuple Bit Errors is found to be 46, 4 and 2 respectively. However, the increased reliability of this hybrid type error correction code is achieved at a cost of slight increment in the overhead bits. The hybrid type Error Correction Code presented here proves to achieve higher error correction rate compared to all other techniques that are considered for experimental purpose and proves to be an attractive opinion for detecting single cell upsets, multiple

upsets and burst errors up to length of 8 bits in SRAM memories that are popularly employed for CAM memories and space applications. Furthermore the immunity for cell upsets can be controlled based on the application types. This also employs encoder redesign technique at receiving end that can aid for further improvements in area overhead and power consumption of encoder and decoder circuits.

Further this work can be advances with the proposed error corrector code augment with artificial intelligent techniques are imperative for both random and burst errors prediction and correction. The proposed FUEC+AI, automatically trains from run time errors. Error prediction models using deep learning methods are imperative for meticulous data interpretation and analytics. Hybrid error correction codes combining LDPC (low density parity check codes) with FUEC is also significant to improve the error correction rate for higher bit values. This study concludes the FUEC combined with MDMC is shown remarkable error handling capacity for both burst and random higher bit -errors.

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