PERFORMANCE EVALUATION OF INVERTED SINE PWM TECHNIQUE FOR AN ASYMMETRIC CASCADED MULTILEVEL INVERTER

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ABSTRACT

Multilevel inverter (MLI) is a new breed of power converter that is suited for high power applications. The various topologies of MLI are diode –clamped, capacitor clamped and cascaded H-bridge inverter[1].This paper focuses on cascaded MLI using two unequal dc sources in order to produce a seven-level output. The proposed topology reduces the number of dc sources and switching elements. Various modulation methods have been reported for the MLI in the literature [2], but this paper emphasis on unipolar inverted sine PWM (ISPWM) technique. The unipolar Inverted Sine Carrier Pulse-Width Modulation (ISCPWM) technique reduces the number of carriers and enhances the fundamental output voltage particularly at lower modulation index ranges with reduction in Total Harmonic Distortion (THD), and switching losses. The performance evaluation of the proposed PWM strategy for three-phase multilevel inverter is done using MATLAB and the optimum switching frequency with minimized total harmonic distortion and switching loss is determined. The gating signals are generated using Spartan FPGA processor as it provides better resolution. The simulation results are verified experimentally.

Keywords: *Asymmetric Multilevel inverter, Unipolar ISPWM, THD & Switching loss.*

1. INTRODUCTION

Multi-level inverters have become an effective and practical solution for increasing power and reducing harmonics of AC waveforms. By synthesizing the AC output voltage from several levels of DC voltages, staircase output waveform can be produced. This allows for higher output voltage and simultaneously lowers the stress on the semiconductor device. Among the various topologies, asymmetric cascaded MLI is employed as it requires two unequal dc sources for producing a seven-level output [3]. In addition, this topology provides low switching losses and high conversion efficiency. The modulation strategy employed in this paper is the phase disposition (PD) based unipolar inverted sine PWM (ISPWM) technique. In the conventional PD-PWM method, triangular wave is used as carrier wherein they are replaced by inverted sine carrier waves in this model. In order to produce a m-level output,generally(m-1) carriers are needed [4]. But this paper employs a PWM technique which uses only three inverted sine wave carriers for producing a seven-level output. The ISPWM technique has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM without any pulse dropping [5]. Also, there is a reduction in the total harmonic distortion (THD) and switching losses.

An inverted sine wave of high switching frequency is taken as a carrier wave and is compared with that of the reference sine wave**.** The pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave.PIC microcontroller is used to obtain the gating pattern for the individual IGBTS. The total harmonic distortion for the different values of switching frequencies is obtained and is found to

be lesser than the conventional method. The switching losses are calculated for various switching frequencies, and from the THD and switching loss values, the optimum switching frequency is obtained. The output voltage waveform which comprises of seven levels is obtained by modulating the inverted sine carriers with optimum frequency. By employing this new modulation technique it has been proved that the fundamental voltage is improved throughout the working range and is greater than the voltage obtained using conventional method which employs triangular carriers for modulation.

2. ASYMMETRIC CASCADED MULTILEVEL INVERTER

Traditionally, each phase of a cascaded multilevel inverter requires 'n' dc sources for 2n+1 levels. For many applications, it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H- bridge multilevel inverter, an asymmetric topology is proposed as shown in Fig.1.This provides the capability to produce higher voltages at higher speeds with low switching frequency. The advantages of asymmetric topology are:

- Reduced number of dc sources
- Low output switching frequency
- Low switching losses
- High conversion efficiency
- Flexibility to enhance
- Reduction in complexity and cost

A seven-level asymmetric cascaded H-bridge multilevel inverter has two H-bridges for each phase.The output voltage of the first H-bridge are denoted by V_1 and the output of the second H-bridge is denoted by V_2 so that the output voltage of the cascaded multilevel inverter is the sum of the two voltages. By opening and closing of the first bridge appropriately the output voltage V1 can be made equal to $-V_a$, 0, or $+V_a$ while the output voltage of the second bridge V_2 can be made equal to $-V_b$, 0 or $+V_b$. Therefore the output voltage of the converter is a combination of V_a and V_b that has seven possible values 0, $+V_a$, $+V_b$, $(V_a + V_b)$, $-V_a$, $-V_b$ and $(-V_a - V_b)$.The output voltage waveforms are shown in Figs. 2,3and 4.

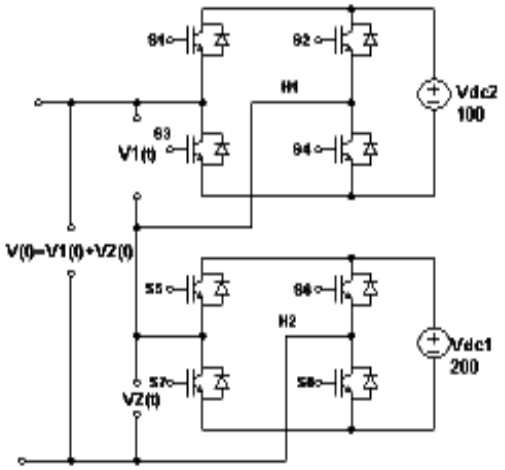

Fig.1.Cascaded MLI with unequal dc sources.

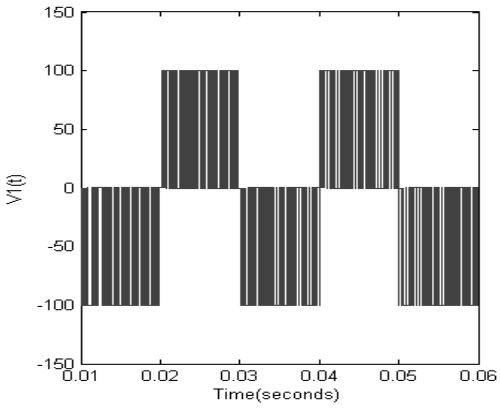

Fig 2. Output voltage of the First Bridge of MLI.

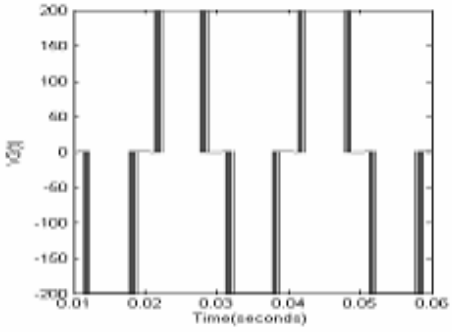

Fig 3. Output voltage of the Second bridge of MLI.

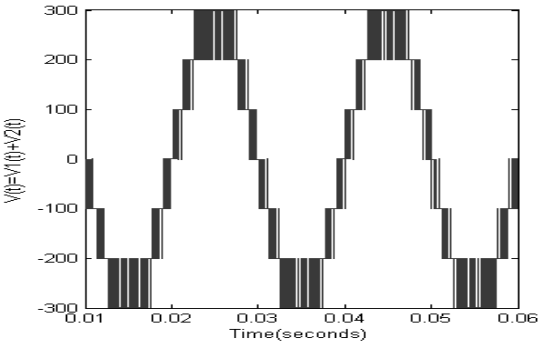

Fig.4. Output Voltage waveform of Seven-level Asymmetric MLI.

3. MODULATION STRATEGIES FOR ASYMMETRIC MLI

There are many control techniques employed for multilevel inverters [6]. However they can be classified into three main categories:

- Fundamental frequency switching
- Space vector PWM
- Sinusoidal PWM (Multicarrier PWM).

In the fundamental switching scheme, the switching angles are calculated and later they are transferred to a digital system. This technique eliminates low order harmonics in order to reduce the distortion in the output voltage. The space vector control technique can be used to obtain the optimal commutation state for the switches and due to their complexity it is implemented in a Digital Signal Processor (DSP). The implementation of this technique becomes more complex when the number of levels in the inverter is increased. This technique is obtained mainly to the diode clamped topology to solve the problems of unbalanced voltages in the dc bus.

3.1. Multicarrier PWM Technique

The multicarrier PWM method uses several triangular carrier signals, keeping only one modulating sinusoidal signal. If an 'n' level inverter is employed, 'n-1' carriers will be needed. The carriers will have the same frequency and the same peak to peak amplitude and are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency 50 Hz. At every instant each carrier is compared with the modulating signal. Each comparison gives one if the modulating signal is greater than the triangular carrier, zero otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter. Multicarrier PWM method can be categorized into 2 groups. 1) Carrier disposition methods (CD) where the reference waveform is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform amplitude, 2) Phase shifted PWM method, where the multiple carriers are phase shifted accordingly. Among these classifications, the phase disposition method is more commonly is employed in this paper as it gives least total harmonic distortion [7].

4. PROPOSED UNIPOLAR INVERTED SINE PWM FOR HYBRID MULTILEVEL INVERTER

The proposed unipolar control strategy replaces the triangular based carrier waveform by inverted sine wave. The inverted sine PWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM. The application of unipolar PWM to inverted sine carrier results in the reduction of carrier frequencies or its multiples and significant reduction in switching losses. So, the advantage of inverted sine and unipolar PWM are combined to improve the performance of the hybrid multilevel inverter. The inverted sine carrier PWM (ISCPWM) method uses the sine wave as reference signal while the carrier signal is an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. From the Fig.5. it is clear that the pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave.

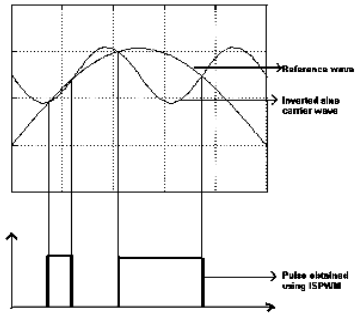

Fig .5. Generation of pulse using ISPWM

The advantages of unipolar inverted sine carrier are:

- It has a better spectral quality and a higher fundamental component compared to the conventional sinusoidal PWM (SPWM) without any pulse dropping.
- The ISCPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges.
- There is a reduction in the total harmonic distortion (THD) and switching losses.
- The appreciable improvement in the total harmonic distortion in the lower range of modulation index attracts drive applications where low speed operation is required.
- Harmonics of carrier frequencies or its multiples are not produced.

4.1. Generation of gating pulses for the proposed PWM using FPGA

To produce a seven-level output, the proposed PWM strategy uses only three carriers compared to six carriers with the conventional PWM[8].The carrier waveforms for the proposed unipolar ISPWM are shown in the Fig.6.

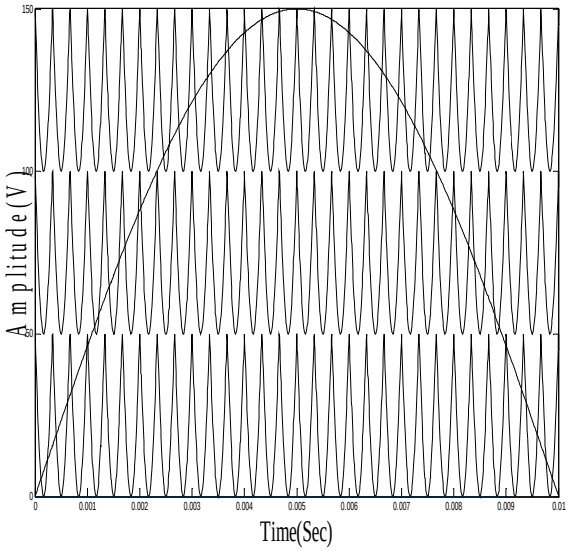

Fig.6.Carrier and Inverted Sine Waveforms for Unipolar ISPWM Technique.

The gating signals for the seven level inverter employing the ISPWM technique is generated using FPGA processor.

5. PERFORMANCE EVALUATION OF UNIPOLAR ISPWM TECHNIQUE

The performance evaluation of an inverted sine pulse width modulated three-phase multilevel inverter[9] is done using MATLAB and the optimum switching frequency with minimized total harmonic distortion and switching loss is determined. The simulation results for the phase voltage and line-line voltage is shown below:

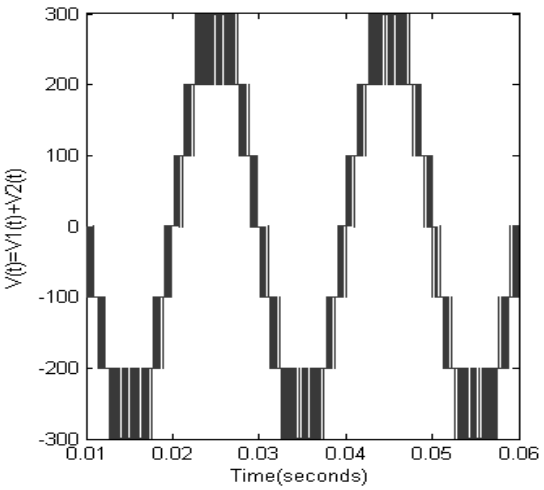

Fig.7.Phase Voltage of Asymmetric MLI

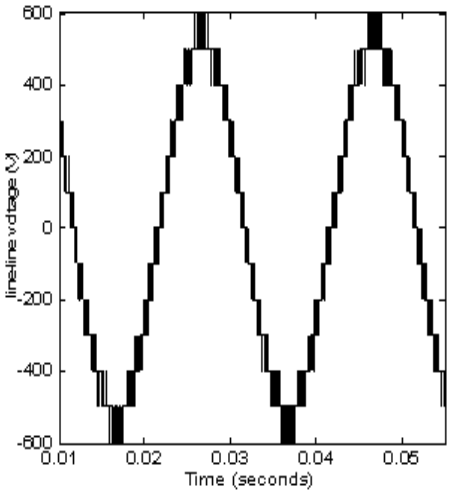

Fig.8. Line – Line Voltage of Asymmetric MLI.

The variation of total harmonic distortion (THD) and fundamental voltage with the change in the switching frequency is shown in the figure. The THD decreases with increase in switching frequency and the fundamental component of voltage increases with increase in switching frequency and is higher for inverted sine carrier compared to the conventional triangular carrier[10,11].

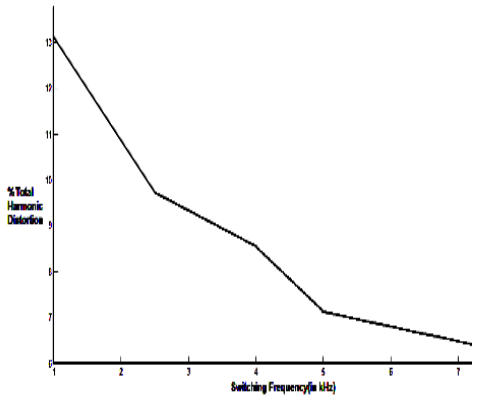

Fig.9. THD Vs. Switching Frequency

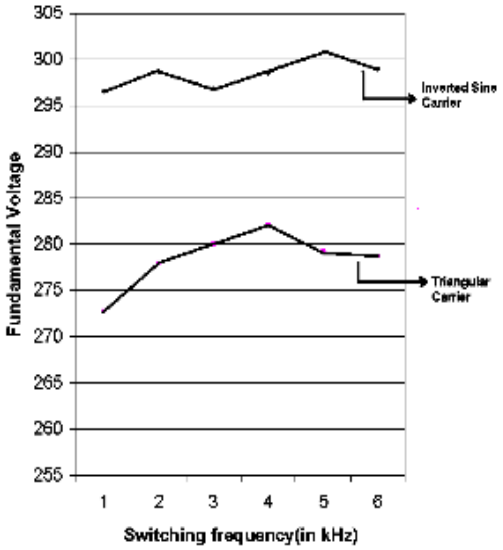

Fig.10. Fundamental voltage vs. switching frequency

5.1. Switching loss Calculation for the main switch IGBT and antiparalleldiode

The equations governing the calculation of switching loss for an IGBT and diode are given below and the switching energy is obtained from the area under the power curve [12, 16]. The equations governing the switching loss is given by

$$E_{on} = \int_{0}^{ton} P(t) \cdot dt \quad (1)$$

$$E_{off} = \int_{0}^{toff} P(t) \cdot dt \quad (2)$$

$$E_{sw} = E_{on} + E_{off} \quad (3)$$

$$E_{sw} = \frac{1}{2} V_{CE} . I_C . (t_{on} + t_{off}) \quad (4)$$

The switching loss [13] of an IGBT is calculated from the equation

$$P_{sw} = f_{sw} \cdot E_{sw} \quad (5)$$

The switching loss of the diode is calculated from the equation

$$P_{swD} = \frac{1}{2} V_D . I_D . (t_{on} + t_{off}) \cdot f_{sw} \quad (6)$$

The voltage, current, power waveforms and the variation of switching loss with frequency is shown in the following figures.

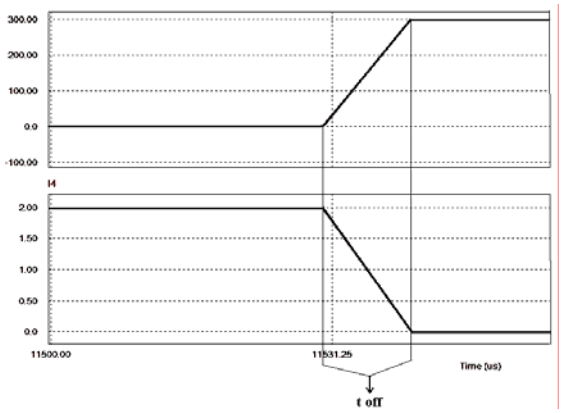

Fig.11. Determination of turn -off time

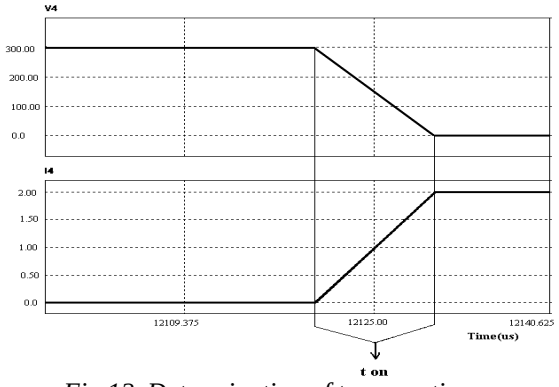

Fig.12. Determination of turn -on time

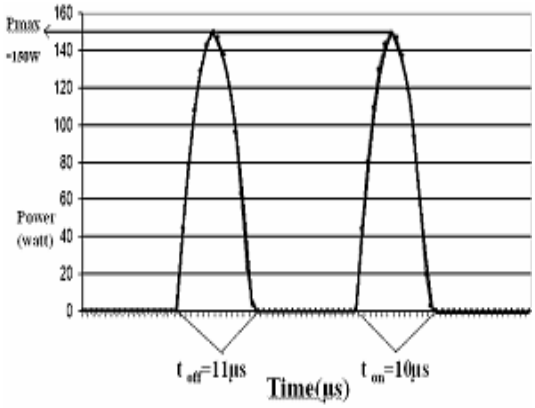

Fig.13. Power curve for IGBT

5.2. Determination of optimum frequency

- With increase in switching frequency, THD decreases and switching loss increases [14, 15].
- To obtain a low value of THD and switching loss, a graph is plotted with THD, switching loss and switching frequency.
- The optimum frequency is found to be 3950Hz and the corresponding THD and switching loss is found from the graph shown below.

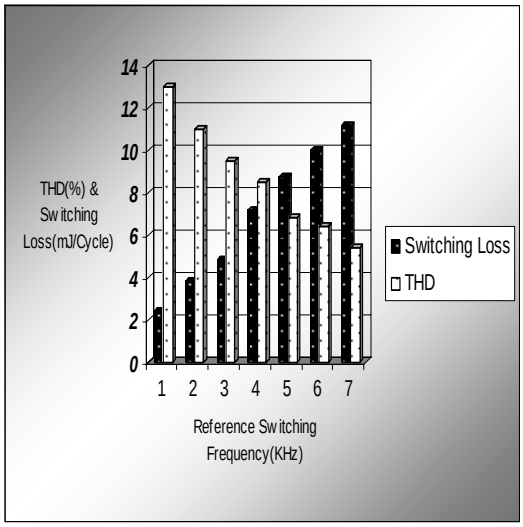

Fig.14.Determination of optimum frequency

The pulse pattern for optimum frequency to obtain the desired voltage levels by triggering the corresponding IGBTs and the pulse waveform is obtained using FPGA and is shown below:

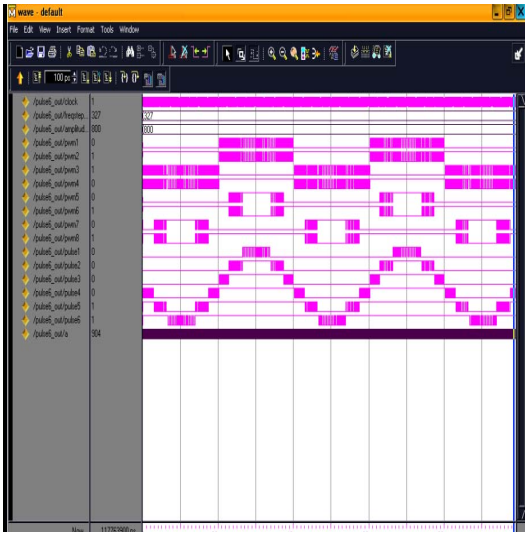

Fig.15.Gating pulse generation in Modelsim

6. EXPERIMENTAL RESULTS

To experimentally validate the asymmetric cascaded H-bridge multilevel inverter using the proposed modulation, a prototype seven - level inverter has been built using FSBB20CH60 smart power module (SMP) as the switching devices as shown in Fig.1.The SMP uses IGBT as the power device and it provides optimized circuit protection and drive matched to low loss IGBT.The gating signals are generated using Spartan FPGA processor and the output power of the inverter is about 850W.The experimental ouput waveforms of the asymmetric MLI is shown in Fig.16.

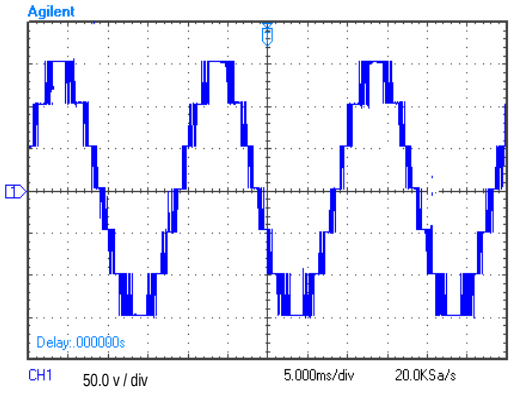

Fig.16. Line – neutral voltage for Asymmetric MLI using Unipolar ISPWM.

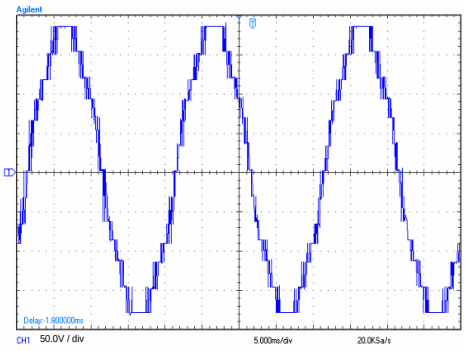

Fig.17. Line – Line voltage for Asymmetric MLI with Unipolar ISPWM.

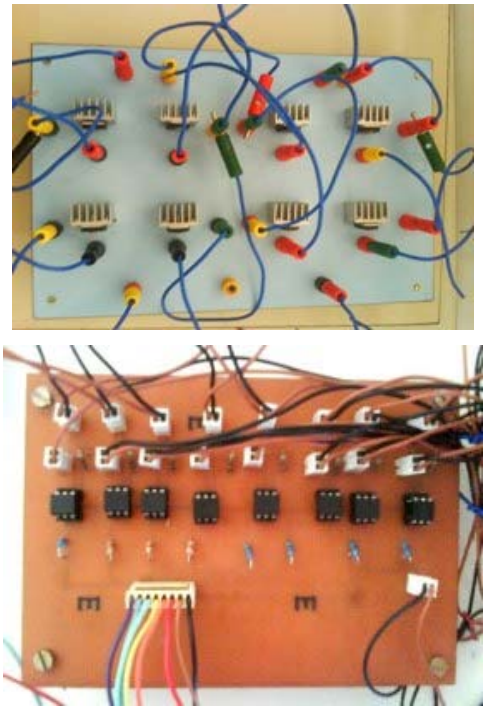

Fig.18.Hardware set-up for Single phase power circuit with optocoupler.

7. CONCLUSION

From the simulation and experimental results, several features of the proposed modulation strategy from the aspect of line voltage have been identified. The line voltage yields better spectral performance for unipolar ISPWM compared to the conventional PWM and this reduces the need for output filter. By employing this new technique it has been proved that the fundamental voltage is improved throughout the working range and is greater than the voltage obtained using conventional method which employs triangular carriers for modulation. In addition to this, switching losses and THD are also lower compared to the conventional PWM technique. This paper also employs asymmetrical DC sources which reduces the number of bridges used thus decreasing the complexity and the cost of the circuit. This can be important in the high power quality cascaded multilevel inverters which require several voltage sources and knowledge of the dc voltage levels. By increasing the number of steps, waveform approaches the desired sinusoidal shape and THD is reduced. The proposed modulation strategy of the multilevel inverter with fuel cell in place of dc sources has a greater scope in applications involving electrical vehicles.

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