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A MODIFIED CASCADED CELLS MULTILEVEL INVERTER WITH BATTERIES STATE OF CHARGE ADJUSTMENT

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ABSTRACT

Power quality enhancement is a critical factor during the design of new multilevel inverters. These topologies are generally modified in order to improve the operating of the converter. In this paper a detailed analysis of a new modified cascaded cells multilevel inverter architecture with power bank adjustment is presented. This new topology provides an enhanced power output through the combination of state of charge balancing in the power bank and the adaptation of firing angles. The present work uses an adapted genetic algorithm for determining the optimal firing angles. The equilibration method assesses the state of charge of the batteries in the power bank in order to generate a balanced discharge. This approach showed promising results related to the voltage output quality, functioning reliability and batteries life span. Each battery string in the power bank is connected to a level generation switch. The monitoring and control algorithm performs a variation of combinations of the power bank's DC storage units in order to control their discharge, while the control algorithm operates independently of the adjustment algorithm. The proposed multilevel inverter topology is first presented, then the discharge method of the power bank is analyzed under different circumstances. All tests on the batteries state of charge and voltage output generation are achieved in a simulation environment.

Keywords: *Multilevel Inverter (MLI), Cascaded Cells, Power Bank, Power Management, New MLI Architecture, SoC Balancing, Discharge Control.*

1. INTRODUCTION

The main advantage of multilevel inverters (MLI) is their strong capability of converting voltage under different ranges of loads, which makes them very suitable for different kinds of industrial applications [1-3]. However, many topologies of multilevel inverters have been introduced trough history, there are three basic architectures, the flying capacitor multilevel inverter (FCMLI), the diode clamped multilevel inverter (DCMLI) and the cascaded H-Bridge multilevel inverter (CHMLI) [4-6]. Other topologies of multilevel inverters were designed to solve issues related to high level configurations, excessive need of semiconductor switches and DC sources voltage fluctuation [7-9]. Thus, these architectures may use special combinations of switches to increase the available configurations levels simply by exploiting non symmetric switching states. Some works have even targeted the use of hybrid architectures based on elite multilevel inverter topologies such as the CHMLI in order to deal with non-equilibration issues by exploiting redundant switching states. Instead of using classic DC voltage repartition trough capacitors like the FCMLI, Multilevel inverters may use consisting DC sources out of a Power Bank [10]. The state of charge unbalancing among batteries in this case is a very common issue that results in voltage output quality degradation and the limitation of batteries life span [11-13].

Some researchers focused on conceiving power banks capable of self-adjustment, others have chosen to design procedures capable of making a balanced discharge exploitation of the batteries, used by the multilevel inverter [14-17]. However, in these works, the voltage output quality and the SoC balance among power bank units were rarely targeted simultaneously for power enhancement. This is why, in this paper a technical approach to equalize batteries state of charge (SOC) as they are exploited by the load, but also dispatch power demand along charging cycles and enhance voltage output is presented. The modified cascaded cells multilevel inverter in this paper uses the batteries directly as DC sources [18-19]. The exploitation of the power bank is managed by an equilibration algorithm while the switching angles are calculated using a genetic algorithm (GA). Many techniques of

batteries performance optimization were introduced in literature like rapid charging adaptation, variable current control and prediction systems [20]. However, the present study is limited to managing the power share among batteries, exploited by a new multilevel inverter topology by routing the available potential to the less charged units. The control strategy used in this study sets adaptive thresholds to choose automatically the best power routing method based on the load and the charging source state. The functioning of the system is simulated using a 9 levels inverter model.

2. MLIS ARCHITECTURES REVIEW AND COMPARISON

2.1 Classic architectures basic study

There are generally 3 basic architectures of multilevel inverters; the flying capacitors multilevel inverter (FCMLI), the diode clamped multilevel inverter (DCMLI) and the cascaded H-bridge multilevel inverter (CHMLI), figure 1 illustrates the basic architectures in 5 levels mode.

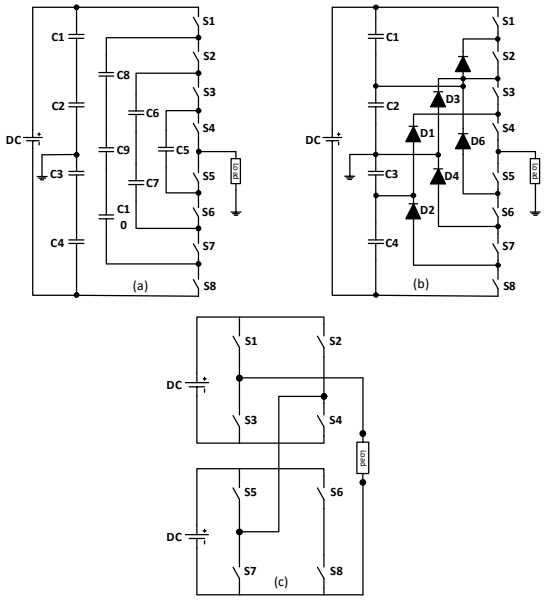

Figure 1: Basic MLI architecture (a) FCMLI, (b) DCMLI, (c) CHMLI

The multilevel voltage output of the FCMLI is produced using different combination of capacitors. This structure requires the pre-charge of capacitors which causes a complex boot and a voltage imbalance in the entry capacitors (the flying capacitors). In order to maintain a proper operating, the FCMLI have to regulate the flying capacitors at their basic values. Authors have dealt with these issues by proposing spontaneous balancing under determined conditions. Ghias et al have proposed a technique based on the use of redundant switching states, taking at consideration the output current direction [21]. Shukla et al have proposed in the same context a different approach that uses the switching states in a more efficient manner [22]. The diode clamped multilevel inverter uses interlocking diodes to synthesize a semi-sine wave voltage output. The voltage inputs can be either capacitors or direct batteries links inside the power bank. In this topology, higher level configurations helps reducing stress on switches and maximum voltage clamped by diodes. Many research studies have reported numerous issues related to DC voltage balancing among voltage entries. Qingquan et al addressed this limitation in the DCMLI by altering the architecture. Thus, the proposed topology uses a reduced number of components and exploits three additional switches to increase the number of possible levels in order to balance voltages trough redundant switching states [23]. Marchesoni et al propose a practical approach for balancing DC-Link voltages, this is done by exploiting the minimum-energy property of a Capacitors based power bank [24].

The cascaded H-bridge multilevel uses cascaded full bridge cells. Each cell generates a fixed number of switching states. By combining the different states, the CHMLI generates a multilevel output. This topology doesn't require the use of interlocking diodes. The CHMLI is very flexible and can be used as a converter for high as well as medium voltage applications, the command pattern required for higher level configurations is easily deduced from lower ones and doesn't require any special modifications. Despite the great performance of this topology, noticeable issues related to voltage balancing have been mentioned in different works [25-28]. Oleg et al proposed a voltage balancing method for capacitors sources case by adopting an initial charge of the power cells while maintaining the voltage values of the capacitors at the same DC voltage reference [29]. Other research studies targeted the equilibration of storage units within the power bank; Ricco et al focused on balancing the batteries (SOC) using the nearest level control and sorting methods. Other approaches focused simply on equalizing all the batteries state of charge [30].

The proposed architecture in this paper is a modified cascaded cells multilevel inverter. This topology adopts a reduced number of components and a simple command pattern. The firing angles are determined based on a genetic optimization algorithm. The SoC balancing control algorithm equilibrates the state of charge while regulating the

voltage of each level to the reference value depending on power appliance [20].

2.2 Power Bank equalization in cascaded cells multilevel inverter

Due to its remarkable performance and scalability among classic multilevel inverters, the cascaded H-bridge multilevel inverter attracted a lot of attention to overcome some of its few disadvantages. Voltage imbalance among DC cells is a major drawback in cascaded cells multilevel inverter, especially in high power and high voltage application. Imbalance in DC voltage inputs causes considerable stress on semiconductor devices, shorten the lifespan of DC storage units and may even cause serious problem during power exploitation. This issue has been dealt with differently depending on the application and the DC voltage storage units' nature. J. Amini et al proposed a balancing method based on switching control; the strategy tends to balance DC links voltage by choosing the most appropriate switching state, thus activating the right switching pairs. The proposed method is designed to be applied to the cascaded cells multilevel inverter regardless of level configuration [31]. Z. Ling et al proposed a state of charge balancing control in a 2MW/10kV battery energy storage system (BESS). Authors, in this work introduce a power control strategy involving power control, phase-phase SOC balancing and inter phase SOC balancing [32]. Following the same approach, L. Mathe et al propose a balancing method in the case of battery packs [30]. This method uses the nearest level control (NLC), authors assume that it reduces considerably the number of switching states and SoC equalization time. This method is most helpful in cases where batteries stacks are used and equalization time is a critical factor. In the case of Capacitors cells, O. V. Nos et al introduce a method where the power cells capacitors are charged with a DC voltage reference, the control technique then fixes a threshold and maintains the DC-link voltage at the fixed voltage reference [29].

Dealing with cells breakdown and sudden unavailability is a major research goal in multilevel inverters, DC inputs voltage structures and (SOC) balancing. Following this objective, O. V. Nos et al use a control strategy based on the neutral shift method to ensure a line-to-line voltage balance even when one or more cells are damaged [33]. J.H. Lee et al propose a fault detection method and a tolerance deviation control in the case of cascaded cells multilevel inverters in order to increase the reliability of the multilevel inverter [34].

The proposed multilevel inverter in this paper is mainly inspired from the cascaded cells multilevel inverter and reduces considerably the number of semiconductor devices needed [20]. This multilevel architecture answers the need to conceive a balancing technique capable of achieving a fast and reliable DC voltage equalization regardless of the level configuration. However, it was not discussed in this paper, the presented topology can be used to overcome the complete loss of a limited number of dc cells.

2.3 Power Bank unbalance in hybrid multilevel inverter architectures

In recent years, many hybrids multilevel inverter topologies have been introduced, each serving a well specified goal. These topologies were basically derived from the classic architectures mentioned previously. The designed topologies aim essentially to reduce the number of components, give an alternative to augment the number of achievable levels using less sources and producing power with minimal distortion.

Babaei et al proposed a hybrid multilevel inverter architecture that they named Developed Cascaded Multilevel Inverter [35]. This topology offers indeed a higher voltage generation and can operate at higher levels with less switching components. The presented topology, however, doesn't maintain an equilibrated stress on the DC voltage sources and uses the voltage difference between sources to create more levels at the output. For a two different DC power banks, each containing three different DC sources, the multilevel inverter is capable of generating 15 levels. However, this multi-level availability is based on a regular voltage difference between DC storage units in the power bank, any difference in exploitation can greatly affect output voltage quality and reduce the efficiency of the converter. As a consequence, the DC sources not configured to be equally exploited which would eventually reduce their lifespan.

Kangarlu et al in [36] propose a new multilevel inverter topology that they named Cascaded Sub-Multilevel Inverter. The main goal behind this architecture is to generate a high-level configuration using a minimal number of switching components. For instance, this topology is capable of generating 13 levels from 6 DC voltage sources.

In contrast with this highly appreciated quality, authors didn't pay attention to the equalization among DC voltage units, thus the first activated source will be withstanding the higher usage rate. This issue can cause a fast deterioration of the most activated units and therefore damage their integrity within a short time of their use.

Lezana et al presented in [37] a hybrid multilevel inverter topology based on the combination of the cascaded H-Bridge multilevel inverter and the flying capacitor multilevel inverter. This architecture exploits preliminary the voltage difference between DC voltage sources. As a result, the voltage of each cell is the main voltage level at the output. The cascaded H-Bridge multilevel inverter reverses the polarity after each half cycle. Conversely, the proposed architecture is incapable of maintaining the voltage balance during exploitation.

The power bank balancing is a critical feature during the design process of a high-performance multilevel inverter. This technical requirement becomes more essential when the targeted level is higher. In addition, the balancing guarantees high quality voltage and avoid losing certain levels after a deep discharge of a dc voltage storage unit. The majority of the proposed multilevel inverters aim to produce higher levels using limited number of switching components. However, authors overlook the necessity of taking at consideration the SoC equilibration of the DC voltage components during the design of the architecture. Therefore, many studies and research work propose adapted management algorithms to overcome the equilibration drawbacks [10], [38-40].

3. MODEL DESCRIPTION

3.1 The 9 levels inverter principle

The proposed multilevel inverter's main purpose is to offer a better voltage output quality, through the optimal choice of the switching angles and the limited use of switching components. To begin with, the main objectives during the architecture design were to establish a performant multilevel inverter, capable of generating a staircase wave form using a limited number of semiconductor devices. Afterwards, a set of control strategies have been added to determine the optimal firing angles in real time and manage the DC storage units to avoid any disturbance on the inputs side. By combining different ranges of DC voltage levels on the entry, a staircase sinusoidal voltage output is created. To validate the work in this study, a 9 levels inverter is used as a model. Figure 2 presents the inverter topology principle in 9 levels configuration.

DC1, DC2, DC3 and DC4 are the main DC outputs of storage units in the power bank. This study is conducted regardless of the storage unit's type; this might be lead acid batteries, capacitors or super-capacitors. The DC storage units are directly connected to the "S" switches depending on the targeted level. The number of components to be employed in any configuration of the new topology is determined using relations (1) and (2):

$$L = 2N_{sw} - 7 \quad (1)$$

$$N_d = \frac{L-1}{2} \quad (2)$$

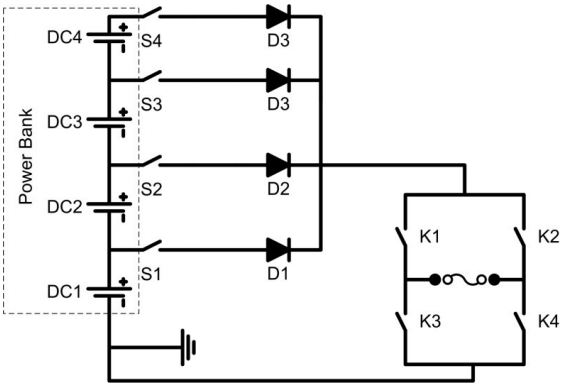

Figure 2: Simplified topology of the 9 levels new multilevel inverter

Where L is the level, N_{sw} is the number of all present switches in the diagram and N_d is the number of diodes. In this topology the "S" switches are the units producing the staircase waveform while the "K" switches invert the signal at the end of each half-cycle.

The output voltage can be expressed using relation (3):

$$V_{out}(t) = \sum_{i=1}^{n} S_i V_{DC_i} \; S_i \epsilon \{0,1\} \quad (3)$$

Where S_i is the state of the switch, it equals 1 when the switch is closed and vice versa. Figure 3 presents the command pattern applied to the studied model.

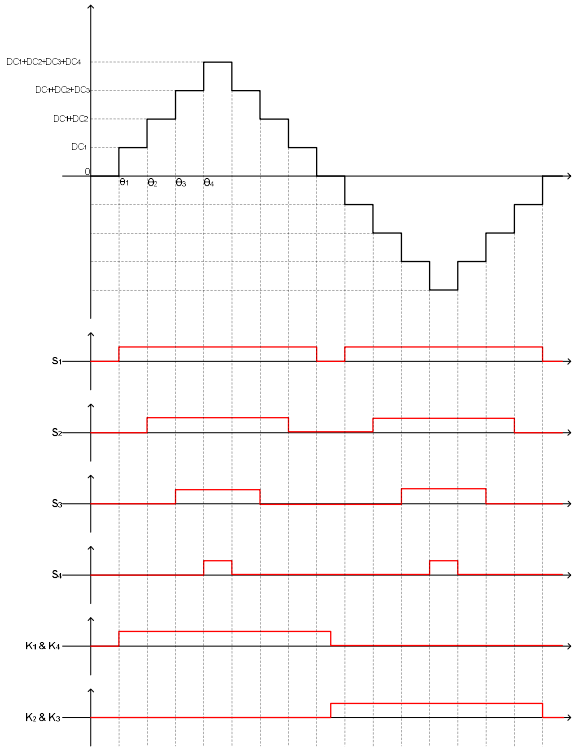

Figure 3: Command pattern applied to the multilevel inverter.

3.2 Power Bank management using a genetic algorithm-based optimization

The voltage of DC storage units inside the power bank may be written as a group of voltage values:

$$V_{PB} = \{v_1, v_2, \dots, v_n\} \quad (4)$$

Where v_1, v_2, …,v_n are the different voltages of the DC storage units, typically batteries in the power bank. For an m level inverter, at least m batty strings would be used, which means that the power bank should contain at least n batteries in a way that $n \geq m$. Technically the batteries may not have the same voltage in the power bank even before the start of the charge/discharge cycles. From the simplified topology presentation in figure 2 and the command pattern represented in figure 3, it can be seen that the most charged batteries should be activated at the first level, then the second most charged battery and so on. This function should be executed continually and simultaneously with the genetic algorithm for the switching angles optimization. Assuming that the voltage of the batteries in real time can be arranged in descending order as follows:

$$v_{1t} \geq v_{2t} \geq \cdots \geq v_{nt} \quad (5)$$

This means that in real time, v_{1t} is the voltage of the most charged battery then v_{2t}, and so on. The Fourier series expansion of the output voltage can accordingly be written as follows:

$$V(wt) = \frac{a_0}{2} + \sum_{k=1}^{\infty} (a_k coskwt + b_k sinkwt) \quad (6)$$

The output voltage of the multilevel inverter is quarter symmetric, constant a_0 and a_k $(k\epsilon\mathbb{N}^*)$ are all equal to 0. The constant b_k can be written as follows:

$$b_k = \frac{4}{k\pi}(v_{1t}cosk\theta_1 + v_{2t}cosk\theta_2 + \cdots + v_{nt}cosk\theta_n) \quad (7)$$

The multilevel inverter subject to this study possesses 9 levels, in this case 4 battery strings in the power bank should be constantly made available as DC inputs. The batteries should also be arranged from high to low voltages as follows:

$$v_{1t} \geq v_{2t} \geq v_{3t} \geq v_{4t} \quad (8)$$

b_k can be written as follows:

$$b_k = \frac{4}{k\pi}(v_{1t}cosk\theta_1 + v_{2t}cosk\theta_2 + v_{3t}cosk\theta_3 + v_{4t}cosk\theta_4) \quad (9)$$

Global expression of the output voltage of the studies multilevel inverter can be written:

$$V(\theta) = \sum_{k=1,3,5}^{\infty} \frac{4}{k\pi}(v_{1t}cosk\theta_1 + v_{2t}cosk\theta_2 + v_{3t}cosk\theta_3 + v_{4t}cosk\theta_4)sink\theta \quad (10)$$

In the power bank, the battery with the highest voltage v_{1t} will be triggered at the switching angle θ_1 because this battery is activated the most. The battery with the second highest voltage will be triggered at the switching angle θ_2, and so on until reaching the battery with the lowest voltage. The algorithm managing the power bank can also be adapted to take at consideration a number of batteries higher than the minimum needed. This configuration would allow the inverter to use the

most charged selection of units and switch to a more charged set when it's available. However, it was not dealt with, in this work, the algorithm can also reduce automatically the number of levels on the output when it's not technically possible to use any sets for actual level configuration, this feature however is not yet investigated and was not subject of this study. Figure 3 presents the bloc diagram of the multilevel inverter with switches control and batteries balancing controller.

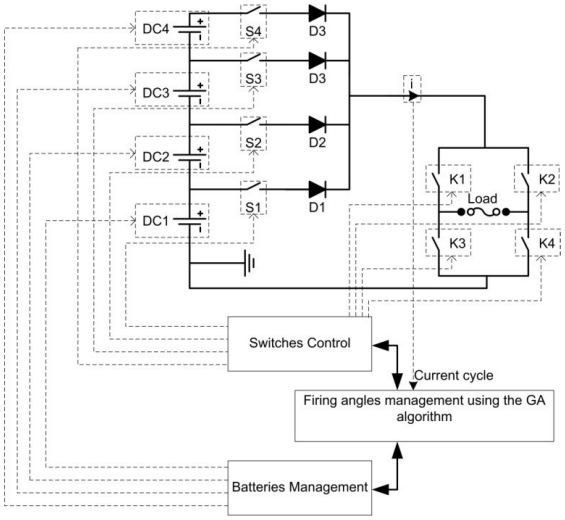

Figure 4: Operations management and signals monitoring in new MLI

through the optimal choice of the switching angles and the limited use of switching components. To begin with, the main objectives during the architecture design were to establish a performant multilevel inverter, capable of generating a staircase wave form using a limited number of semiconductor devices. Afterwards, different control strategies have been added to determine the optimal firing angles in real time and manage the DC storage units to avoid any disturbance on the inputs side. By combining different ranges of DC voltage levels on the entry, a staircase sinusoidal voltage output is created. To validate the work in this study, a 9 levels inverter is used as a model. Figure 2 presents the new multilevel inverter topology principle in 9 levels configuration.

The power bank balancing is a critical feature during the design process of a high-performance multilevel inverter. This technical requirement becomes more essential as the generated level is higher. In addition, the equilibration guarantees high quality voltage and avoid losing certain levels after a deep discharge of a dc storage unit. The majority of the proposed multilevel inverters aim to produce higher levels using limited number of switching components. However, authors neglect the necessity of taking at consideration the SOC balancing of the DC voltage components during the design of the architecture. Therefore, many studies and research work propose adapted management algorithms and balancing techniques in order to overcome the equilibration drawbacks [10], [38-40].

4. SYSTEM SIMULATION AND RESULTS

4.1 The proposed multilevel inverter simulation

The expression (10) of the output voltage using Fourier series gives the expression of harmonic content, which is reduced using the GA optimization. Finding the appropriate switching angles on the first quarter of the output voltage is sufficient to determine all switching angles, because the signal is quarter symmetric. The adopted 9 levels MLI uses 4 batteries sources, which suggest finding constantly four switching angles such as:

$$\theta_1 < \theta_2 < \theta_3 < \theta_4 < \frac{\pi}{2} \tag{11}$$

The nth harmonic is written:

$$H(n) = \frac{4}{n\pi}(v_{1t}cosn\theta_1 + v_{2t}cosn\theta_2 + v_{3t}cosn\theta_3 + v_{4t}cosn\theta_4) \tag{12}$$

The voltages of the batteries are not equilibrated thus their state of charges should be optimized simultaneously along with the switching angles during their real time update. The present approach minimizes the 3rd, 5th and 7th harmonics while equilibrating v_{1t}, v_{2t}, v_{3t} and v_{4t}.

$$\begin{cases} \frac{4}{\pi}(v_{1t}cos\theta_1 + v_{2t}cos\theta_2 + v_{3t}cos\theta_3 + v_{4t}cos\theta_4) = V_0 \\ (v_{1t}cos3\theta_1 + v_{2t}cos3\theta_2 + v_{3t}cos3\theta_3 + v_{4t}cos3\theta_4) = 0 \\ (v_{1t}cos5\theta_1 + v_{2t}cos5\theta_2 + v_{3t}cos5\theta_3 + v_{4t}cos5\theta_4) = 0 \\ (v_{1t}cos7\theta_1 + v_{2t}cos7\theta_2 + v_{3t}cos7\theta_3 + v_{4t}cos7\theta_4) = 0 \end{cases} \tag{13}$$

Figure 5 presents the global flowchart of the optimization procedure including the genetic algorithm optimization and batteries state of charge balancing. As described in the flowchart, both the optimization of the switching angles and storage balancing are simultaneously processed.

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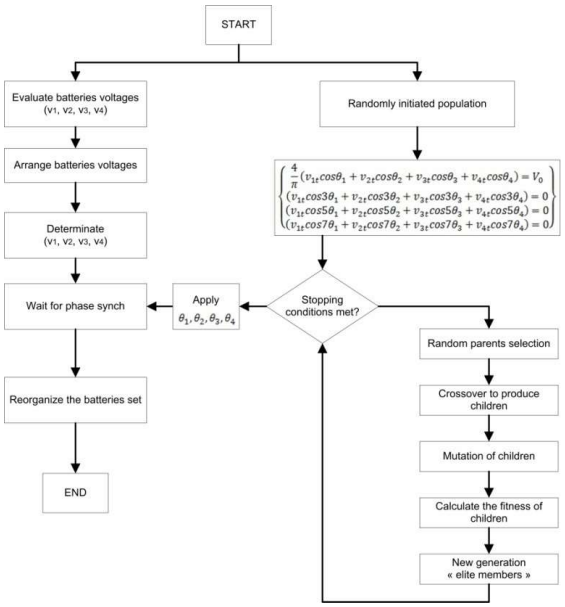

Figure 5 Flowchart of the optimization procedure with power Bank balancing.

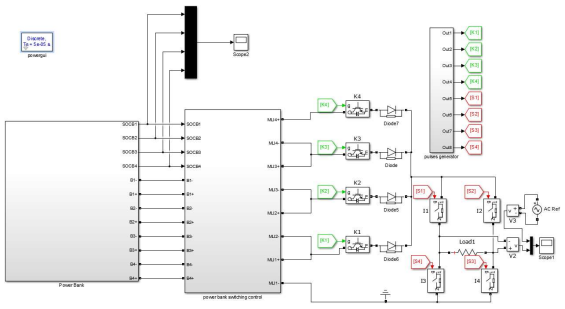

Figure 6 Model of the 9 levels MLI with Power Bank management.

The algorithm starts by randomly choosing a population of switching angles and voltage reference for the case study. At the same time the controller evaluates the batteries voltages within the power bank. Figure 6 presents the Matlab model used to simulate the 9 levels MLI adopting power bank management. The power bank on the left in figure 6 contains the batteries, while the controller in the middle arranges the batteries exploitation by interchanging the units according to the state of charge in real time.

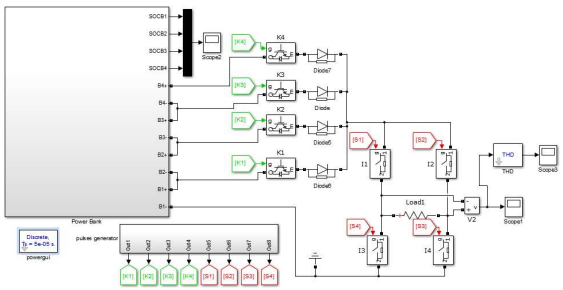

Figure 7: Model of the 9 levels MLI without Power Bank management.

The power bank balancing is a critical factor during the design process of a high-performance multilevel inverter. This technical requirement becomes more essential as the generated level is higher. In addition, the balancing guarantees high quality voltage and avoid losing certain levels after a deep discharge of a dc voltage storage unit. The majority of the proposed multilevel inverters aim to produce higher levels using limited number of switching components. However, authors overlook the necessity of taking at consideration the SOC balancing of the DC voltage components during the design of the architecture. Therefore, many studies and research work propose adapted management algorithms and balancing techniques in order overcome the equilibration drawbacks [10], [38-40].

4.2 Simulation results and analysis

In order to assess the full impact of the multilevel inverter on the batteries we connected the power bank directly to the input switches. The batteries were initially fully charged, and have following characteristics:

- Nominal voltage: 12V.
- Rated Capacity: 7Ah.
- Initial state of charge (SOC): 100%.

Figure 7 presents the voltage matlab simulink model used to simulate the functioning of the system without power bank balancing and control.

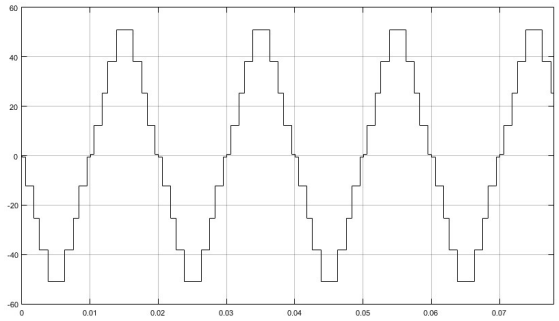

Figure 8: Voltage output of the proposed multilevel inverter at the beginning of the simulation.

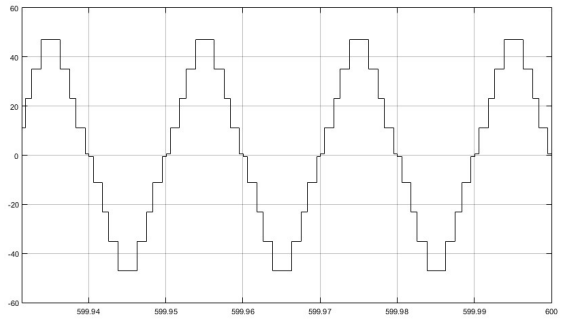

Figure 9: Voltage output of the new multilevel inverter after 10 min simulation.

In the model represented on figure 7, there is no switching control; therefore, the batteries are exploited randomly without any equilibration approach. Figure 8 presents the voltage output of the multilevel inverter at the beginning of the simulation and figure 8 presents the same voltage output after 10min of simulation time. From the comparison of figure 8 and 9 it can be seen that the first level decreases continually, due to the over exploitation of the battery activated at this level. To put things differently, in any type of multi-DC sources architecture, each level is generally drawn from the same DC source continually and without any special measures. This type of setups doesn't take into consideration the battery's state of health and preservation of its life span. Besides, the voltage levels inequalities in the output always results in high THD content. That's why, the proposed architecture ensures, both, levels equivalence in the output and controlled firing angle for the best possible waveform. The state of charge of each battery was carefully monitored using a proper simulation approach. In the 9 levels case, 4 batterie sections have been used, the state of charge timely evolution of each one before applying any type of balancing is presented on figure 10.

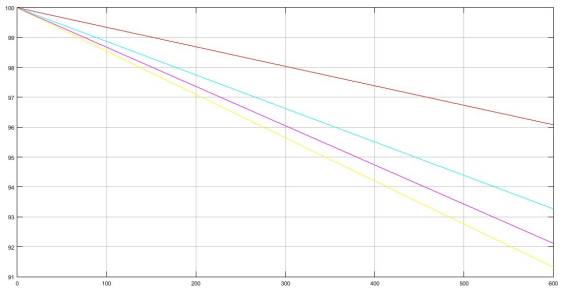

Figure 10: State of charge evolution of each battery section in the power bank.

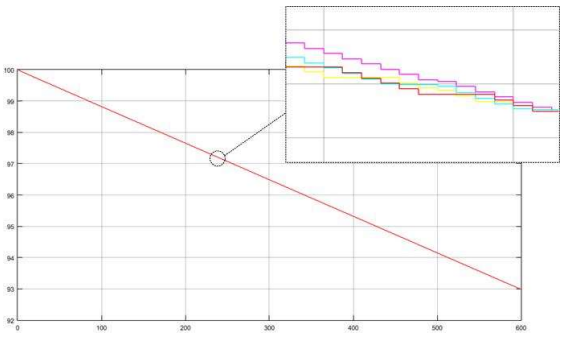

Figure 11: state of charge evolution battery sections in the power bank after applying the balancing algorithm.

The balancing algorithm helps keeping the batteries evenly charged by power routing technique when the switching angles are activated, or by using any extra available DC storage units in the power bank. In fact, this technique can be useful in both charging and discharging modes. Moreover, it can even help Power bank's management algorithms to minimize shifting operations. However, in charging mode, it should be mentioned that the technique is mostly efficient when extra chargeable batteries are present. Figure 11 illustrates the timely evolution of the batteries state of charge after applying the balancing algorithm. This approach guaranties the SoC equilibration of all the Power Bank's DC storage units. It can also be appreciated that the use of such topology minimizes the requirement of semiconductor devices while performing a better voltage output. Figure 11 clearly shows that the batteries SOC were kept evenly charged during exploitation, using the state of charge equilibrating algorithm.

5. CONCLUSION

In this article, a new multilevel inverter topology with batteries state of charge balancing was

presented, in order to overcome the SOC unbalance in classic power bank architectures, while performing the best voltage output performance in a newly developed multilevel inverter architecture. The switching angles of the multilevel inverter are determined using a genetic algorithm. An equilibration control strategy implemented in the power bank manages the batteries by routing power from the most charged units to the less charged ones. The management algorithm, also, coordinate between the activation of the switching angles, the exploitable battery sections and the available configurations of the batteries. The simulations and analysis performed in this work proved that this method helps keeping the power bank storage units equalized and optimizes the exploitation of the DC sources. Furthermore, this management strategy preserves batteries state of health and increases the batteries life span by distributing the stress equally between the power bank units. The study showed that, using this method, the output power quality is enhanced and the THD content is reduced. The present management approach, can of course, be compared to other works in terms reliability and simplicity of integration and can even be analyzed for a fault tolerant upgrade. We intend, in our future work, to analyze how far can we exploit this architecture, by developing a fault tolerant power bank, using the same MLI architecture. Any new development in the topology will be analyzed in real time.

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