DESIGN OF ACCUMULATOR DUMP FOR RFID READERS USING 0.35 µM CMOS TECHNOLOGY

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ABSTRACT

This research aims to design a dump accumulator being capable of producing bit values in parallel from the sigma-delta ADC output signal that is serial in the reader of the Radio Frequency Identification (RFID) system. RFID system consists of two parts, namely a tag and a reader. The tag uses the delta-sigma ADC to convert the input signals from the sensor which, then, become the digital serial data that are transmitted to the reader. The reader uses the dump accumulator method to convert digital bits serially into 8-bit parallel resolution. The accumulator dump uses the counter and register latch circuits as output parallel bits. The results are divided into 3 time- periods, namely period 1 (T0) during the initialization and the synchronization, period 2 (T1) shows 8-bit binary data equivalent to $127_{(10)}$, and period 3 (T2) shows 8-bit binary data equivalent to $128_{(10)}$. By using 0.35 µm CMOS technology, the number of transistor hardware resources needed is 1022 transistors with a power dissipation of 28.5 mW. These results can save 77.42% using fewer transistors and are more efficient than the comb decimator method. This method contributes and enriches knowledge on the development of on-chip systems with serial to parallel signal processing for RFID devices.

1) *Keywords: ADC Delta-Sigma, Dump Accumulator, Efficiency, RFID, serial to parallel*

1. INTRODUCTION

RFID (Radio Frequency Identification) is a process to identify an object using radio waves. RFID which is used as a sensor in the industrial field is still not widely used in Indonesia [20].

RFID works by using wireless radio frequency having a greater distance when compared to a barcode. It makes RFD possible to read automatically and quickly. Besides,

RFID is capable of making changes to data which have been stored (system reset) at any time. As it works by radio waves, reading does not need a line of sight as that in the barcode. Readings can also penetrate obstacles, such as paper, glass, books, and other non-metallic materials.[19].

In the process of retrieving data, an object is closely related to an identification [19]. Auto-ID or Automatic Identification is one of the identification methods which are considered the most profitable because the identification of the objects automatically uses the method of data retrieval without any human involvement. The Auto-ID working automatically can reduce any errors in entering the data and increasing efficiency because it does not require any human resources to operate, so the human labor readily available can be focused on the other fields. Barcodes, smart cards, voice recognition, biometric identification such as retina scan, Optical Character Recognition (OCR) and RFID are the kinds of technology using the auto-ID method.

The identifying process is done by RFID which consists of an RFID reader and RFID transponders (RFID tags) [21]. RFID tags are placed near a substance or an object to be identified.   Each RFID tag has a unique identification data (ID) number that differs from one another, so there are no RFID tags having the same ID number [21].
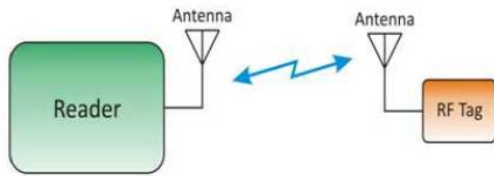
Figure 1: RFID system, consisting of Reader and Tag

In figure 1, The RFID tags can physically be paper or plastic of various sizes or it can be in the form of stickers. Inside each of these RFID tags there are a chip being capable of storing the ID number and a certain amount of information needed, and an antenna to transmit information or data to the Reader.

The antenna functions to transmit the radio wave frequency signals between the RFID reader and the RFID tag. Meanwhile, in the RFID tags and the RFID readers there are each its own internal antenna because RFID tags and RFID readers are transceivers (transmitters) which can send and receive data or information to each other.

The RFID reader will read the ID number and other information stored by the RFID tag[31], [32]. In order that RFID tags can be read by RFID, the RFID reader must be compatible with RFID tags. The process of moving data or information will occur when a tag is brought close to a reader or vice versa, and this is known as a coupling process. The difference in frequency used by the active RFID tags and the passive RFID tags causes differences in the method of transferring data or information used on the two tags. Transferring data or information on the active RFID tags using a backscatter coupling method, whereas the passive RFID tags use a magnetic (inductive) coupling method. The Inductive coupling method occurs at low frequencies [23].

When the radio wave field of the reader is adjacent to the passive tag, the antenna coil contained in this passive tag will form a magnetic field. This magnetic field will induce an electrical voltage which supplies power to the passive tag. At the same time there will be a voltage dropping on the tag load which will be read by the reader. This change in voltage drop applies as a modulation amplitude for the data bits. Clearer exposure to inductive coupling [24] can be seen in Figure 2.
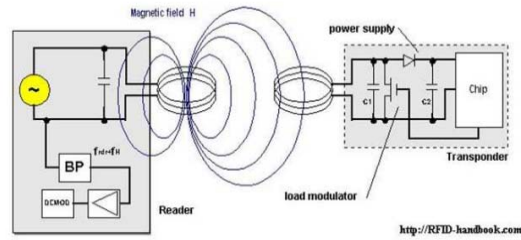

Figure 2: Inductive Coupling

A Backscatter coupling method occurs at high frequencies. The Radio frequency signals emitted by the reader (P1) will be received by the tag in a small portion [25,26].

This radio frequency signal will trigger a voltage that will be used by the tag to activate or deactivate the load to create the modulation of the data signal or the information signal. The reflected wave emitted by the tag is modulated with a data carrier wave (P2). So that the modulated waves can be captured by the reader. The illustrations for the backscatter coupling method can be seen in Figure 3.
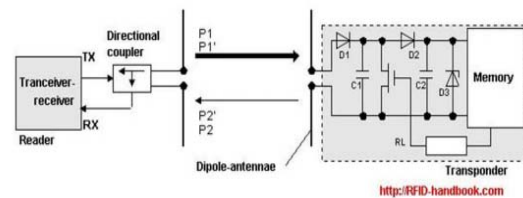

Figure 3: Backscatter Coupling

RFID technology is an easy-to-use identification system, flexible and suitable for operating systems automatically. RFID can be designed in an equipment that can be read only (read only) or that can be read and written (Read / Write). In this case it is unlike infrared which requires direct contact or a light path in accessing the barcode to be able to operate.

To create a Back End Control design for sensors embedded in a passive RFID tag chip, this passive RFID tag works at a frequency of 13.56 MHz (High Frequency), which requires a low voltage supply of 3.3 volts and which is energy efficient with low power dissipation.

The Back End Control on this passive RFID tag chip captures the analog data from the

sensor, converts them to the digital data and sends them to the RFID Reader via a modulator. The analog data are obtained from the object whose data will be retrieved.

Designing a backscattering control unit uses the backscattering method [22] which will control the addressing mode and the reading mode. Addressing mode is the time of the process in getting the information signals from the demodulator, selecting and retrieving the data, until converting the analog data into the digital data. Reading mode is the time when controlling the ADC delta sigma output that is ready to be sent to the RFID Reader via a modulator. A converter of the analog signal to the digital signal (ADC) is needed.

A converter of an analog signal into a digital signal is the most important component in the data acquisition. If an analog signal can be transformed into a digital signal, the computer can process the data needed later. Converting an analog signal into a digital signal requires a device called a converter, namely the Analog to Digital Converter (ADC). ADC works by encoding a continuous time analog signal voltage into a discrete time series of digital bits called Digital Signal Processing (DSP) [1],[27]. In devices such as sensors, ADC is used as an intermediate analog sensor with a computer which is then measured using a digital system [2].

Two basic characteristics of the main principle of ADC are sampling speed and resolution. The sampling rate shows how often the analog signals are converted to the digital signals in a certain time range. The ADC resolution determines the accuracy of the value of the ADC conversion results, namely the higher the ADC resolution, the more accurate the ADC conversion results [3] [4].

One type of ADC that exists is delta-sigma [5]. This ADC is widely applied to the audio equipment because it has a high resolution, but the disadvantage is the low speed. Much research has been carried out on this delta-sigma ADC type in an effort to increase the speed so that it can be used for the RF applications with mixed design technology [6]. Delta-sigma ADC has a simple circuit, high resolution, small power efficiency, and small layout size compared to the other types of ADC [5] [7].

In RF devices such as RFID sensors, the ADC is much implemented as a converter. Some studies of RFID with delta-sigma ADC include [8] implementation of delta-sigma ADC on RFID Passive Tags, and [9]

implementation of delta-sigma ADC in the form of serial digital data sent to the RFID reader using the ASK modulation-demodulation (modem) with a frequency of 13.56 Mhz (High Frequency). In research [8] and [9] the serial digital data output in research [8] is still considered not fast enough, so parallel digital data output can be needed.

In this study, it brought forward a method of modifying a serial data signal from the ADC sigma-delta output on an RFID Tag which becomes a parallel signal to an RFID reader. One method that converts the serial data signal into a popular parallel is that it can use a decimator. The research related to the decimator has been carried out in the researches [11], [12], [13] using the Comb Decimator (DC) circuit method. In Previous research, DC circuits can convert series to parallel, but the number of transistor components used is still too much with the power dissipation used is quite large, which consists of 4525 transistors with a power dissipation of 2.2 Watt. [11]. In this research, we propose a circuit design that can convert serial data signal to parallel. This design can be used and implemented on the reader of the RFID device. This circuit design is called the Dump Accumulator (DA), which consists of a register and counter circuit.

The objective of this research is to design a circuit on the RFID reader that can convert serial to parallel data signals with minimal use of transistor components and low power dissipation from previous studies. The CMOS technology used to design DA in this study uses CMOS 0.35 um from AMS[29],[30]. The DA design is expected to produce a more efficient design compared to the Comb Decimator method. Besides, this DA design can enrich researches in the field of system on chip (SOC).

2. DELTA-SIGMA ADC

The Block diagram of the Order 1 delta-sigma ADC modulator in the time domain can be seen in Figure 1 [12]. The output of this ADC is digital data with the input voltage (Xi) in the serial data format. Many samples of the input signals to produce a 1-bit code stream are acquired by the delta-sigma ADC. The Clock System (Ck) works with the sampling speed (Fs) on the comparator (1 bit ADC) so that the resulting quantization is in harmony with the clock system.
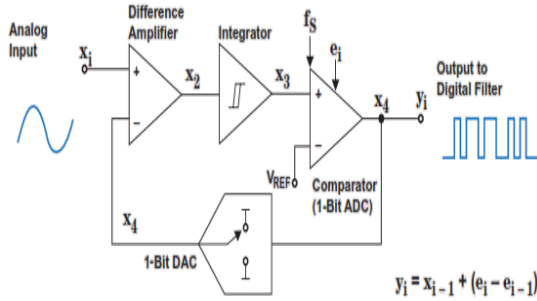
Figure 4: Order 1 Delta-Sigma ADC modulator in the time domain

Based on Figure 4, the ADC sigma delta consists of a Difference Amplifier, Integrator, Comparator and Digital Analog Converter (DAC)

2.1 Difference Amplifier

The Difference amplifier is implemented using a Bipolar Junction Transistor (BJT) or Field-Effect Transistor (FET). In order that DA will produce very high speeds, an emitter-coupled (ECL) logic circuit is used. The DA configuration consists of two transistors Q1 and Q2 arranged in a Common Emitter (CE), the differential pair has two inputs V1 and V2 with Vo1, Vo2 and Vout outputs [16]. A simple circuit of DA can be seen in Figure 5.
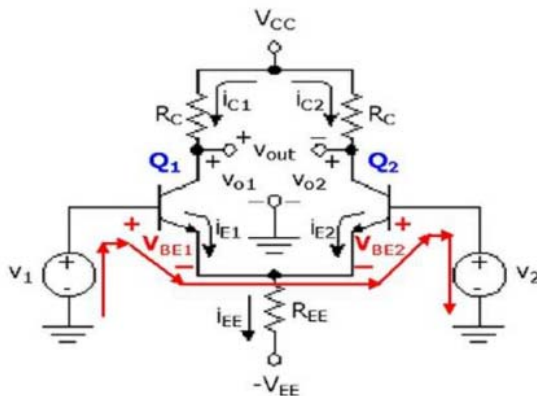

Figure 5. Differential Amplifier Circuit [16]

2.2 Integrator

The Integrator circuit is built on the basis of Op-AMP or also called integration amplifier. As it is built from Op-AMP, the integrator is similar to Inverting Op-AMP, but the feedback resistor (Rf) is replaced by the Capacitor feedback (Cf) as shown in Figure 6. The integrator functions to quantify the input signals in the form of an analog signal which will become the input for the comparator circuit.

The Integrator output voltage values can be calculated by equation (1), where C is an integration constant with the output voltage at t = 0. By equation (1), the output voltage has an inverse relationship between Rf and Cf. The result is a relationship that is directly proportional to the negative integral of the input voltage.

$$Vo = -1\left(\frac{Rf}{Cf}\right)xVin\int_0^t Vin\ dt + C \qquad (1)$$

In DC conditions, Cf provides infinite resistance so that the circuit will be like an inverting Op-AMP with the infinite feedback resistance where Rf = ∞. Then, the voltage gain equation (A) as in equation (2).

$$A = -\frac{Rf}{R1} \qquad (2)$$

By substituting   Rf = ∞, the gain A = ∞. This configuration was chosen because of a small offset voltage problem and a voltage error in the output. By adding Rf will improve the low frequency gain (A). Simply put, the offset voltage will not affect the offset output voltage.
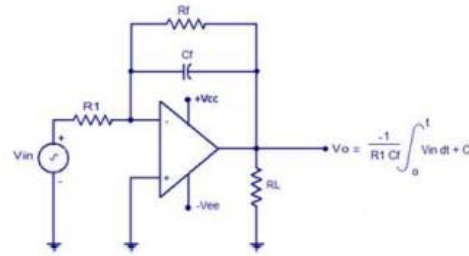

Figure 6. Op-AMP Integrator Circuit [17], [18]

2.3 Comparator

The comparator functions to compare the integrator output signal in the form of voltage with a reference signal. The comparator consists of two parts, namely the 2-stage Op-AMP Operational Transconductance Amplifier (OTA) [28] and buffer. The comparator circuit can be seen in Figure 7.
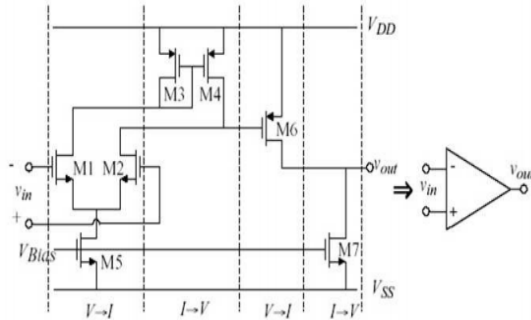
Figure 7. Comparator Circuit [6], [10]

3. DUMP ACCUMULATOR

The core parts of the delta-sigma ADC are the delta-sigma modulator and the decimator / digital filter which can be seen in Figure 8 [12]. The delta-sigma ADC output is still in the form of serial data so that it is generally converted from serial data to parallel data. This is converted with a digital filter and decimator circuit.
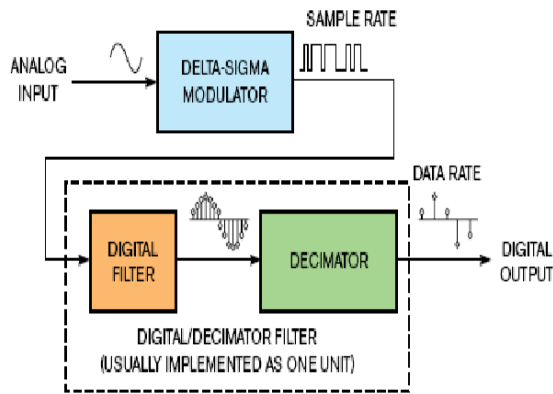

Figure 8: The core functions in the delta-sigma ADC are the delta-sigma modulator and the decimator / digital filter [14].

Replacement of digital and decimator filters are the dump accumulator which functions as a modifier to the ADC output from serial to parallel. The decimating filter given in the Bandwidth equation (B) is half the sampling frequency (fs) divided by the average input sample (K) used in the accumulator and dump method [6] [15]. Decimating filters in the time domain can be formulated by equation (3).

$$y(Ki.Ts) = \sum_{n=K(i-1)}^{Ki-1} \frac{x[n.Ts]}{K} \qquad (3)$$

To get the average input, the decimating filter takes input K by adding together, then dividing the results by K. If K = 16 and i = 1, then the samples from x (0) to x (15) are added and divided by 16. If in the z-domain, equation (3) can be rewritten, so the z-domain representation for the filter is formulated in equation (4) or (5).

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{K}\sum_{n=0}^{K-1} z^n = \frac{1}{K}(1 + z^{-1} + z^{-2} + ... + z^{1-K}) \quad (4)$$

Or

$$H(z) = \frac{1}{K}\cdot\frac{1 - z^{-1}}{1 - z^{-1}}\cdot(1 + z^{-1} + z^{-2} + ... + z^{1-K}) \qquad (5)$$

The z-domain transfer function for the decimator (average) can be seen in equation (6)

$$H(z) = \frac{1}{K}\cdot\frac{1 - z^{-K}}{1 - z^{-1}} \qquad (6)$$

If K = 8, then the equation (6) becomes equation (7)

$$H(z) = \frac{1}{8}\cdot\frac{1 - z^{-8}}{1 - z^{-1}} \qquad (7)$$

4. PROPOSED DESIGN

In this research, a series of sigma-delta ADCs and dump accumulators are proposed. The block diagram design can be seen in Figure 9. The two parts are parts of the RFID system, where the ADC sigma-delta is in the tag and the dump accumulator is in the reader. This RFID system refers to a passive RFID tag study [9], where the analog sensor insert will be converted using delta-sigma ADC.

After that, the serial data are generated from the delta-sigma ADC output which are next transmitted to the RFID reader with ASK modulation-demodulation (modem) with a frequency of 13.56 Mhz. In the RFID reader, the transmitted data resulting from the RFID tag are later entered, still in the form of serial data, which are then converted using a dump accumulator so that they become parallel data. These parallel data can speed up the process of reading data from RFID tags.
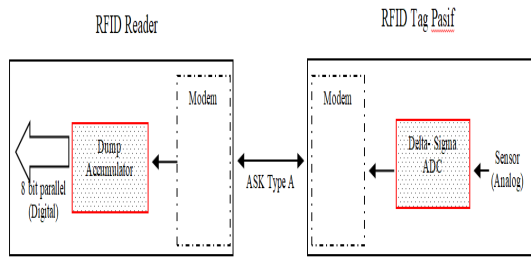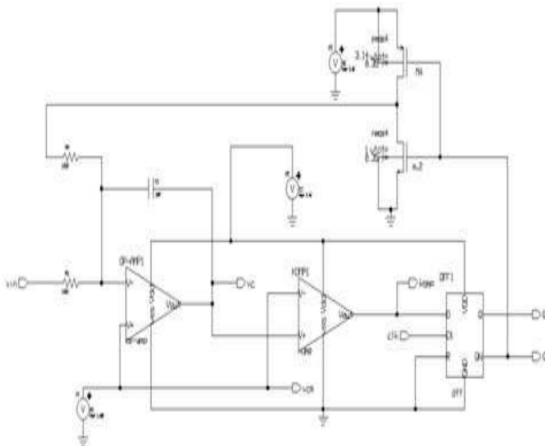
Figure 9: Block diagram design of RFID 13.56 MHz tag and reader

4.1. Design of ADC Sigma-Delta

The design of a sigma-delta ADC circuit on CMOS basis can be seen in Figure 10 [14].The input data from the sensor are still in the form of analog data with a 3.3V VDD voltage source supply with an offset voltage of 1 V and a reference voltage on the comparator 1V.

Figurer 10: Delta-Sigma ADC design

The delta-sigma ADC circuit is built from a series of Integrators, comparators and 1 bit DAC. Clock is used to count the resulting quantization time. The input voltage (Vin) is 1 volt, and the offset voltage is 1volt. The delta-sigma (Q) ADC circuit outputs are still serial logic 1 and logic 0 data.

4.1.1. Integrator Design

The design of an the integrator circuit based on the cmos transistor can be seen in Figure 11. The Resistor Feedback (Rf) and the Capacitor Feedback (Cf) are used to obtain the infinite gain as in the equation (1).
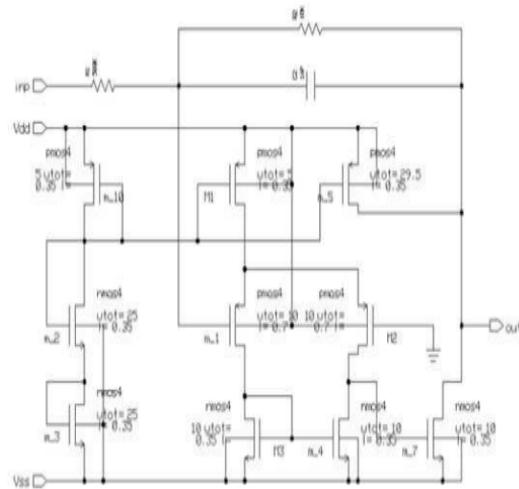

Figure 11: Integrator Circuit

4.1.2. Comparator Design

The design of the comparator circuit based on CMOS is shown in Figure 9. This circuit will compare the output signals from the integrator which will be the input signals of the comparator with the reference signals. The output signals from the comparator consist of two signal levels, namely the signals above the reference signals and the signals below the reference.
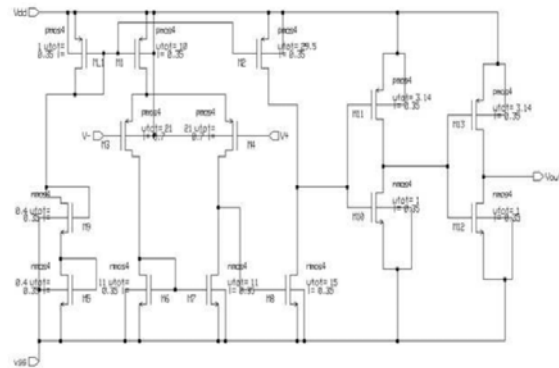
Gambar 12: Comparator Design

4.2. Dump Accumulator Design

The proposed dump accumulator design can be seen in Figure 13. In accordance with the proposed Figure 14, the dump accumulator is placed in the reader position to speed up the process of data reading. The data transmitted from the tag are still in the serial data format. The serial data will then be stored into a counter. After the data are collected, the data will be released into 8-bit parallel data through synchronously working registers.
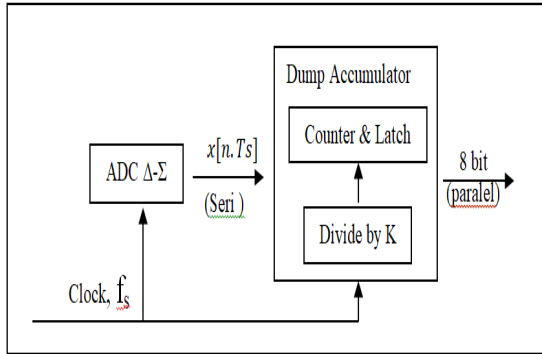
Figure 13: Diagram block of accumulator dump for delta-sigma ADC.

This circuit consists of two circuit blocks, namely the Divide by K series as accumulators and the Counter and the Latch register as dumps. The accumulator consists of counters and AND gates while the dump consists of counters and latches that function as registers. This circuit is designed functioning as a determinant of resolution (K) to produce an output of 8 bits.
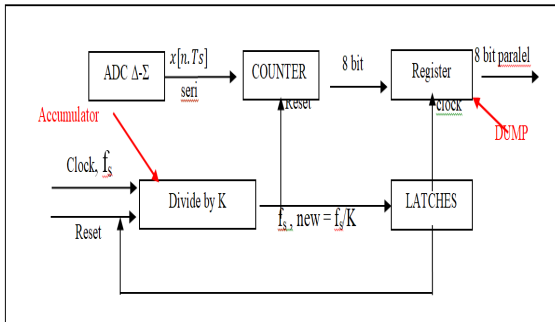

Figurer 14: Complete diagram block of the accumulator dump circuit.

A discrete dump accumulator circuit design can be seen in Figure 14. The design of the dump accumulator consists of a combination of counter circuits in Figure 16 and registers in Figure 17; while the Accumulator Block consists of a series of counters and AND 8 input gates. This AND 8 input gate functions as Reset. If all logical inputs are 1 (high), the counter will reset. The Clock (fs) as synchronization works in harmony between delta-sigma ADC blocks.
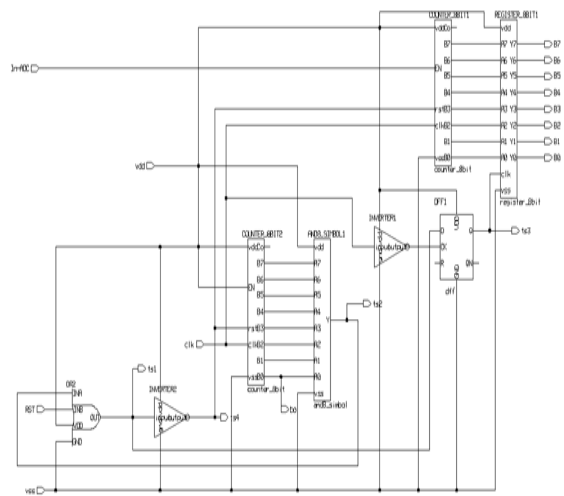

Figure 15: Design of accumulator dump circuit.

Figure 15 is the 8-bit counter circuit contained in the dump accumulator circuit, Figure 16. The counter circuit is built from the Half Adder (HA) circuit, AND gate, and Flip Flop D. The Enable input (EN) on the counter circuit is obtained from the ADC delta-sigma output . The EN input is still in the form of serial data which next becomes the HA series, it is then held in the D Flip-Flop circuit. The output from the counter data is already in the form of parallel data.
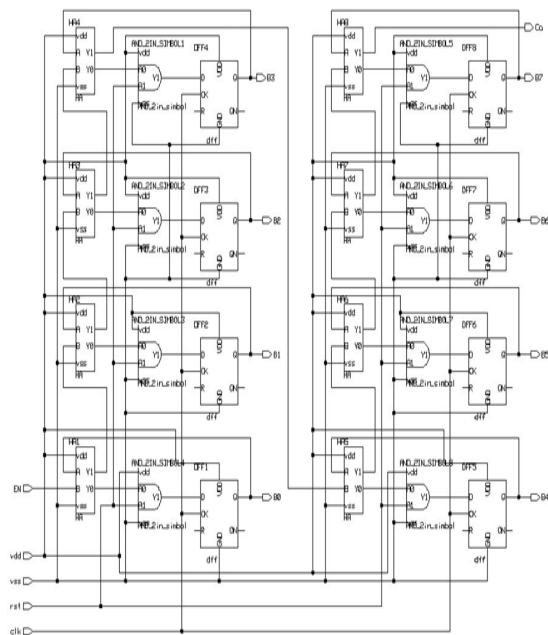

Figure 16: 8-bit Counter circuit.

Figure 17 is an 8-bit register circuit built from 8 D flip flops with V0-V7 strength. The functions of the register are to hold and then to produce the 8 parallel bits of data as the desired output in this study.
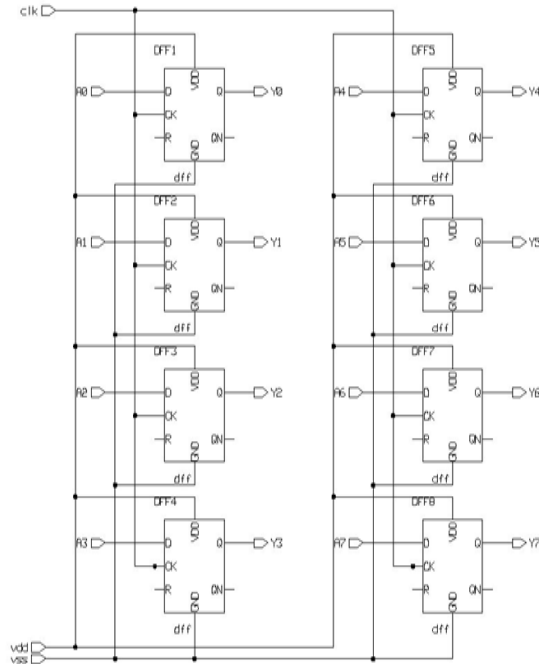

Figure 17: Rangkaian Register 8 bit.

5.   SIMULATION RESULTS
5.1. Simulation of Integrator Circuits

The results of the Integrator output in the sigma-delta ADC circuit are shown in Figure 18. The output of the sigma-delta ADC signal is enlarged by the V (IN) input, the integrator output as V (c), the Comparator output signal as V (komp), the clock signal V (V) clk) and the sigma-delta V (Q) ADC output, where the output V (Q) is still in the form of a digital signal with serial data format. The Value V (IN) input is 1 V with a resistance value R = 100 k$\Box$, capacitor C = 10pF and with the time needed to raise the signal dt = 0.4 μs. The simulation results and the equation (1) produce the output V (c) = 0.4 V.
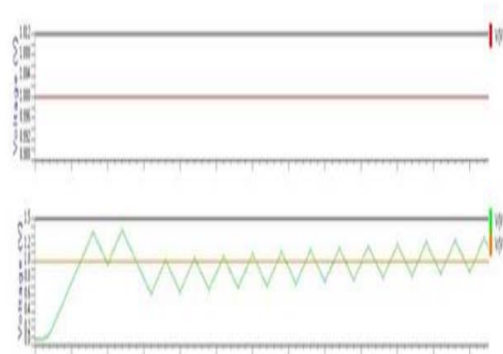

Figure 18: Integrator simulation results

5.2. Simulation of Comparator Circuits

The comparator circuit simulation results are shown in Figure 19. This circuit works by comparing the output signal from the integrator and the reference signal V (N) of 1 V. The results obtained are two signal levels. If the integrator output signal value V (c) is below V (N), the comparator output signal V (komp) is considered a logic value Low (0), and vice versa, if V (c) is above V (N), the signal output V (komp) is considered a high logic value (1).
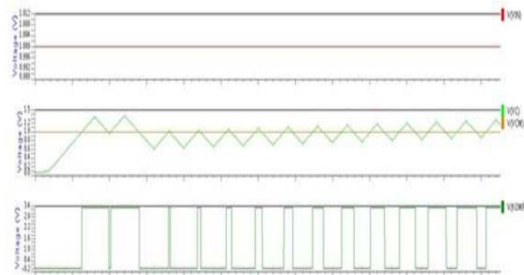

Figure 19: Comparator Simulation Results

5.3. Simulation of Sigma-Delta ADC

The simulation results of the delta-sigma ADC output signal can be seen in Figure 20. The input signal V (VIN) of 1 volt goes into the integrator circuit with a resistor value (R) = 100 kΩ; a capacitor (C) = 10 pF and the time required for the signal to raise (dt) is 0.4 μs, then the output V (Q) is obtained as in figure 10. To get the output signal V (Q), the integrator output with V_{offset} = 1 volts with an integrator signal above the offset voltage gives a high logic value (1), and an integrator signal below the offset gives a low logic value (0). The comparator output signal is an input to the D flip-flop circuit synchronized with the clock to produce an ADC delta-sigma V (Q) output signal. The value of V (Q) will be an input into the

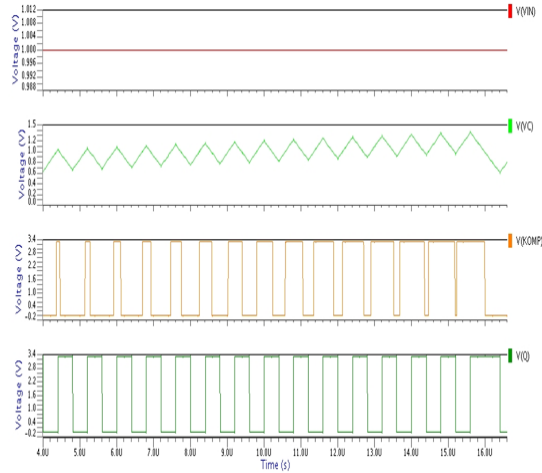accumulator dump circuit as a serial data converter to be parallel.

Figure 20: Simulation results of the delta-sigma ADC output signal.

The results of the simulation of accumulator dump can be seen in Figure 21. The input signal V (IN) of 1 volt and the ADC output of delta-sigma V (OUT_DS1). V (B0) - V (B7) are 8 bits of parallel signal output from the dump accumulator. At the beginning, namely period 1, it is a process of synchronization and initialization that takes up to 10.8 µs. After that, period 2 starts from 10.8µs to 21µs. The Output V (B0) is as the least significant bit (LSB) to V (B7) as the most significant bit (MSB).

In period 2, V (B2) and V (B7) produce high logic so that the output generated is 0111 1011$_{(2)}$ or 123$_{(10)}$ in decimal where the data should be 0111 1111$_{(2)}$ or 127$_{(10)}$. The output can be said to be equivalent to the output that should have been 127$_{(10)}$. In period 3 at the time between 21µs to 31.3µs the opposite occurs that V (B2) and V (B7) show a low logic so that the output is 11000 0100$_{(2)}$ or 132$_{(10)}$ which should have been 1000 0000$_{(2)}$ or 128$_{(10)}$. The output in period 3 can also be said to be equivalent to the output that should have been 128$_{(10)}$. The number of transistors needed in the dump accumulator is 1022 transistors with a power dissipation of 28.5 mW.
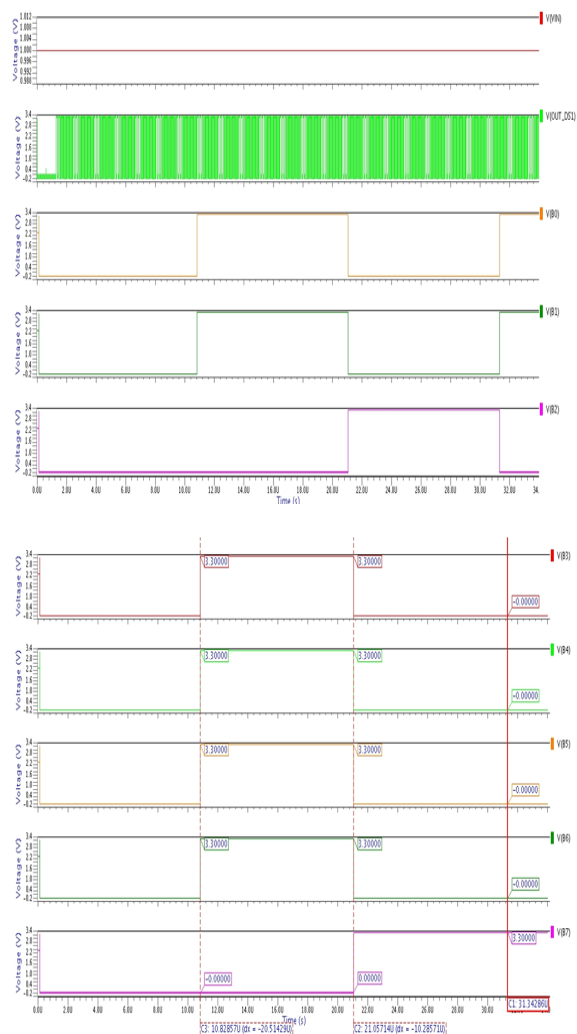

Figure 21: The results of the simulation signal of the accumulator dump

The comparison of the results of this study with the previous research is shown in table 1. The results in this study indicate that the serial to parallel process can use a dump accumulator circuit. On the use of transistor components, there is that the savings in component use and power dissipation are smaller than previous studies. The result of the output bit test shows that the difference with the value it should be is the value of the LSB bits.

Table 1. Comparison Result

Method	Process	Transistor	Power Dissipation (Watt)	Pros	Cons
Comb Decimator	Serial to para	4525	2.2	-	Transistor Usag

	llel				e
Dump Accumulator	Serial to parallel	1022	0.285	Transistor usage and Power Dissipation	LSB Value

6. CONCLUSION

The design of a dump accumulator with serial to parallel processing on an RFID reader has been discussed. The dump accumulator circuit design can convert eight digital bits serially into eight parallel bits as expected. The dump accumulator design consists of registers and counters circuit using 0.35 μm CMOS technology . From the simulation test results which are divided into 3 periods, namely period 1 : (T0) initialization and synchronization, period 2 : (T1) 8 parallel binary data equivalent to 127 (10) and period 3 : (T2) 8 parallel binary data equivalent to 128 (10). Besides, the result of this design is that the number of transistor components used is 1022 transistors with a power dissipation of 28.5 mW. The efficiency of using transistors was 77.42% and 98.72% for power dissipation from research using a decimator. From the discussion of these results, the design in the future would try to processed fabrication an IC CMOS 0.35 μm based process..

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