SPICE ELECTRICAL MODEL OF COOLMOS TRANSISTOR CONSIDERING QUASI-SATURATION EFFECT

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ABSTRACT

This paper deals with the macromodelling of the CoolMOS power transistor. A novel power CoolMOS transistor macromodel giving accurate results is setting up. It is based on the subdivision of the CoolMOS power transistor into an intrinsic MOSFET, a JFET, a Zener diode and a voltage-controlled voltage source. All these components are incorporated within a sub-circuit in order to describe the power CoolMOS transistor effects like saturation and quasi-saturation. These effects as well as the parameters extraction procedure will be explained clearly in this paper while introducing the new sub-circuit model. The effectiveness of the proposed model has been verified by comparing the proposed model simulation results under PSpice with the results of datasheets given by manufacturers and with the models presented by Infineon Technologies. Our model provides an accurate description in all operation regions for DC characteristics. It gives less than 5.5% as an average error percentage for the output characteristics.

Keywords: *Macromodel, CoolMOS, PSpice, Saturation, Quasi-saturation.*

1. INTRODUCTION

Conventional power MOSFET structure, as any power component, integrates an area called drift region, which has a dual effect. On one hand, it allows sustaining voltage in the OFF state and on the other hand it has a significant resistive side in the ON state. For highest breakdown voltages (V_{br}), largest and lightly doped drift region are needed [1]. Therefore, this large and softly doped region presents in the ON state, a very high resistance (R_{ON}) which often generates unacceptable values of the energy losses that can damage the component [2]. According to Equation (1), the increasing of V_{br} produces a significant increase in R_{ON} [1].

$$R_{ON} = \frac{4\ V_{br}^2}{\varepsilon_0\ \varepsilon_r\ \mu\ E_c^3} \qquad (1)$$

where V_{br} is the desired breakdown voltage, μ is the electron mobility, ε_0 is the permittivity of free space,

ε_r is the relative permittivity and E_c is the critical electric field.

In high voltage (HV) applications, the rapidly increase of the R_{ON} penalizes the functionality of the conventional power MOSFET, and this is considered as the major drawback. The major challenge consists of finding the best trade-off between the on-resistance and the breakdown voltage. In order to overcome this compromise, new concepts have been proposed. We cite the super-junction (SJ) and floating islands (FI) [3,4], whose idea's based on the structural change of the drift zone. Also, advanced semiconductors materials as Silicon-carbide (SiC) can be considered [2,5].

The introduction of the superjunction concept in the late 1990s showed that by adopting a different design based on the introduction of alternating N and P semiconductor bands with relatively high doping in the drift region, the on-state resistance may be

reduced compared to the conventional power MOSFET transistor.

CoolMOS transistor, also called the Super-junction MOSFET or the super multi-resurf MOSFET [6, 7], based on the superjunction concept, is considered as a revolutionary technology for high voltage power MOSFETs [8]. The first CoolMOS power transistor has been manufactured and marketed by Infineon Technologies [9]. Up to now, different CoolMOS generations of different values of drain to source breakdown voltage (500- 900V) have seen the day [10-13].

With the advent of this new technology, the so-called silicon limit was broken in terms of the on-resistance [14]. The CoolMOS transistor provides a fast switching speed and a reduced R_{ON} by factor of 5 when maintaining the same V_{br} [9,15,16]. It offers a significant reduction of conduction, switching and driving losses compared to the conventional power MOSFETs counterparts [10]. As it is shown on Figure 1, compared to the conventional structure for the same level of breakdown voltage, the R_{ON} was dramatically reduced.
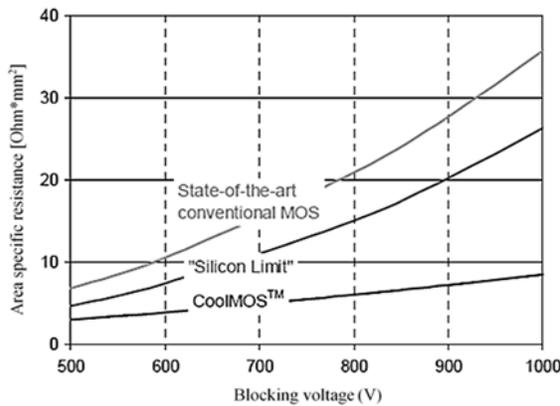

Figure 1: Area-specific on-resistance versus breakdown voltage comparison of conventional MOSFET and CoolMOS technology [17]

The CoolMOS structure employs a novel drain structure using the super-junction concept in contrast to the conventional power MOSFET (Figure 2); the constant N- drift region of the conventional power MOSFET is replaced by several vertical alternating strips N- and P- [18], hence, the obtained principal junction becomes more important. This modification

leads to a significant change in the electric field profile in the device, resulting in a high breakdown voltage and low on-state resistance.

In these structures, the main I_{DS} current path is much more heavily doped than for a conventional power MOSFET: the doping level in the N- pillars is higher than that of conventional power MOSFETs, which reduces the on-state resistance. It should be pointed out that the SJ devices are based on the charge compensation principle: The doping level of the N- pillars becomes greater than that of the conventional power MOSFET and the excess charge in the N- pillars can be counterbalanced by the adjacent charges in the P- pillars. The CoolMOS structure is depicted on Figure 2b.
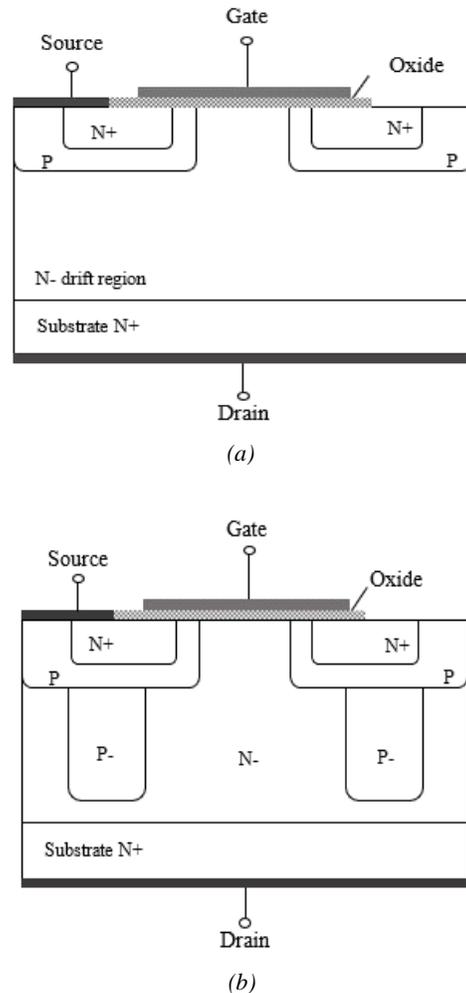

(a)

(b)

Figure 2: Conventional power MOSFET structure (a) CoolMOS transistor structure (b)

In the on state, the I_{DS} current flows through the N- pillars to the drain; the conduction area is then reduced compared to VDMOS transistors, whose entire active area is used for the drain-source current conduction. The P- pillars do not contribute to conduction in the on-state, but they are essential for achieving a higher breakdown voltage, despite the high doping of the N and P bands. In the off-state, the N and P bands will be fully depleted well before the breakdown voltage is reached, resulting in a flat electric field profile instead of a triangular profile as in the case of VDMOS transistors.

Modelling is a needful step to estimate the device behavior. Over the past years, in order to represent the power MOSFET behavior, numerous models have been developed and improved [19-28]. These models use an equivalent circuit of the power MOSFET transistor structure consisting of an intrinsic conventional MOSFET, representing the channel region, and active or passive devices added in series to represent the drift region behavior. Generally, two approaches were used to describe the power MOSFET behavior [27]: compact modelling [19-22] and macromodelling [23-28]. Compact models are generally based on the physics of semiconductor and need technological and geometrical parameters that are not given by manufacturers. As for the macromodels, they use SPICE built-in models. Also, they present many advantages such as a higher accuracy, a good portability as they can be integrated on all electrical simulation software, and an independence of the component physical parameters.

The first CoolMOSC2/C3 SPICE macromodels were elaborated by Infineon Technologies in 2001 to describe the behavior of the power CoolMOS transistor [24,26,29]. Presently, different PSpice models of the CoolMOS generations are available at the Infineon Technologies website [30]. The model proposed in [24] uses a polynomial gate voltage dependent source (VCVS) with a smoothing function to represent accurately the saturation effect of I_{DS} of the power CoolMOS transistor. Although this modelling assures a good accuracy, the associated extracting parameters method of the gate VCVS is time consuming as the coefficients of the

polynomial function used need many attempts to ensure a good fitting with measurements characteristics given in manufacturers datasheet.

In this paper, a new macromodel for the CoolMOS transistor, inspired by the model presented in [24], suitable for accurate prediction of static CoolMOS's transistor behavior is presented. The model required parameters were extracted from datasheet using a simple parameter extracting method. The paper also demonstrates the model performance, using the PSpice simulator, for different CoolMOS generations device samples: CoolMOSC3, CoolMOSC6 and CoolMOSCP power transistors. The simulation results of our model will be compared to the ones of the models available at the Infineon Technologies website [30] for the cited samples. To further prove the performance of the presented model, another comparison has been done with the model proposed in [24] in terms of accuracy, simulation time and parameters extraction method complexity. Our model describes with excellent agreement the I-V characteristics of the CoolMOSC3, C6 and CP over the all V_{GS} values.

The remaining paper sections are arranged as follows: The macromodel and the parameter extraction procedure of the model components will be presented and explained in section 2 and 3. The results of comparison between the simulation results and those of measurement taken from manufacturer datasheets using an appropriate program named GetData graph digitizer will be given and discussed in the section 4 before the conclusion.

2. THE PROPOSED COOLMOS DC MACROMODEL

According to the Figure 2b, when an applied gate voltage V_{GS} exceeds the threshold voltage V_{Th}, the electrons flow from the N+ source through the created channel under the gate, through the N- pillar of the drift region to the drain terminal. Therefore, we can assume that the CoolMOS sub-circuit is a combination of an intrinsic MOSFET and a drift region. Hence, the new macromodel proposed to describe the static behavior of the CoolMOS power transistor is shown in Figure 3. It incorporates within

an equivalent sub-circuit, a standard low voltage SPICE level 3 MOSFET (intrinsic MOS) to represent the channel region behavior, a JFET in series to describe the drift region effect, a dependent source E to have a continuous transition between linear and saturation regions and a Zener diode linked between the gate and the source to model the saturation effect. The choice of low voltage SPICE level 3 MOSFET is based on the fact that it is simple, more accurate and requires a simple parameter extraction procedure.
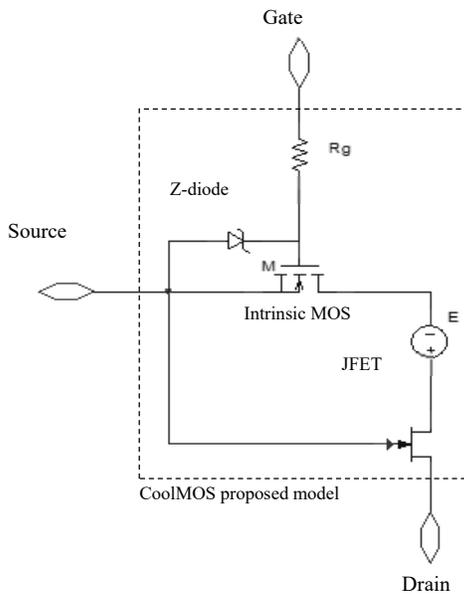

Figure 3: New CoolMOS sub-circuit

The CoolMOS power transistor terminals are as follow: the drain of the JFET is the same as the drain of the CoolMOS power transistor, while the source and the gate conform to the ones of the intrinsic MOSFET (NMOS).

As it is shown in the measured output characteristics of the IPA60R125C6 CoolMOSC6 transistor (Figure 4), for lower values of V_{GS}, and with the increasing of V_{DS}, the saturation regime is obviously observed. The current can no longer increase proportionately with V_{DS}, therefore the intrinsic MOS is saturated. The CoolMOS power transistor behavior is well modelled by the intrinsic MOSFET model because the channel resistance is very large compared to the drift resistance [31].
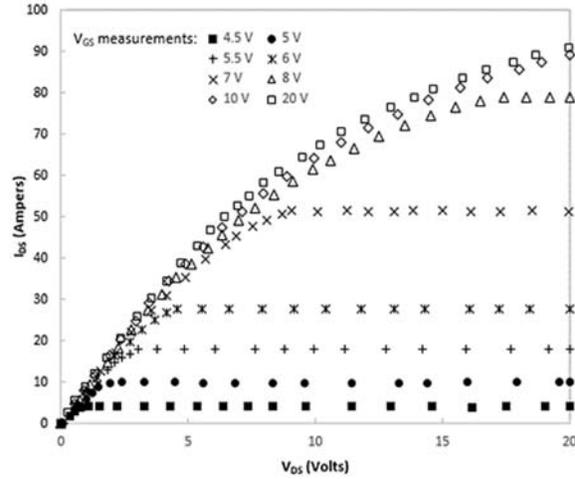

Figure 4: Measured output characteristics $I_{DS} = f (V_{DS})$ of the CoolMOSC6 power MOSFET

We note that for certain values of V_{GS} ($V_{GS} >$ 8V), as it is shown in Figure 4, the output characteristics start to compress. The current I_{DS} incurs a partial saturation and rises slowly with V_{DS}. It is independent of gate to source voltage V_{GS}. In this case, the drain current is dominated by the drift region current instead of that of channel region because the drift resistance becomes higher than the channel resistance [23,24,31]. This phenomenon is referred to as quasi-saturation. As well documented in [20,32,33], this effect occurs when both the gate and drain biases are high: when V_{DS} is sufficiently large, the lateral electric field intensity E surpasses a critical value E_C and causes carrier velocity saturation in drift region causing the quasi-saturation effect. The drift region is well modelled using a JFET to account for a quasi-saturation effect.

The voltage-controlled voltage source E linked between the drain of the intrinsic MOSFET and the source of the JFET, is used to make a smooth continuous transition for V_{DS} from the linear to the saturation region. This can be done using the following smooth function [34]:

$$V_{DS,eff} = V_{DS,sat} - 0.5 * \left[V_{DS,sat} - V_{DS} - \delta + \sqrt{(V_{DS,sat} - V_{DS} - \delta)^2 + 4\delta V_{DS,sat}} \right] \quad (2)$$

where δ is a parameter that helps adjusting the smoothness of the transition between the linear and the saturation region.

3. PARAMETERS EXTRACTION PROCEDURE

For clarity, capital letters are used as subscripts for the designation of the complete power CoolMOS transistor parameters, while lower case letters are used for the designation of JFET parameters.

The proposed model requires a simple parameters extraction procedure:
At a constant value of drain-source voltage (V_{DS}= 20 V) and for T = 25 °C as it is shown in Figure 5, the transfer characteristic (I_{DS} = f (V_{GS})) becomes linear when the gate voltage is increased towards a critical value named V_{GSC}. The electrical current (I_{DS}) increases while the gate voltage is lower than V_{GSC}, but by reaching this value, the transconductance becomes quasi-constant [25,35]. The Zener diode linked between the gate and the source is used to model the saturation current at V_{GSC} by making the Zener breakdown voltage (BV) equals to V_{GSC}: Once V_{GS} reaches V_{GSC}, the Zener diode will clamp the applied gate to source voltage V_{GS} to its breakdown voltage (BV). From Figure 5, the critical gate to source voltage V_{GSC} can be extracted.
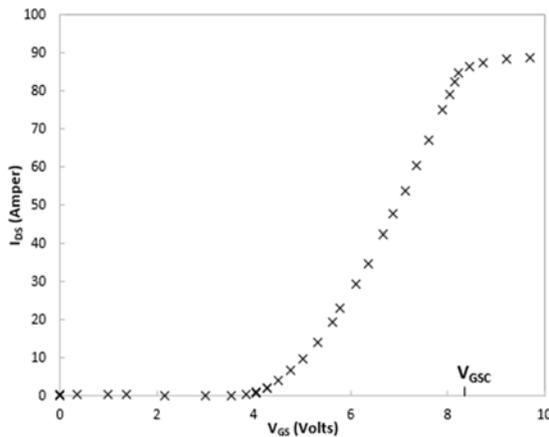

Figure 5: Measured transfer characteristic $I_{DS} = f(V_{GS})$ of the CoolMOSC6 power MOSFET at $V_{DS} = 20$ V and T= 25°C

3.1. Intrinsic MOSFET parameters

The SPICE level 3 MOSFET model requires mainly two parameters: the threshold voltage V_{Th} and the transconductance K_P. These parameters are extracted from the transfer characteristics when the transistor is operating in saturation mode at high V_{DS}

(V_{DS} = 20 V) as shown in Figure 6. The MOSFET drain current equation in the saturation region is as follow:

$$I_{DS} = \frac{K_p}{2} (V_{GS} - V_{Th})^2 \qquad (3)$$

The interception of the tangent drawn at the maximum first derivative point of $\sqrt{I_{DS}}$ versus V_{GS} curve and the gate voltage axis is equal to V_{Th}. The transconductance K_P is extracted from the tangent slope which is equal to $\sqrt{\frac{K_p}{2}}$.
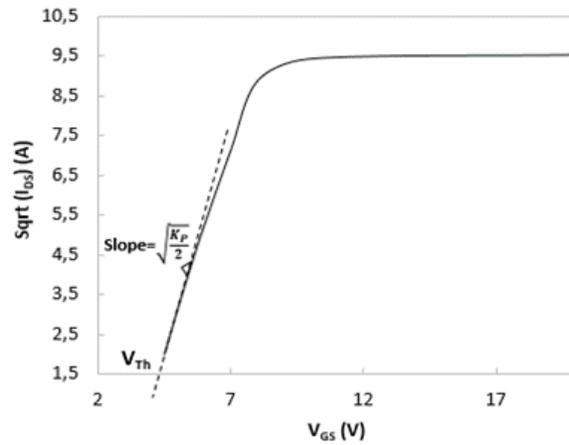

Figure 6: $\sqrt{I_{DS}}$ versus V_{GS} curve for the CoolMOSC6 power MOSFET at $V_{DS = }$ 20 V

3.2. JFET parameters

The required JFET parameters β and V_p, which are respectively the transconductance and the pinch-off voltage, can be extracted from the following equation:

$$I_D = \beta. V_{DS} [2 (V_{gs} - V_t) - V_{DS}] \qquad (4)$$

where V_p = -V_t

When high gate voltage is applied on the CoolMOS power transistor, the channel resistance is smaller than the drift resistance. Hence, we may assume that V_{DS} of the CoolMOS is the same as V_{DS} of the JFET and $V_{gs} \approx 0$ V for the JFET.

To calculate the two JFET parameters, we suppose that V_{gs} = 0 V. Equation (4) can be rewritten as follow:

$$I_D = \beta . V_{DS} [2 V_p - V_{DS}] \tag{5}$$

By choosing two points (I_{DS1}, V_{DS1}) and (I_{DS2}, V_{DS2}) from the target CoolMOS output characteristics given in datasheet, we can extract the two needed JFET values β and V_p from Equation (5).

Table 1 lists the extracted model parameters for the IPA60R125C6 CoolMOS N-channel power MOSFET using measured graphs given by manufacturer datasheet.

Table 1. Extracted Model parameters for IPA60R125C6 CoolMOS N-channel power MOSFET

Parameter	Description	Unit	Value
V_{Th}	Threshold Volatge of the MOSFET	V	3.6
K_P	MOSFET Transconductance	A/V²	9.54
V_p	Pinch off voltage Of the JFET	V	19.2
BV	Zener Breakdown voltage	V	8.14
β	JFET Transconductance	A/V²	0.29
δ	Smoothness factor	-	0.01

4. MODEL RESULTS AND DISCUSSION

The sub-circuit simulation was performed using PSpice. In order to validate the efficiency of our macromodel to represent faithfully the DC CoolMOS behavior, different CoolMOS generations device samples were used, namely SPP08N80C3, IPA60R125C6 and IPL60R385CP.

Figure 7 presents the simulation results of the output characteristics obtained with the CoolMOSC3 PSpice model available at the manufacturer website [30] in comparison to the measurements given in datasheet. As it is shown, the model given in [30] produces very large errors compared to the measurements. It gives 26.56% as average error for the output characteristics and 27.16% for the transfer characteristic. Using our proposed model, the average error for the output characteristics can be reduced to 3.65% with 5.34% as a maximum error (Figure 8). Regarding to the

transfer characteristic, our model can give 8.07% as an average error. The proposed model presents better agreement with the measured data and an improvement of 22.91% compared to the manufacturer model for the output characteristics.
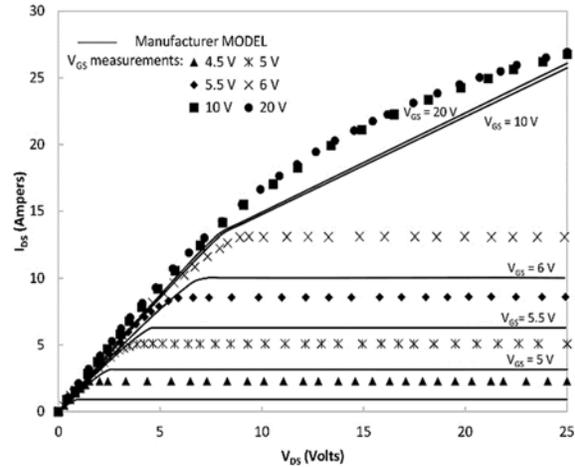

Figure 7: Comparison between the manufacturer model output characteristics and those of measurement for the CoolMOSC3 transistor
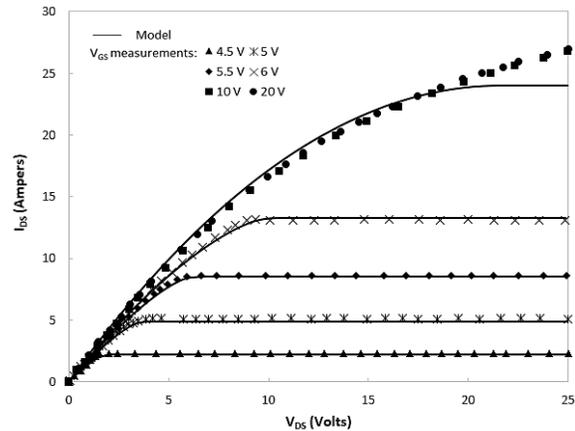

Figure 8: Comparison between the proposed model output characteristics and those of measurements for the CoolMOSC3 transistor

In order to evince the validity of the proposed model, other CoolMOS device samples were used. We applied this new model to the IPA60R125C6 CoolMOS N-channel power MOSFET. The static measurements given on the datasheet and the PSpice simulations results were compared.

Figure 9 presents the measured transfer characteristic of the IPA60R125C6 CoolMOS transistor compared to the simulations results for

T = 25°C and at V_{DS} = 20V. We can note that the new proposed model describes precisely the static behavior of the CoolMOS power transistor on the entire V_{GS} variation band. We observe that the simulations correlate well with the measurements. The transfer characteristic simulation results compared to the measurements of the IPA60R125C6 CoolMOS transistor give an average error equal to 4.58%, which is an improvement of 5.48% compared to the IPA60R125C6 CoolMOSC6 manufacturer model.
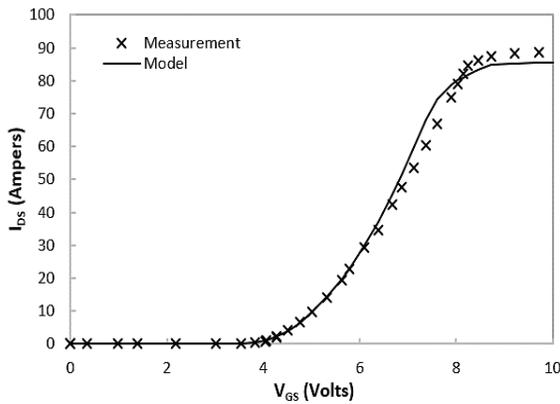

Figure 10: Comparison between the measurements and the proposed model transfer characteristic of the CoolMOSCP transistor at V_{DS} = 20 V, T= 25°

Figure 9: Comparison between the measurement and the proposed model transfer characteristic of the CoolMOSC6 transistor at V_{DS} = 20 V, T= 25 °C

Figure 10 and 11 respectively represent the comparison between the measured transfer characteristic at V_{DS} = 20 V for T = 25°C and the results of simulation of the IPL60R385CP CoolMOSCP transistor, and the measured output characteristics in comparison with the proposed model simulation results. As it is obviously observed from these figures, the proposed model represents faithfully the static behavior of the CoolMOS in all its regions. Indeed, our model reproduces results close to those of the model proposed by the manufacturer for the IPL60R385CP CoolMOSCP transistor. The results of comparison between the measurements results and the simulation results of our proposed model for the transfer characteristic gives 3.47% as an average error, while, for the output characteristics, the model gives an average error equal to 5.18%.
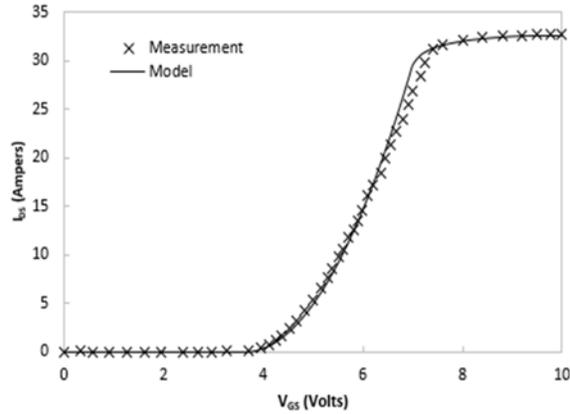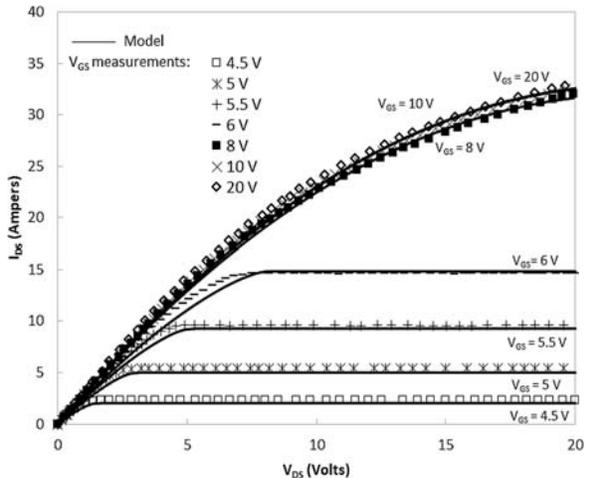

Figure 11: Comparison between the proposed model output characteristics and those of measurements for the CoolMOSCP transistor

Figure 12 is a comparison between the transfer characteristic simulation results of our proposed model and those of the model proposed in [24] for the IPL60R385CP CoolMOSCP transistor at V_{DS} = 20 V and T= 25°C. In this plot, a satisfied accuracy has been achieved for both of models over the whole V_{GS} values. As it is obvious on the figure, the simulation results of our proposed model show excellent agreement with measurement results in contrast to the model proposed in [24]. The results of comparison between the measurements results and the simulation results for the transfer characteristics give 3.47% as an average error for our proposed model, while, for the model proposed in [24], they give an average error equal to 5.55 %. So,

by using the Zener diode to model the saturation effect, our proposed model leads to a good accuracy, with less parameters extraction method complexity and low analysis time comparing to the one proposed in [24]. The SPICE simulation of our presented model has yielded up excellent results. Indeed, all the figure showed (figure 8 to 12) above confirm our conclusion.
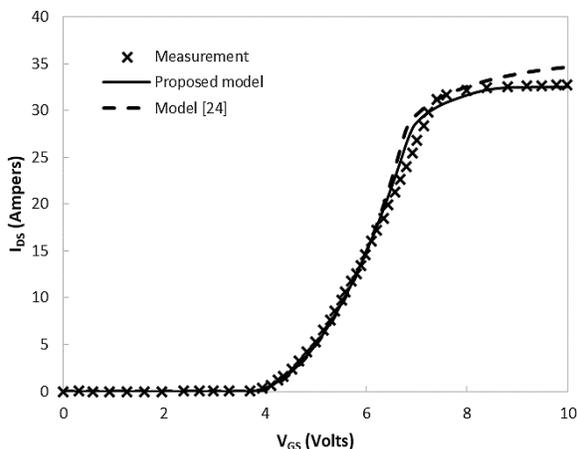

Figure 12: Comparison between the simulated transfer characteristic of our proposed model and those of the model proposed in [24] for the CoolMOSCP transistor at V_{DS} = 20 V, T= 25°C

5.   CONCLUSION

A new CoolMOS power transistor macromodel is proposed in this paper. The sub-circuit and the parameters extraction procedure were presented. The CoolMOS macromodel was implemented on the PSpice simulator in order to verify its effectiveness. The macromodel performance was demonstrated for different CoolMOS generations device samples: CoolMOSC3, CoolMOSC6 and CoolMOSCP power transistors. The proposed model can be used to model accurately the static behavior of the CoolMOS power transistor in all its regions. It produces correctly the quasi-saturation effect and leads to a good agreement between simulation and measurement results for the whole V_{GS} range.

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