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IMPLEMENTATION OF A PCG SIGNAL CLASSIFICATION SYSTEM IN THE FPGA EMBEDDED PLATFORM

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ABSTRACT

The medical assistance systems do not cease to evolve from one day to the next, which requires them to be implemented in reliable platforms that are capable of guaranteeing the efficiency and accuracy of these systems. In this perspective, this document describes in detail the hardware implementation of a medical assistance system that can classify PCG phono cardiac signals in two types: normal and abnormal. This system combines two algorithms: an algorithm for the description of the acoustic signal based on discrete wavelets transform and statistical operations, and a classification algorithm based on MLP artificial neural networks. In order to give this system the possibility of being used in real world applications, a hardware implementation was made in the embedded platform FPGA type, this implementation is based on the NIOS II microprocessor and its input-output devices. The results of the hardware implementation of this system have shown that the system is robust, fast and accurate in these decisions.

Keywords: *PCG classification, discrete wavelet transform, artificial neural network, FPGA, NIOS II*

1. INTRODUCTION

Recently, heart disease has been classified among the most common causes of death in the entire world.

Disease or heart defect is a disorder in the rhythm of the heartbeat. In a case of abnormality heart beats rapidly or slowly. In the latter case, the heart does not pump enough blood to all organs of the body [1].

To avoid the dangers caused by these anomalies, pre-surveillance and diagnostic methods are needed to avoid the consequences of these abnormalities or reduce their dangers to human life [2]. The most recognized diagnostic cardiac abnormalities systems are based on either the ECG analysis or the PCG analysis. The analysis of the ECG and PCG plays an important role in automated diagnosis of heart defects and their classifications. The ECG is a recording of electrical potential, generated by the human heart relative to time [3] [4], while the PCG is the recording of the sound signal of cardiac activity.

The PCG signal presents an interest in the diagnosis of cardiac anomalies; this is due to the low cost of obtaining the signal and its accuracy [5]. In this context, radiologists are confronted with several difficulties in sound analysis of the PCG to analyze and identify heart abnormalities. This led to the emergence of intelligent computer systems of medical assistance [6].

In doing so, medical assistance systems require very advanced algorithms for signal processing, which presents problems in the treatment of PCG signals. These problems are due to the difficulty of recognizing abnormal heart rhythms PCG [7].

To remedy these difficulties and provide solutions to these medical assistance systems, this paper discusses the combination of two algorithms to create a fast and robust cardiac signals classification system in detail. These algorithms are divided into two types: a signal processing algorithm and an algorithm of artificial intelligence. The signal processing algorithm is used to extract the characteristics of the PCG signal, based on the discrete wavelet transform. And the algorithm of artificial intelligence is used to detect cardiac abnormalities, such as tachycardia and bradycardia, based on artificial neural networks.

The major problem frequently encountered during the creation of cardiac signals classification

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systems based on complex signal processing and artificial intelligence algorithms is related to their implementation in embedded systems, which are able to maintain the performance of these systems.

Thus, several approaches to hardware implementation of cardiac signals classification systems can be adopted. These approaches are based on microcontrollers and DSP kits [8]. Despite some attempts that have been made in this direction, it was found that the use of the FPGA platform provides advantages compared to microcontrollers and DSP, in terms of speed and cost.

The FPGA is a programmable digital circuit that offers several perspectives for bioinformatics applications. Among these perspectives, the ability to optimizing the material and the parallel processing of data and the transfer of a design made for a specific FPGA device to another with similar capabilities [9].

In this way, the paper discusses in its second part the implementation of the proposed system of classification of cardiac signals. This implementation is based on a NIOS II microprocessor developed by the constructors of the FPGA platform.

This document provides a set of contributions, namely, first the use of discrete wavelet transform with statistical methods for extracting the reduced characteristics of cardiac signals. The second is the use of artificial neural networks such as classifier with the discrete wavelet transform. And the third is to implement the complete classification system in the FPGA platform based on the NIOS II microprocessor.

The paper is organized as follows. The next section details the respective algorithms of signal processing and classification operated in this document. Section 3 describes in detail the various stages of implementation and the experimental results of the classifier used. The last section is devoted to the conclusion.

2. FEATURE EXTRACTION AND CLASSIFICATION ALGORITHMS

This section details the two signal processing and artificial intelligence algorithms used in this document:

- ✓ Discrete wavelet transforms.
- ✓ Artificial neuron network.

In this section, a set of feature vectors of PCG signals is extract by the wavelet descriptor DWT to form a training database and a test database of the ANN classifier MLP type. The PCG signals used in this document are from the MIT BIH database (fig.1) [10].

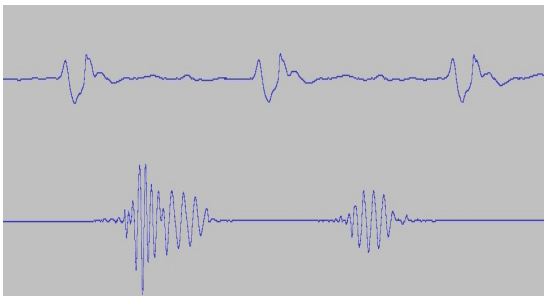

Fig.1. Normal and abnormal PCG

2.1 Discrete wavelet transform

In a speech recognition system, feature extraction is an essential part; the proposed system uses the discrete wavelet transform as feature extractor for the phonocardiogram signal.

The wavelet transform has become a very useful tool to aid medical decision systems, specifically in the classification of cardiac signals [11].

The discrete wavelet transform is an efficient algorithm for signal processing, it has several advantages, including; the evaluation of high frequency using a short time interval and a long time interval for the evaluation of low frequencies. The decomposition efficiency of different scale signals in order to extract the necessary information from the processed signal [12]. And its ease of implementation and optimization of computing time [13].

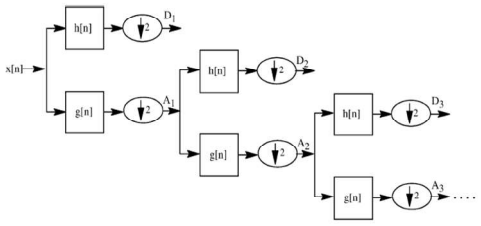

Fig.2. the DWT decomposition

The DWT allows decomposing the input signal at different scales and analyzing with a certain resolution (fig.2) [14]. As shown in the figure, the decomposition process is based on the high-pass filters and low pass filters to extract details Di of the signal and approximations Ai [13]. The decomposition process is an iterative process. During each level, the samples generated by the high-pass filter are completely decomposed; the

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other samples generated by low pass filters will be the entries to the next level [15]. The choice of the wavelet and the number of decomposition levels is performed in a manual way in our application. Satisfactory results were obtained in our case by the Daubechies wavelet to 6 levels.

The decomposition of the phonocardiogram signal using the discrete wavelet transform allows extracting a feature vector in large-dimension, taking into account the size of the PCG signals. This makes recourse to a phase of reduction of size of these vectors. This phase consists in moving from a large vector at a reduced size vector. This reduction is based on statistical functions that are used on the set of wavelet coefficients extracted. The statistical functions used are as follows [16]:

The average values of the coefficients in each sub band.

$$\mu = \frac{1}{N}\sum_{n=1}^{N} X_n \quad (1)$$

The average power of the wavelet coefficients in each sub-band.

$$av = \frac{1}{N}\sum_{n=0}^{N} (X_n)^2 \quad (2)$$

The standard deviation of the coefficients in each sub-band.

$$sd = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \mu)^2}{N}} \quad (3)$$

Each PCG signal, the math functions have reduced the feature vector to 21 features. These vectors therefore constitute the input data of the artificial neural network for learning and classification (fig.3).

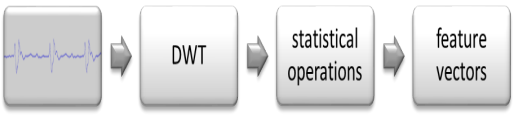

Fig.3.The DWT extraction

2.2 Artificial neuron network

The classification is a process that allows for an unknown pattern at several known classes [17]. The classifier used for the classification of PCG signals is the artificial neural network.

The artificial neural network is a heuristic mathematical model inspired by the human brain diet including how to treat the information [18]. The artificial neural network requires a number of highly interconnected neurons to perform tasks of recognition and classification with a high speed [19].

The artificial neural network follows a critical process for the creation of an architecture dedicated to a specific application, the process used to select the number of hidden layers and the number of neurons in each hidden layer, the learning algorithm, and the choice of the database (training and test).

The construction of artificial neural network of the proposed system of classification of PCG signals follows the following figure (fig.4):

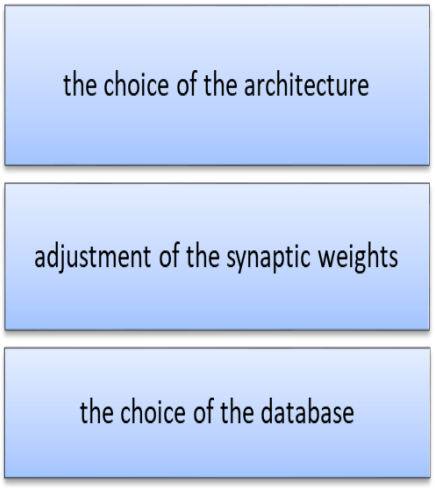

Fig.4. the construction of ANN

The first step is to choose architecture of the artificial neural network, it consists in choosing the number of neurons in each layer and how to interconnect these neurons. The most used architecture in the literature is the multilayer perceptron MLP (fig.5), which will be used in this application. It uses in addition to the input and output layer, the intermediate layers called hidden layers [20].

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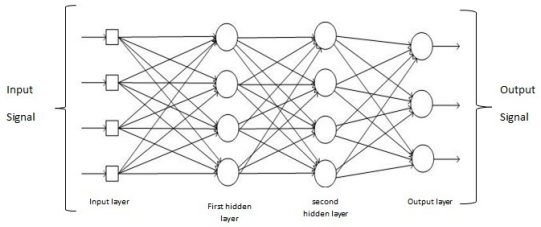

Fig.5. the MLP architecture

The second step fixed the choice of the weight adjustment algorithm for different connections called synaptic weights. The most commonly used algorithm with the multilayer perceptron is the retro-error propagation algorithm (Back pro) that simulates the phenomenon of learning by error [21]. The objective of this algorithm is to minimize the overall error according to gradient descent method described by the following equation (4) [19]:

$$E(n) = \frac{1}{2}\sum_{j\in C}(dj(n) - yj(n))_2 \qquad (4)$$

With: dj(n) is the desired output.

Yj(n) is the current output.

The last step is to use a database to train the proposed classification system of PCG signals. The database contains data labeled for learning and unlabeled data for testing.

In the proposed system, the network learns the different types of PCG (normal and abnormal) from the data set (the training set) and then generalizes their learning to classify the test PCG signals.

3. THE IMPLEMENTATION OF THE CLASSIFICATION SYSTEM

3.1 Introduction to the classification system

The cardiac abnormalities classification system allows to extract firstly the features for learning and secondly to extract the features for classification (decision making).

The learning phase allows the use of DWT to extract the PCG signals features vectors of the MIT BIH database [10]. The artificial neural network receives at its input the database created by these vectors for training to adjust its synaptic weights.

The classification and test phase consists in using the artificial neural network for the classification of PCG signals; the network receives at its input a feature vector extracted by the DWT algorithm representing PCG signal to be processed, and then the network decides whether the PCG signal is normal or abnormal. The following diagram illustrates the overall system of PCG signals classification (fig.6).

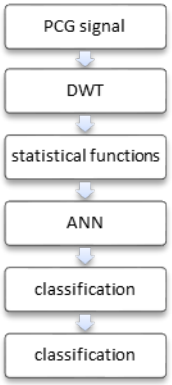

Fig.6. the PCG signal classification system

The database used to test the performance of our PCG classification system is MIT BIH database [10]. This database contains the record of several normal and abnormal patients, and is 30 minutes each.

These signals are decomposed into 1s intervals to extract feature vectors of the same dimension. Then these signals have created a learning base (fig.7) 480 examples and a test database of 109 examples.

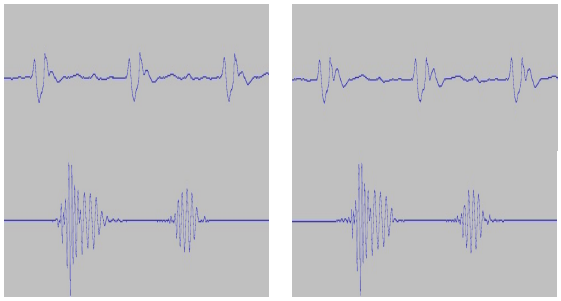

Fig.7. the PCG signal learning database

3.2 The implementation tools

The objective of this document is to implement the PCG classification system in the FPGA platform; this implementation is based on the use of softocore NIOS II microprocessor.

This section is devoted to describing the various stages and modules necessary for the implementation of the proposed classification system.

a. FPGA

The field programmable gate array is integrated circuits used for the implementation and design of complex circuits. The FPGA contains three types of resources (fig.8): logic blocks, inputs outputs and programmable interconnects. [22] In addition the

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FPGA is composed of look up table (LUT) and latches in order to program more or less complex logic functions.

The FPGA device offers several advantages, including the parallel processing of data, which provides the ability to implement complex digital functions, the execution of complex functions with speed, and flexibility, and the possibility to exploit a single FPGA chip in many electronic systems [23].

The language frequently used to develop applications in the FPGA boards is the hardware description language VHSIC Hardware Description Language (VHDL) or Verilog and the software of this description is specific software named Quartus [23].

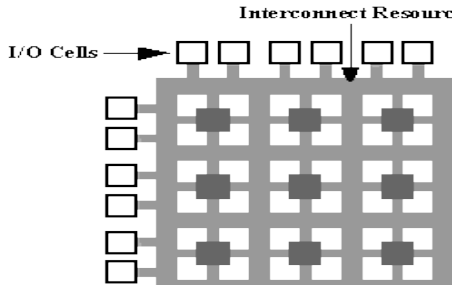

Fig.8. Logic cell array architecture of FPGA

b. NIOS II

The NIOS II (fig.9) is an embedded processor from the FPGA Altera family dedicated to a variety of embedded applications in various fields [24]. This is a 32 bit microprocessor with an internal architecture HARVARD and a RISC instruction set. The NIOS II contains 32 general registers and six special purpose registers. Thus, the NIOS II has several features including a synchronous interface, 6 pipeline levels, a clock frequency which can reach 200MHz and performance that varies between 30 and 80 MIPS (Million Instructions per Second) [25] [26].

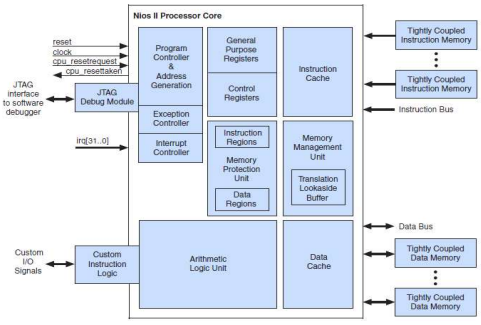

Fig.9. NIOS II processor

3.3 Implementation of the proposed classification system

The implementation of the classification system of the PCG signals in the FPGA platform based on the NIOS II can improve design efficiency on the FPGA platform and reduce complexity.

This implementation is divided into 2 stages:

a. Hardware part

The development of application based on NIOS II microprocessor requires two development tools: QUARTUS and SOPC Builder.

The QUARTUS II design software from Altera provides a comprehensive and multi-platform environment in order to easily design any application. Thus The Quartus offers solutions for all phases to design an application [27].

The SOPC Builder development tool is a new concept for embedded system. The SOPC is a tool characterized by the flexible design, adaptation to the application, extension, scalability and software and hardware programming, which helps the evolution of the technology design assisted by computer [23].

The implementation of our PCG classification system requires in addition to the NIOS II, other input output peripherals that help the proper functioning of the system.

Among these devices: the 7 segment display, audio controller, sdcard controller, SDRAM, LCD display, the LEDs and the Switches. The following diagram (fig.10) illustrates the implementation of the classification system.

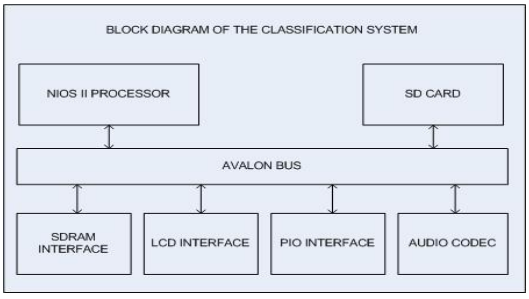

Fig.10. the block diagram of the PCG classification system

The system uses the DE2_70 platform to develop a classification system of PCG signal; this system is based on reading data streams from the SD card in play mode, and the chip used is the Cyclone II EP2C70F896C6.

The figure shows the hardware implementation of the classification system of the PCG signal. The

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system is based on the SD CARD interface; it allows connecting the SD CARD with the NIOS II to convert audio files in a data flow that will be used later. The SD CARD interface is provided by connecting pin 4 PIO to SD CARD. The system uses an SDRAM interface to provide a storage area for the data stream.

In this design, the system performs two tasks. The first task is to provide the data to the audio controller. This controller requires an input clock that operates at 18.432 MHz frequency, which is generated by the PLL block, and an I2C interface to control data stream [28]. The second task is to process data in parallel with the first task, using the respective signal processing algorithms (Discrete Wavelet Transform) and artificial intelligence (Artificial Neural Network) to classify the PCG signal.

The 7-segment display and LCD are controlled respectively by the 7 segments controller and the LCD interface to display the information on the track or the type of PCG signal to be processed and the classification result.

The following figure shows the overall system generated by the SOPC Builder (fig.11).

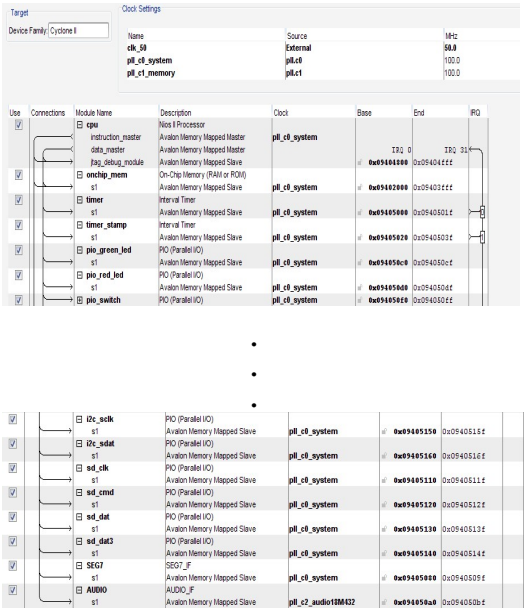

Fig.11. the SOPC builder system

The SOPC Builder generates as a result of compiling a single module (Fig.12) which is added to the component library of the FPGA. This module which is composed of NIOS II and its peripherals is equivalent to a microcontroller that has its own set of instructions which will be programmed later in the classification of PCG signals using a programming language such as C language.

Fig.12. the block design of the proposed system

After the integration of the system with these devices, a JTAG UART interface is used to connect the NIOS II system on the host computer to the DE2_70 FPGA board via USB [29].

b. Software part

The software development tool is the NIOS IDE; it is a tool that is based on Eclipse altera including a compiler and assembler available for NIOS II processor. The development languages used by the NIOS IDE are C, C ++ and assembler [30].

The system implements multiple blocks as shown in the figure, among these blocks (fig.13):

- ✓ SD card driver implements the drivers of the sdcard for the detection of the sdcard and reading the data.
- ✓ The FAT block 16 implements the FAT16 file system to play audio files from sdcard.
- ✓ The WAVE lib block allows the decoding the audio file stored in WAVE format.
- ✓ The I2C and audio blocks used to implement the I2C protocol and audio code to send audio codec and configure the audio interface (the size of the channel, sample rate and mode of operation of the audio chip) [29].

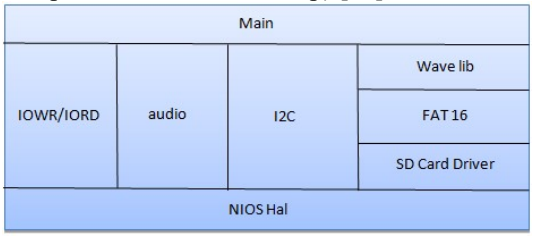

Fig.13. NIOS II combination with the devices

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The figure (fig.14) shows the functioning of our classification system of PCG signals based on the NIOS II microprocessor, the first step performed by the NIOS II is to detect the presence of the SD card. Once the SD card enabled, the files in the SD card are listed in FAT 16 format. The type of audio files used in our system is WAV files. After this operation the LCD display of the DE2_70 board displays the names of files, and the ability to select the signal to be processed while using the switches and the Keys [29].

The following step is a critical step in our system. Once the PCG signal to be processed is selected, the DWT algorithm converts the signal into a vector feature. This signal will be the input of artificial neural network, which will classify it according to its nature (normal or abnormal).

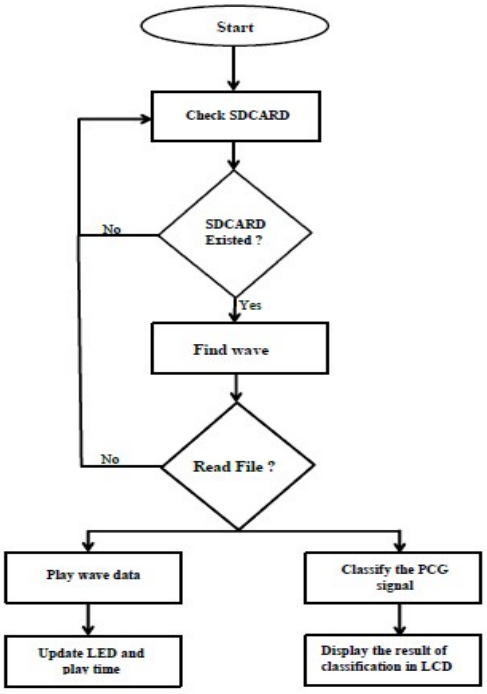

Fig.14. the global PCG classification system

4. RESULTS AND DISCUSSION

In this section, the implementation of our PCG signals classification system will be simulated and tested in the FPGA DE2_70 EP2C70F896C6 release (Fig.15). This section will be dedicated to collecting some performance indicators of the proposed system are: the correct classification rate (DC), the execution time (TE), material resources employed and the evolution of the squared error.

Fig.15. Altera DE2_70

Regarding the first three indicators, we have performed the test with an architecture implemented on the NIOS II software Software Build Tools for Eclipse and consist of:

- ✓ 21 neurons in the input layer, which corresponds to the number of feature vector parameters extracted by the DWT algorithm.
- ✓ 32 neurons in the hidden layer.
- ✓ 2 neurons in the output layer representing classes of PCG signal (normal or abnormal).

The experimental results collected show that:

The rate of correct classification of the PCG signals could reach a rate of 96,33% for optimal neural architecture. This is due to the relevance of features extracted by DWT descriptor and also the efficiency of ANN.

The test also allowed taking a collect of material resources and execution times of our PCG signal classification system. These results are illustrated in the following figure (fig.16):

Family	Cyclone II
Device	EP2C70F896C6
Timing Models	Final
Met timing requirements	N/A
Total logic elements	6,080 / 68,416 (9 %)
Total combinational functions	5,108 / 68,416 (7 %)
Dedicated logic registers	3,704 / 68,416 (5 %)
Total registers	3842
Total pins	538 / 622 (86 %)
Total virtual pins	0
Total memory bits	147,392 / 1,152,000 (13 %)
Embedded Multiplier 9-bit elements	4 / 300 (1 %)
Total PLLs	1 / 4 (25 %)

Fig.16. the hardware result

The results obtained during the implementation of the classification system of PCG signal in the FPGA-based on microprocessor NIOS II can show the performance of system in terms of hardware capabilities and execution time.

The implementation of the proposed system in the FPGA platform has consumed few material resources (fig.16) and that is due to the use of the

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NIOS II whose material resources are optimized by designers from Altera and which also gives the possibility of implementing the algorithms of treatment as a code written in C without recourse to other additional hardware resources.

For the execution time, the implementation has undeniable advantages in terms of computing speed, reaching 0.13 s; this is due to the optimization of neuronal and hardware system.

As for the collection of the square error, the test was done using two methods:

- ✓ The variation in the number of iterations for each fixed ANN architecture (fig.17).

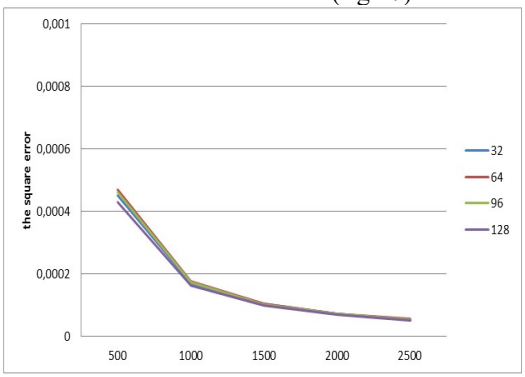

Fig.17. the variation of the iterations number

- ✓ The variation of the ANN architecture for each fixed number of iteration (fig.18).

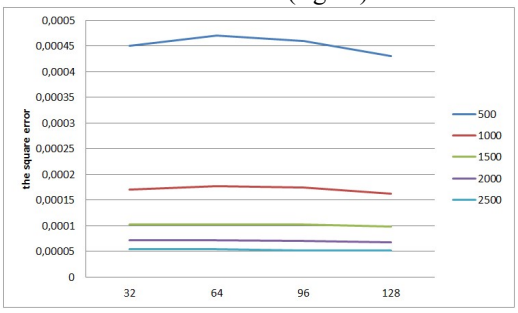

Fig.18. the variation of the ANN architecture

The results of the first method are illustrated on (fig.17) and which allow remarking that to increase or decrease the number of iterations eventually has an impact on the value of the square error and that it varies an inverse proportion to the number of iterations. These results are evident because the RNA will be enough time when the number of iteration is important to adjust its synaptic weights and converge to their optimal values.

The results of the second method are illustrated on (fig.18). They show that the variation of ANN architectures for a fixed number of iterations did not significantly influence the value of the squared error, because all tested architectures are optimal solutions to this classification and also the number of classes of this particular binary classification (normal and abnormal).

5. CONCLUSION

This article has proposed a medical assistance system implemented in the FPGA platform that can classify PCG signals into two classes (normal and abnormal). This system is based on the combination of efficient algorithms in terms of signal processing (reduced discrete wavelet transform) and in terms of artificial intelligence (the artificial neural network multilayer perceptron type). Moreover, the implementation of this system has given very satisfactory experimental results in terms of correct classification rate DC and in terms of execution time TE.

However, the future work will focus on the contribution of improvements in this single-object detection system (PCG normal, abnormal PCG) to make it a multi-object classification system (normal, tachycardia, bradycardia, etc.) robust, fast and usable in real applications.

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