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# HARDWARE IMPLEMENTATION OF DIGITAL IMAGE CODING USING FDCT

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### ABSTRACT

Image coding becomes an interested issue for its extensive use in wide range of applications. This work deals with the Fast approaches of hardware implementation for Forward Discrete Cosine Transform (FDCT) and the Inverse Discrete Cosine Transform (IDCT). These approaches are normally used for image coding and decoding applications. The implemented approaches are built using hardware design with specific control parameters to speed up the processing. The implemented approach based on one dimensional Discrete Cosine Transform (ID-DCT) and fast transposing through high access memory that offer real time operation. The control system of flow of pixels is built to have two principal processing of rows and columns and the flow of coefficients comes from high speed access memory. The implementation of the system is done to achieve high speed and accurate results. The differences between the original image and the recovered image for all tested sizes are very small and it is about 10<sup>-16</sup>.

Keywords: FDCT, IDCT, Image Coding, Image Decoding.

### 1. INTRODUCTION

Nowadays digital signal and image processing have important applications especially in industry [1,2], communications, robotics, computer vision, radio, Television and many other military and civil applications [3,4]. Image coding and decoding are denoted as an important fields of image processing [5,6,7,8]. Most of the published works at this filed are concentrated the accurate results and real time processing [9,10].

Digital representation of images offers many benefits but required big amount of data for representation [11,12]. On the other hand this open new issues to be considered such as storage devices and operating speed [13,14]. Therefore the reduction of data is an important solution to be implemented to make handling of high resolution digital images [15,16].

Several techniques and methods are explained to view the benefits of the fields of compression and coding [17,18]. Some techniques are simple that give low compression, other techniques are powerful and expensive [19,20]. Anyhow the relation between cost and quality is an important issue [21,22]. Considering a specific parameters for mixing between hardware and software are very important to design an image processing system [23,24].

Most of the implemented transform coding techniques using discrete cosine transform give significant compression with reasonable cost and quality [25,26]. Image coding leading to represent images using few number of bits as possible [27,28]. This operation have many applications in reduction of channel bandwidth required for image transmission and storage devices [29,30].

### 2. RESEARCH OBJECTIVE

The hardware implementation of digital image processing play an important role in many applications, including image coding applications. So this research discovered that large number of papers have been published on this subject. The aim of this work is to study the digital image coding technique applied on images using discrete cosine transform. Then this work try to address the design of an efficient approach of hardware implementation of digital image coding using fast discrete cosine transform and study the coefficients of both DCT and IDCT. So the main objective of this research is to offer an efficient image coding approach to achieve high accuracy and high speed.

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harmonically-related

cosine functions [34].

signals.

Digital

3. DISCRETE COSINE TRANSFORM

The Discrete Fourier Transform (DFT) [31] and Discrete Cosine Transform (DCT) [32] perform

similar functions: they both decompose a finite-

length discrete-time vector into a sum of scaledand-shifted basis functions [33]. The difference between the two is the type of basis function used by each transform; the DFT uses a set of

functions, while the DCT uses only (real-valued)

Figure 1 shows both one dimensional Forward

Discrete Cosine Transform (1D-FDCT) and one

dimensional Inverse Discrete Cosine Transform

(1D-IDCT) that are used for coding and decoding of

1D Forward

complex

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exponential

Digital

1620

(2D-IDCT) that are used for coding and decoding of two dimensional signals such as images.

The forward 2D-DCT is given by the following equation [39,40]:

$$\begin{array}{l} x(k1, k2) = \\ c(k1)c(k2) \sum_{n=0}^{N-1} \sum_{n=0}^{N-1} x(n1, n2) \cos\left[\frac{(1n1+1)k(n)}{2N}\right] \cos\left[\frac{(2n2+1)k(n)}{2N}\right] \\ (4) \end{array}$$

Where X(k1,k2) is the output square matrix coefficients values, x(n1,n2) is the input square matrix data values, N is the number of discrete values (rows and columns), (n1,n2) are the indices of the input values, (k1,k2) are the indices of the output values.

The inverse 2D-DCT is given by the following equation [41,42]:

$$\frac{X(k1, k2)}{\sum_{n=0}^{N-4} \sum_{n=0}^{N-4} o(k1) o(k2) x(n1, n2) \cos\left[\frac{(2n1+1)k1\pi}{eN}\right] \cos\left[\frac{(2n1+1)k1\pi}{eN}\right]}{(5)}$$

Where

$$c(k1) = \begin{bmatrix} \sqrt{1/N} f \text{ or } k1 - 0 \\ \sqrt{2/N} f \text{ or } k1 = 1, 2, \dots N - 1 \end{bmatrix}$$
(6)  
$$c(k2) = \begin{bmatrix} \sqrt{1/N} f \text{ or } k2 = 0 \\ \sqrt{2/N} f \text{ or } k2 - 1, 2, \dots N - 1 \end{bmatrix}$$
(7)



Figure 2 two dimensional discrete cosine transform

### 4. RELATED WORK

According to the huge amount of publications in this field, it is impossible to recover all the aspects of these publications. In this item some concentration on the most recent publications:

Input Signal Digital Coded Signal 1D Inverse Coded Signal Digital Coded Signal Digital Signal Signal Digital Signal Signa

Figure 1 one dimensional discrete cosine transform

The forward 1D-DCT is given by the following equation [35,36]:

$$X(k) = \sigma(k) \sum_{n=0}^{N-1} x(n) \cos[\frac{(2n+1)k\pi}{2N}]$$
(1)

Where X(k) is the output coefficients values, x(n) is the input data values, N is the number of discrete values, n is the index of the input values, k is the index of the output values.

The inverse 1D-DCT is given by the following equation [37,38]:

$$x(n) = \sum_{k=0}^{N-1} c(k) X(k) \cos[\frac{(n+1)k\pi}{n}]$$
(2)

Where

$$c(k) = \begin{bmatrix} \sqrt{1/N} \text{ for } k = 0\\ \sqrt{2/N} \text{ for } k = 1, 2, \dots N - 1 \end{bmatrix}$$
(3)

Figure 2 shows both two dimensional Forward Discrete Cosine Transform (2D-FDCT) and two dimensional Inverse Discrete Cosine Transform



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T. C. Tan et al. (2001), proposed a fast DCT algorithm that mapped to a hardware structure composed of log2N modules. This hardware structure can be used for serial bit or serial implementation of bit serial. Compared to other hardware deployment methods, the project provides a natural interface to sequentially submitted input data, enables high hardware utilization, requires low latency processing, and has a modular architecture that can be extended to support different processing sizes [43].

Tang Li (2004), optimized a technique based on the conservation of DCT energy assets, for motion estimation, DCT and quantification of standard video encoders developed. Firstly, proposed a stop criterion for motion estimation to reduce the number of control points to find the motion vectors and save the calculations. The advantage of introducing this stopping criterion lies in its adaptability to the quantization parameter and the applicability to various fast algorithms. Next, the DCT and the quantification are optimized together by plotting the remaining signal energy and eliminating unnecessary calculations in the DCT process and quantification. 2D-DCT based on DCT's fast Huang algorithm is presented to demonstrate the superiority of this algorithm to full DCT and a completely zero total block detection method. Although this approach is computationally efficient,, the algorithms do not indicate any obvious loss of quality [44].

Yi-Ming Zhou (2009), improved the coding of fractal images by provided efficient algorithms for encoding fractal images using a special unified feature and a DCT encoder. Depending on a necessary condition for the most appropriate search rule in fractal image coding, it treats the fast algorithm that uses a special unified function and can reduce the lookup space of course and exclude the sub-locks coincidences more inappropriate before the best matches. In order to improve the quality of the reconstructed image, a DCT encoder is combined to construct a hybrid fractal image algorithm. The experimental results show that the proposed algorithms can obtain reconstructed images of good quality and require much less time than the basic algorithm of fractal coding [45].

Hui Li et al. (2010), explained an inverse modified discrete cosine transform (IMDCT) approach and an efficient hardware accelerator architecture. The proposed fast algorithm is derived from the discrete cosine algorithm type IV transformed into discrete sine cosine Type IV. After the transformations, the computational elements continue to be recombined to share hardware resources. The experimental results show that the calculation cycles of the proposed algorithm are reduced by 20% and 51%, respectively, compared to two other fast algorithms reported. Using resource sharing and multiplexing techniques, the proposed hardware accelerator reduces 24% and 48% of transistors compared to two other methods respectively [46].

K. Viswanath et al. (2011), implemented an approach of image filtering in the transformation domain using a symmetric convolution in the DCT block space. Due to the application of the convolution multiplication property in the DCT domain, the filtering operation requires much less computation than its equivalent in the original signal and image space. To care for discontinuities along the boundaries of the blocks, the filtering is performed on a larger DCT block composed of adjacent blocks. Subsequently, the filtered DCT block is obtained by decomposing it. The proposed filtering technique achieves the same results of linear convolution in the space domain with a reduced cost. With the proposed filtering, it is possible to considerably accelerate the operation by ignoring certain elements in the filter matrices whose magnitudes are less than a threshold value. The standard deviation of the input blocks of the DCT domain is also taken into account for an additional reduction in the calculation cost [47].

Zhongwei He et al. (2012), proposed Markov-based approach to detect this specific artifact. First, the original Markov characteristics generated from transition probability matrices in the DCT domain is developed to capture not only the intra-block correlation but also inter-blocks between the DCT coefficients of the block. Then more functionalities are constructed in the DWT domain to characterize the three types of dependence between wavelet coefficients between positions, scales and orientations. Then, the support vector machine entity selection method is used to perform the task of reducing functionality, which facilitates the management of calculation costs. Finally, the support vector machine (SVM) is exploited to classify authentic and spliced images using the reduced final functionality vector. The results of the experiment demonstrate that the proposed approach can overcome some of the more advanced methods [48].

Lech Jóźwiak, Yahya Jan (2013), described a new multiprocessor based multiprocessor accelerator

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design methodology that addresses the architectural design challenges of multiprocessor processors for highly demanding embedded applications. Using the LDPC decoder design for the latest high-speed communication system standards as an application example that conducted extensive experimental research on multiprocessor design issues, as well as methodology and design framework. The experiments clearly demonstrated the existence of several complex architectural compromises that could only be solved by a spatial exploration of a combined quality design adapted to the micro and macro architects of the processors and the corresponding memory and communication architectures are provided by our method [49].

Hai Huang, Liyi Xiao (2014), designed a reconfigurable segmented processor for FFT / IFFT and DCT / IDCT calculations over a variable length variable length distance compatible with IEEE 754. This approach minimized storage and power consumption, a reconfigurable radix-4 butterfly to reduce the adders by 75% compared to the conventional butterfly radix-4 parallel and bank structured partly-shared records ping-pong provided cache mechanism ultimate data effective and specific means to achieve maximum utilization ratio of the resources adder and to ensure high performance for the pipeline design. The 4 input points adder merged point unit and the point to the floating product 2 input points are proposed, which can not only improve a signal to noise ratio by 3 dB, but also save 28% above in equipment compared to discrete implementations. The simulation results show that the latency for FFT calculations is approximately 25% of the design without loss of performance, and it reaches more than 139 dB SONR [50].

Abdessalem Ben Abdelali et al. (2016), presented a hardware design for the discrete forward cosine transform (BinDCT) and its application in a programmable matrix grid array device. Different architectures of the module have been explored to ensure maximum efficiency. The development of these architectures included architectural design, timing and pipeline analysis, hardware description synthesis language modeling, design and implementation. The developed hardware module has a high efficiency in terms of operating frequency and material resources, which made it suitable for the latest video standards with high resolution image and refresh rate. A high hardware efficiency will make it a very good candidate for time-limited applications and resources. Compared

to several recent implementations of discrete cosine transform approximations, it has been shown that the proposed module has the best performance [51].

D. Ravì et al. (2016), implemented an approach for generating specific segmented segments. We present two new features that use the quantified data of discrete cosine transformation in a Semantic Texton Forest (STF), combining color and texture information for semantic segmentation. The combination of multiple features in a segmentation system is not a simple process. The proposed system is designed to exploit complementary functionalities in a computationally efficient way. functions describe complex These textures represented in the frequency domain and not just simple textures obtained using differences in pixel intensity as in the conventional approach. Unlike existing methods, a limited amount of resources is required. The proposed method was tested in two popular databases: CamVid and MSRC-v2. The comparison with the recent advanced methods shows an improvement in the precision of the semantic segmentation [52].

C. J. Tablada et al. (2017), proposed two approaches of DCT with 8 points without multiplication based on the factorization of Chen and their fast algorithms are also derived. Both transformations are evaluated in terms of calculation cost, error energy and coding gain. Experiments are performed with a JPEG image compression system and the results are compared with competing methods. The proposed low complexity transforms are scaled according to the algorithm for 16 and 32 points approximations. The new transformation sets are integrated into the HEVC reference software to provide a fully compliant HEVC video encoding scheme. The approximate transformations can overcome traditional transformations and advanced methods at a very low cost of complexity [53].

Daniel Llamocca (2017), implemented a new methodology by recovering similar models known for graphics and isomorphic interconnections as hardware accelerators in the system design. It has been proposed an efficient approach that converges in polynomial time to find similar subgraphs. Then, an algorithm has been proposed to perform cluster programming and minimizing the overhead. All algorithms were written in Python to analyze the description of the data flow and check the accuracy of the proposed works. The proposed design flow was applied to five different programs that are sine,

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cosine, exponent, matrix multiplication and discrete cosine transform. These were described as a flow chart data and were used for comparison of the results. An estimation table has been developed that shows the hardware and software parameters of the data flow operators for the chronology and the analysis of the program area [54].

According to these related works, it is clear that these works are concentrated on study the design of algorithms to implement both DCT and IDCT. This approach try to implement a real time approach to perform the performance as well as the accuracy of the implemented algorithm. The proposed approach try to design and implement an efficient fast digital image coding using DCT and IDCT.

# 5. METHOGOLOGY

The methodology of this approach is concentrated on design and implementation of fast image coding. This methodology is explained in detailed in the following items.

# 5.1 Design Consideration

The design of the system is built to carry out fast processing issue through multiplications, additions and transposing operations via DCT function. The main idea of the operation is the partitioning of two dimensional matrix into set of rows that means 2D-DCT can be implemented via 1D-DCT of rows and columns respectively, and also it is true for 2D-IDCT.

Before implementing this approach, some notes must considered, these are as below:

- The first point is the dimension of the selected matrix it must be square matrix in order to avoid the complexity.
- The second point is the length of rows and columns of the selected matrix must be 2 to the power of integer that leads to fast processing.
- The third point is the selection of the weighting factors in both forward and inverse DCT in which the weighting factors are divided for both cases which are clear from equations 3, 6 and 7.

### 5.2 DCT System Implementation

The steps of the procedure of the DCT system implementation are explained as below (figure 3):

Coefficients calculation for both DCT and IDCT that generates the matrix multiplier with the input image matrix.

Transposing operation is implemented through the multiplication process by controlling the addresses of memory using programmable counter.

The timing controller generator is used to control the overall processing of the system via dividing the time according to the required process.



Figure 3 DCT system implementation

The multiplier is constructed of two chips of 16 bits SN54157A (considering the image data of eight bits per pixel). The multiplier output control is shown in figure 4 in which there are two main outputs; the first output is the low significant bits LSB (7:0) and the second output is the most significant bits MSB (15:8). LSB (7:0) is the normal output part and go directly to the output in case of the output values within 255. On the other hand when the output values exceed the value of 255, in this case there is an existing data at the part MSB (15:8).

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#### **RESULTS AND DISCUSION** 6.

The DCT coefficients are shown in table 1 and demonstrated in figure 5. These coefficients can be used to implement the image coding approach according to direct reading of these coefficients. On the other hand the IDCT coefficients are shown in table 2 and demonstrated in figure 6. These inverse coefficients can be also used to implement the image decoding approach according to direct reading of these inverse coefficients.

According to these two tables it is clear that the IDCT coefficient are the transposed matrix of DCT coefficients in which can be simply applied via the implemented system within the sequence to serve the processing via the timing control. It is clear that there is a similarity between these two set of coefficients, so it can be used in bidirectional for image coding and image decoding.

|    | C1  | C2   | C3   | C4   | C5   | C6   | C7   | C8   |
|----|-----|------|------|------|------|------|------|------|
| R1 | 256 | 256  | 256  | 256  | 256  | 256  | 256  | 256  |
| R2 | 355 | 301  | 201  | 71   | -71  | -201 | -301 | -355 |
| R3 | 335 | 139  | -139 | -335 | -335 | -139 | 139  | 335  |
| R4 | 301 | -71  | -355 | -201 | 201  | 355  | 71   | 301  |
| R5 | 256 | -256 | -256 | 256  | 256  | -256 | -256 | 256  |
| R6 | 201 | -355 | 71   | 301  | -301 | -71  | 355  | 201  |
| R7 | 139 | -355 | 335  | -139 | -139 | 335  | -335 | 139  |
| R8 | 71  | -201 | 301  | -355 | 355  | -301 | 201  | -71  |
|    |     |      |      |      |      |      |      |      |

Table 1 coefficients of DCT

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Figure 5 coefficients of DCT

Table 2 coefficients of IDCT

|    | C1  | C2   | C3   | C4   | C5   | C6   | C7   | C8   |  |
|----|-----|------|------|------|------|------|------|------|--|
| R1 | 256 | 355  | 335  | 301  | 256  | 201  | 139  | 71   |  |
| R2 | 256 | 301  | 139  | -71  | -256 | -355 | -355 | -201 |  |
| R3 | 256 | 201  | -139 | -355 | -256 | 71   | 335  | 301  |  |
| R4 | 256 | 71   | -335 | -201 | 256  | 301  | -139 | -355 |  |
| R5 | 256 | -71  | -335 | 201  | 256  | -301 | -139 | 355  |  |
| R6 | 256 | -201 | -139 | 355  | -256 | -71  | 355  | -301 |  |
| R7 | 256 | -301 | 139  | 71   | -256 | 355  | -335 | 201  |  |
| R8 | 256 | -355 | 335  | 301  | 256  | 201  | 139  | -71  |  |
|    |     |      |      |      |      |      |      |      |  |



Figure 6 coefficients of IDCT

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This approach is implemented on different images of water pollution that collected from real test of water pollution. All original images are of high resolution and of size 1920\*2560. Then these images are resizing into three main types 256\*256, 512\*512 and 1024\*1024. The first original image and its histogram are shown in figure 7, in which the original image is shown in figure 7a and then apply histogram operation to demonstrate the distribution of pixels as shown in figure 7b. The resizing stage is applied to all images to be ready for processing. Figures 8, 9 and 10 demonstrate the resized images of 256\*256, 512\*512 and 1024\*1024 with their histogram respectively.



(a) Grayscale original image



(b) Histogram of image in (a) Figure 7 first original image and its histogram (1920\*2560)



(a) Grayscale of original image



(b) Histogram of image (a) Figure 8 first original image and its histogram (1024\*1024)



(a) Grayscale of original image

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(b) Histogram of image (a) Figure 9 first original image and its histogram (512\*512)



(a) Grayscale of original image



(b) Histogram of image (a) Figure 10 first original image and its histogram (256\*256)

On the other hand DCT process is applied on the original images to encrypt these images, then IDCT is applied on the output of DCT to recover the image. Figure 11 shows the first original image after resized into 256\*256, in which it is clear that this image has been encrypted into a new environment that is impossible to distinguish the details of the original image. After that applying IDCT approach to recover the original image as shown at the same figure. Comparing input and output images leading to high similarity and quality between original image and the recovered image, in addition that the compressed image occupied low space of size. The difference between the original image and the recovered image is very small and it is about  $10^{-16}$ .



Figure 11 first original image and its DCT (256\*256)

Figure 12 shows the first original image after resized into 512\*512, in which it is clear that this image has been encrypted into a new environment. The difference between the original image and the recovered image is very small and it is about  $10^{-16}$ .



Figure 12 first original image and its DCT (512\*512)

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Figure 13 shows the first original image after resized into 1024\*1024, in which it is clear that this image has been encrypted into a new environment. The difference between the original image and the recovered image is very small and it is about  $10^{-16}$ .



Figure 13 first original image and its DCT (1024\*1024)

Figure 14, 15 and 16 show the second original image after resized into 256\*256, 512\*512 and 1024\*1024 respectively, in which it is clear that this image has been encrypted into a new environment. Comparing input and output images leading to high similarity between original image and the recovered image, in addition that the compressed image occupied low space of size. The differences between the original image and the recovered image for all tested sizes are very small and it is about 10<sup>-16</sup>.



Figure 14 second original image and its DCT (256\*256)



Figure 15 second original image and its DCT (512\*512)



Figure 16 second original image and its DCT (1024\*1024)

PSNR is the peak signal-to-noise ratio in decibels (dB). Figure 17 shows the PSNR values of the four tested images within the three sizes. This figure shows that the values of PSNR is around 40 dB and there is small increment with the increase of the image size.

The mean square error (MSE) is the squared norm of the difference between the input image and the recovered image divided by the number of elements. Figure 18 shows the MSE values of all tested images. These values are ranged from 13 to 5 according to the increment in the image size.

MAXERR is the maximum absolute squared deviation of the input image and recovered image. Figure 19 shows MAXERR values in which varied from 20 to 50 according to the contains of the image.

L2RAT is the ratio of the squared norm of the recovered image to the input image. Figure 20 shows L2RAT values in which varied from 0.9996 to 0.9999 depends on the image size.

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Figure 18 MSE values







Figure 20 L2RAT values

### 7. CONCLUSIONS

Algorithms can be implemented via software hardware forms. Software or implementation is very important to achieve flexibility. Hardware implementation is very important to achieve real time processing and transmission. Two dimensional discrete cosine transform is an important technique for image coding operation. The implemented approach combined both forward and inverse discrete cosine transform. The implemented approach used high speed components to achieve the real time image coding processing. The overall system is simulated to obtain a good results for both forward and inverse discrete cosine transform applied for image coding. The recovered image guarantee high performance of the retrieved images. The differences between the original image and the recovered image for all tested sizes are very small and it is about 10<sup>-16</sup>. At this accuracy, this approach can achieve high accuracy and high speed of processing that can be matched with the mentioned objectives.

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