

REAL-TIME HARDWARE ARCHITECTURE OF THE ADAPTIVE DUAL THRESHOLD FILTER BASED ECG SIGNAL DENOISING

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ABSTRACT

This paper presents a hardware architecture of the Adaptive Dual Threshold Filter (ADTF). This architecture leads to real-time process of the ECG signal denoising. The ADTF is a recent technique that offers a simple and efficient algorithm of the ECG signal denoising. The implementation of the ADTF is based on a structural VHDL description of different functional blocks. The overall architecture was designed and parallelized in order to accelerate processing. Results of this architecture design show high performances of the real-time denoising process of the ECG signal. The proposed architecture presents a low complexity and a low occupancy of the various resources of an FPGA architecture based low-cost systems presented in this research work.

Keywords: *Electrocardiogram, VHDL, Real-Time, ADTF, FPGA, Low-Cost Systems*

1. INTRODUCTION

The electrical activity of the heart muscle is represented by the electrocardiogram signal (ECG) [1-2]. This activity is collected on a patient by electrodes placed on the surface of the skin. These electrodes record the electrical signals in at least twelve branches, six in the frontal plane (frontal electrodes) and six in the horizontal plane (precordial electrodes) [3]. The ECG is an essential element in patient monitoring as well as the diagnosis of cardiovascular disease. The bases of the ECG signal recording were stated by Einthoven [4-5].

The ECG signal is a signal rich in the variety of waves that constitute it (P and T waves and the QRS complex). Thus, it has a power spectral density which varies as a function of the signal morphology [6-7]. The ECG signal is characterized by a small frequency range (0.05 Hz-150 Hz), which makes this signal weak in front of different types of noises [8]. These noises affect the ECG signal over the width of its frequency range, which makes the ECG signal denoising a complex task.

Several methods have been developed to deal with the denoising task of the ECG signal, such as the Discrete Wavelet Transform (DWT) [9-10], the

Empirical Mode Decomposition (EMD) [11-12], the Ensemble Empirical Mode Decomposition (EEMD) [13-14] and recently the Adaptive Dual Threshold Filter (ADTF) [15-16]. The major disadvantage of convolution-based linear filters (e. g. DWT) is that noise reduction is accompanied by a transition propagation between regions. In addition, the problem of selecting the wavelet function for a particular operation persists [17]. The EMD technique lacks of robustness to small perturbation. This is due to the problem of mode mixing that appears in the different IMFs [18]. This issue is overcome using the EEMD approach, but the complexity of this approach is more important.

We have proposed recently a novel approach of the Adaptive Dual Threshold Filter (ADTF) [15-16]. This approach has been inspired by the adaptive dual threshold median filter by V. Gupta [19]. The aim of the ADTF technique is the filtering of the high frequency noises of the ECG signal using a low complexity process. The results proposed by the ADTF approach are very ambitious comparing to recently proposed techniques using the EMD and the EEMD approaches [15-16].

Nowadays, embedded architectures are emerging in a remarkable way in the different research fields

of the biomedical engineering. We specify the development of a cardiac data monitoring system using embedded hardware. Several researches have been proposed in the different axes of this research field e. g. ECG signal denoising [20] and ECG signal features extraction [21]. One of the embedded architectures widely used in the different engineering fields is the Field-Programmable Gate Array (FPGA). FPGAs are reconfigurable VLSI components, which allows them to be reprogrammable at will in order to speed up some phases of computation. The advantage of this type of circuit is its great flexibility, which makes it possible to reuse them at will in different algorithms implementation [22]. Design of FPGA based architecture is achieved using the High Level Synthesis tools (HLS) or the Hardware Description Language (HDL) e. g. VHDL, Verilog and systemC.

This paper proposes a hardware architecture of the Adaptive Dual Threshold Filter (ADTF) for a real-time process of the ECG signal denoising. The proposed architecture is designed for an implementation over different FPGAs. We propose a VHDL implementation in order to optimise and to simplify the proposed architecture. This design is based on a structural VHDL description of the different functional blocks. The overall architecture was designed and parallelized in order to accelerate processing.

The next section presents the Adaptive Dual Threshold Filter (ADTF) and its complexity. The second section presents the VHDL implementation of the ADTF. Following, the results and discussion section shows and discuss the different results, whether qualitative or statistical as well as the comparison of the results with those of the ADTF software-based implementation. Finally, the last section concludes this paper.

2. ADAPTIVE DUAL THRESHOLD FILTER

The Adaptive Dual Threshold Filter (ADTF) is a non-linear filter for denoising the ECG signal. The theoretical bases of this filter have been inspired by the recently published adaptive dual threshold median filter [19]. This method offers an important solution for image denoising. In single-threshold filters, any pixel with a lower value (eg, low-pass filter) or higher value (eg, high-pass filter) than the single threshold value, is considered as a noise. This may increase the possibility of incorrect noise detection. In the case of the double thresholding approach, noisy pixels are identified within a relatively narrow range and thus may reduce the probability of false detection.

In relation to the ECG signal, we have proposed an Adaptive Dual Threshold Filter (ADTF) [15-17]. The purpose of this filter is to calculate three elements for each sliding window of the ECG signal, namely, the average of this window, the upper threshold and the lower threshold. The equation of the mean of a filtering window is as follow:

$$g = \frac{1}{m} \sum_{i=n}^{n+m} \psi(i) \quad (1)$$

g is the mean of the selected window, m is the size of the window, and $\psi(i)$ is the noisy ECG signal. Following is the upper threshold equation:

$$Ht = g + [(Mx - g) \times \beta] \quad (2)$$

Ht is the upper threshold of the ADTF window, Mx is the maxima of the selected window, and β is the thresholding coefficient of the ADTF where:

$$0 < \beta < 1 \quad (3)$$

The lower threshold equation is as follows:

$$Lt = g - [(g - Mi) \times \beta] \quad (4)$$

Lt is the lower threshold of the ADTF window, Mi is the minima of the selected window.

The β coefficient used to adapt the thresholding process for filtering the ECG signal. As presented in [15-16], the smaller values of the β coefficient are necessary for the high concentration of noise. In the case of the lower concentration of noise, a greater tolerance is required, that is to say that higher values of the β coefficient are recommended. The ADTF algorithm for a given window of size $[i; i+m]$ is the following where φ is the corrected ECG signal:

$$\text{if } \psi(i + m/2) > Ht \Rightarrow \varphi(i + m/2) = Ht \quad (5)$$

$$\text{if } \psi(i + m/2) < Lt \Rightarrow \varphi(i + m/2) = Lt \quad (6)$$

$$\text{if } Lt < \psi(i + m/2) < Ht \Rightarrow \varphi(i + m/2) = \psi(i + m/2) \quad (7)$$

Fig. 1 shows a presentation of the evaluation of β coefficient based on a variety of levels of White Gaussian Noise (WGN) added to a real ECG signal of the MIT-BIH database [23-24], where the equation of the MSE parameter (mean square error) is as follows:

$$MSE = \frac{1}{m} \sum_{i=1}^n [\phi(i) - \varphi(i)]^2 \quad (8)$$

$\phi(i)$ is the original ECG signal. Fig. 2 presents the

impact of the window size of the ADTF algorithm on the ECG signal denoising process.

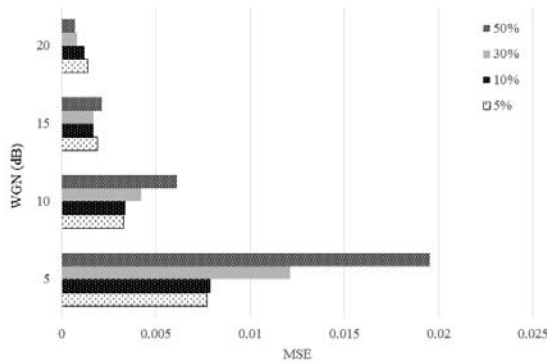


Figure 1: Evaluation of the β coefficient (%)

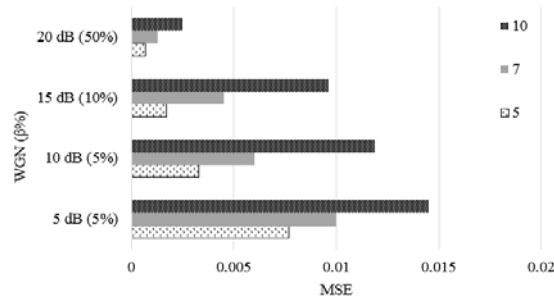


Figure 2: Evaluation of the window size of the ADTF algorithm

Fig. 3 shows results of the improvement of the signal-to-noise ratio (SNRimp) between the original signal, the noisy signal and the corrected signal, where:

$$SNR_{imp} = 10 \times \log_{10} \frac{\sum_{i=1}^n [\phi(i) - \psi(i)]^2}{\sum_{i=1}^n [\phi(i) - \varphi(i)]^2} \quad (9)$$

Several signals from the MIT-BIH database are proposed in this study. The SNRimp parameter varies between 7.8 for 5 dB of WGN for the different analyzed signals and 2.59 for 20 dB of WGN.

Fig. 4 presents a comparison diagram of the average SNRimp parameter of different signals of the MIT-BIH database between the proposed technique and those of the EEMD-FR [25] and the EEMD-GA [26]. As shown in this figure, the ADTF offers competitive results to the recently published EMD-GA [26] technique. Concerning the EEMD-FR [25] technique, the ADTF offers much better results for all the noise levels presented in this study.

To evaluate the complexity, this work proposes a comparative study between the proposed technique, the classical EMD and the classical EEMD without integrating the part of the thresholding algorithms according to Y. Wang [27]. This means that the

compared algorithms [25-26] have more complexity related to thresholding algorithms proposed in [25-26].

The ADTF algorithm proposes a linear complexity $O(n)$ related only to the size (n) of the signal to be studied. The EMD and the EEMD propose a linear complexity $O(n)$ but linked to the different parameters, namely, the size of the signal or the envelopes (n), the number of the IMFs studied (N_m), the number of sifting processes (N_S) and the number of the noisy signals used in the EEMD process.

Table 1 presents a comparison of the complexity of the ADTF, the EMD and the EEMD algorithms. The complexities of the EMD and the EEMD are proposed by Y. Wang [27] as well as the computation time of each arithmetic operation or of the test.

For the various reasons related to the low complexity of the ADTF as well as the high performances of ADTF-based ECG signal filtering, we have proposed a real-time hardware architecture of the ADTF process for online ECG signal denoising.

In the case of ADTF algorithm, the size of the window used in this study is 5 samples. As presented in Table 1, the ADTF algorithm proposes a low complexity for even a single level of the IMF for either the EMD or the EEMD. This is well represented in the diagram of Fig. 5 with a very small evolution of the complexity of the ADTF for larger data by comparing it with the EMD or the EEMD. For processing time, we considered a calculation time of an operation of 10 μ s equivalent to data processing frequency of 1 MHz.

3. VHDL IMPLEMENTATION OF THE ADTF

The VHSIC Hardware Description Language (VHDL) is a hardware description language designed to represent the behavior and the architecture of a digital electronic system. An architecture described in VHDL can be verified by simulation before the detailed design is completed. In addition, the design tools allow switching from a functional VHDL description to a logic gate schema to be implemented in digital circuits, ASIC or FPGA circuits. The purpose of a hardware description

language such as the VHDL is to facilitate the development of a digital circuit by providing an efficient method of describing the operation and the architecture of the desired circuit [28].

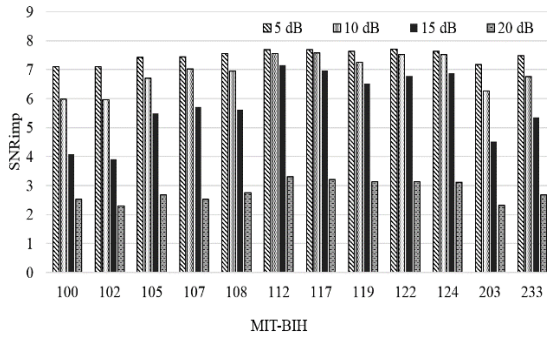


Figure 3: Evaluation of the SNRimp parameter of the ECG signal denoising based on the ADTF algorithm

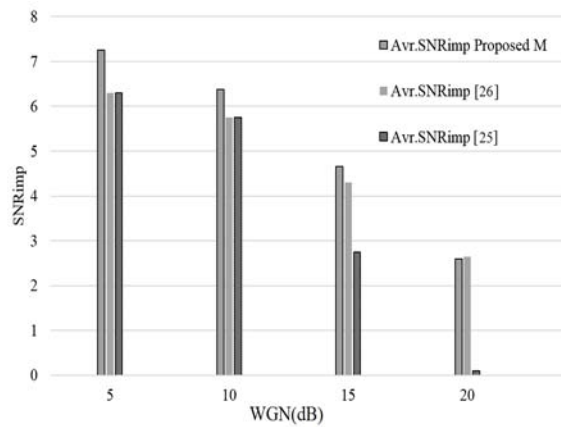


Figure 4: Comparative diagram of SNRimp evaluation for ECG signal denoising based on ADTF, EEMD-FR and EEMD-GA

Table 1: Complexity comparison of ADTF, EMD and EEMD algorithms

Algorithms	T
ADTF	$40 \times n$
EMD	$NS \times (41 \times Nm \times n)$
EEMD	$NE \times NS \times (41 \times Nm \times n)$

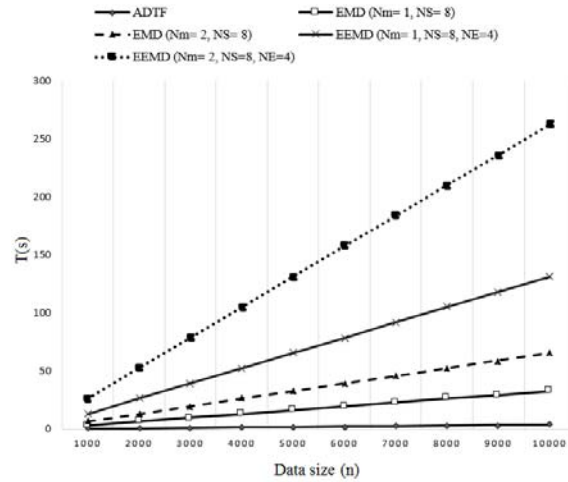


Figure 5: Comparative diagram of the time complexity depending on the data size (n)

This research work proposes an architecture of the ADTF based on three modules. The first concerns cardiac data loading by providing a real-time process without occupying a memory space. The second module makes it possible to calculate the elements necessary for ADTF processing. The third module deals with the calculation of the threshold levels as well as the application of the cardiac data tests and the assignment of the output data.

3.1 Real-time data loading module (RTDL)

The aim of the RTDL module is to read the incoming data through the 11-bit Input-signal port and prepare them for the following modules. This module is based on a shift register with a processing frequency identical to that of sampling the input ECG signal. In this case, we have used the signals from the MIT-BIH database of 360 Hz [29].

The processing window of the ADTF in this study is 5 samples, so the size of the shift register is 5 elements. This approach allows on-line processing of cardiac data without occupying a memory space for storing data before and after processing. Each element of the module is linked to an output of the same data size.

Fig. 6 shows an RTL scheme of the RTDL module. In the digital circuit design, the Register Transfer Level design (RTL) is an abstraction that models a digital circuit in terms of data-flow between the hardware registers and the logical

operations on signals analyzed.

3.2 Calculation of the ADTF features (CFM)

CFM module allows preparing the data necessary for processing, namely the average of the window of the ADTF, the maximum and the minimum of this window. The analyzed data comes from the RTDL module output. The processing frequency of this module is greater than that of the RTDL module. This ensures real-time analysis of the ECG signal. This implementation proposes a frequency of 3.6 KHz which is 10 times the frequency of the RTDL module.

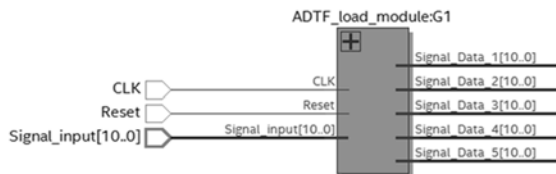


Figure 6: RTL scheme of the RTDL module

The calculation of the average is based on 4 sum operations plus one division. The output data size of this operation is encoded in 30 bits, 15 bits for the operation of the sum and 30 bits after the division. After this operation, the size of the output of the average encoded in 30 bits is minimized to 16 bits, 11 bits for the integer part and 5 bits for the fixed point of this value. To calculate the maximum and the minimum, two test loops applied are applied over the input data. The output is encoded in 11 bits for both operations. Fig. 7 shows an RTL scheme of the CFM module.

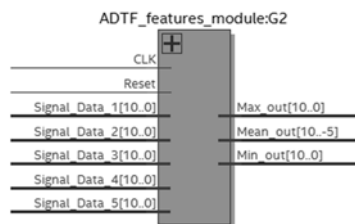


Figure 7: RTL scheme of the CFM module

3.3 Test and Assignment Module (TAM)

The aim of the TAM module is to calculate the threshold values for the two levels H_t and L_t . Data necessary for the calculation are obtained from the output of the CFM module, namely, the average of the window, the maximum and the minimum of this window. The calculation frequency of the TAM

module is identical to that of the MCP module. The TAM module process is as follows:

- Calculation of β coefficient: in this step, an 11 bits register is created to store the β coefficient. The high-order bit is reserved for the zero, which is the integer value of β where $\beta = 0.1$. Bits that follow are the binary values of the fixed point of this parameter.
- Calculation of H_t and L_t values: for this stage of processing, the calculation begins with a subtraction operation, then a multiplication of the output to the β coefficient and, in the end of this process, a subtraction or an addition to the mean of the ADTF window for the calculation of H_t and L_t respectively.
- Test and assignment: for the test phase, the comparison concerns the values of H_t and L_t with the value of the median sample of the ADTF window. Each of these tests focuses only on the integer values of H_t and L_t encoded in 11 bits. This is due to the size of the median sample of the ADTF window of 11 bits. The result of these tests is an assignment of a value to the output signal, whether those of H_t and L_t or the median sample.

The size of the output data is encoded in 16 bits, 11 bits for the integer part and 5 bits for the fixed point whether it is the value assigned to the output, namely H_t , L_t or the median sample of the ADTF window. For the first two values, the output is an adjustment of their values to 16 bits. In the case of the assignment of the median sample value of the ADTF window to the output, which is encoded in 11 bits, the 11 MSB (Most Significant Bits) of the output are identical to that of the median sample of the ADTF window plus 5 bits of zeros for the fixed-point part. Fig. 8 shows an RTL scheme of the TAM module.

Fig. 9 shows the RTL schema of the global ADTF architecture. These inputs are: the 11 bits input signal, the reset input, the two clocks Clk for reading the input data and $Clk-test$ for the CFM and TAM modules. The output of this architecture is the corrected signal of 16 bits (output signal). The global ADTF architecture design is based on a structural description.

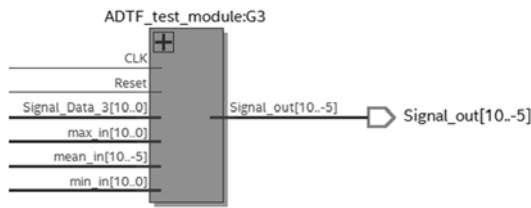


Figure 8: RTL scheme of the TAM module

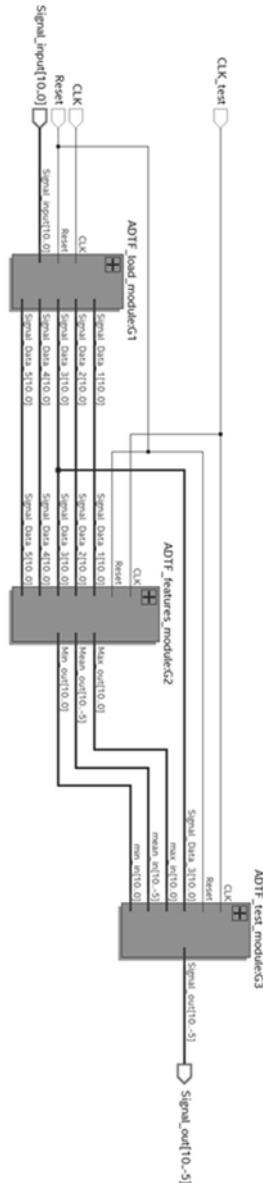


Figure 9: RTL scheme of the global ADTF architecture

The structural description of a complex circuit in VHDL allows separating a circuit into a set of blocks having well-identified functions. These functional

blocks can then be described in behavioural form, or into separated blocks. The structural description makes it possible to separate the different modules of the ADTF architecture and to make them operating in parallel. This allows reducing the processing time and offers a more efficient design where all blocks proceed in parallel.

4. RESULTS AND DISCUSSION

4.1 Functional simulation

In this task, the simulation of the proposed ADTF architecture is ensured by ModelSim software. ModelSim is an HDL simulation environment developed by Mentor Graphics for the simulation of hardware description languages such as VHDL, Verilog and SystemC [30]. ModelSim can be used independently, or in conjunction with Altera Quartus or Xilinx ISE. The simulation is performed using the graphical user interface (GUI) or automatically using scripts.

4.2 Qualitative results

In this section, this paper proposes a qualitative results study of the results of the proposed ADTF-based real-time ECG denoising using the MIT-BIH database. This study provides an evaluation of the performances of the ADTF architecture implemented in VHDL.

Fig. 10 shows an example of the real-time denoising of the signal No. 100 to 20 dB of the WGN under ModelSim. Fig. 22 illustrates the data-flow based on a clock of a real-time monitoring. As shown in this figure, the proposed ADTF architecture offers an efficient solution for the denoising of high-frequency noise in real-time.

Figs. 11 and 12 present a qualitative comparison between filtering results based on the Soft-ADTF (conventional programming) and the real-time filtering based on the proposed hardware ADTF architecture. The first figure presents a case of the addition of 20 dB of the WGN in the signal No. 100 of the MIT-BIH database. The second figure shows a case of the addition of 10 dB of the blue noise (colored noise) in the signal No. 203. The colored noise assigns to the power spectrum of a noise signal. Depending on whether it is pink, blue ... etc., the colored noise will have a different power spectrum. Depending on this power, the noise density varies at

different frequencies. This makes the different natures of colored noise closer to those actually found in nature and influencing physiological signals e.g. ECG signal [31].

between the results of the filtering of the Soft-ADTF and the Hardware-ADTF in real time. This reflects the high performance of the proposed VHDL architecture.

In Figs. 11 and 12, a high similarity is observed

4.3 Quantitative results

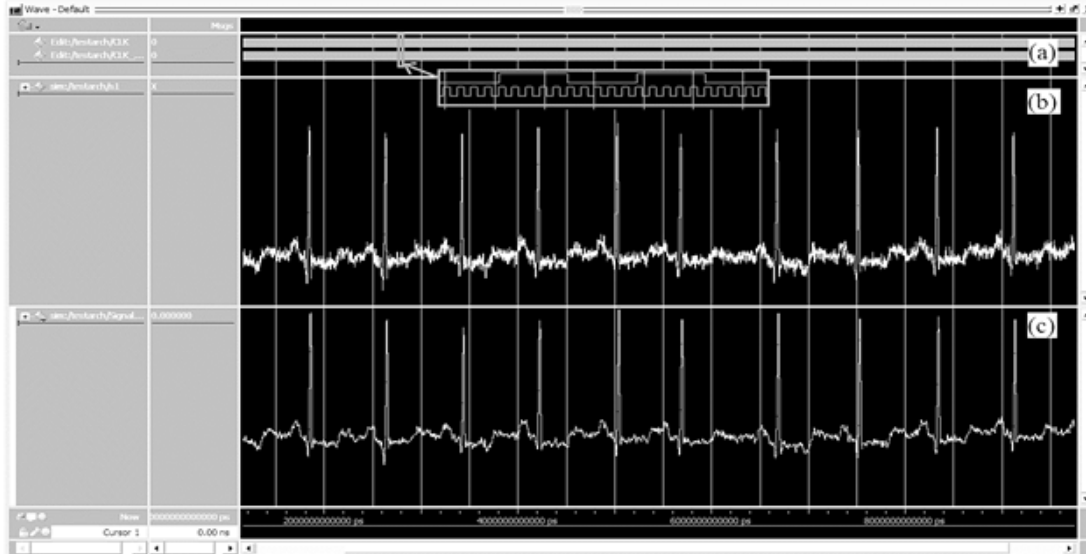


Figure 10: Real-time denoising: case of the MIT-BIH signal No. 100 with 20 dB of WGN. (a) CLK and CLK-test, (b) input signal, (c) output signal

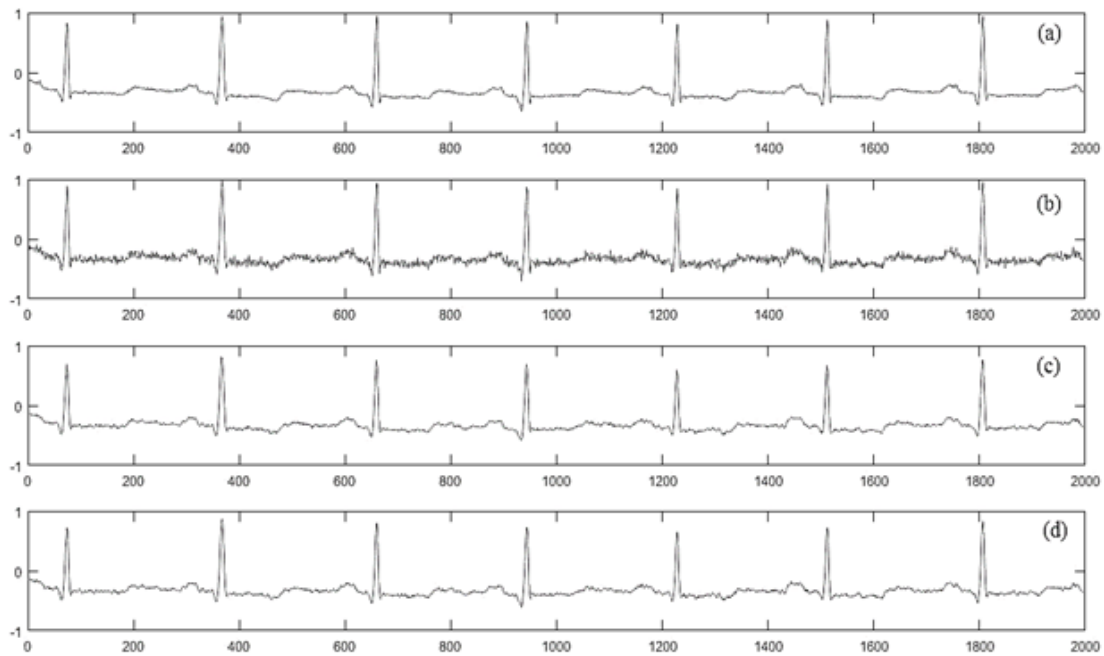


Figure 11: ECG signal denoising based on the ADTF: case of signal No. 100 with 20 dB of the WGN. (a) original signal, (b) noise-infected signal, (c) soft-ADTF corrected signal, (d) Hardware-ADTF corrected signal

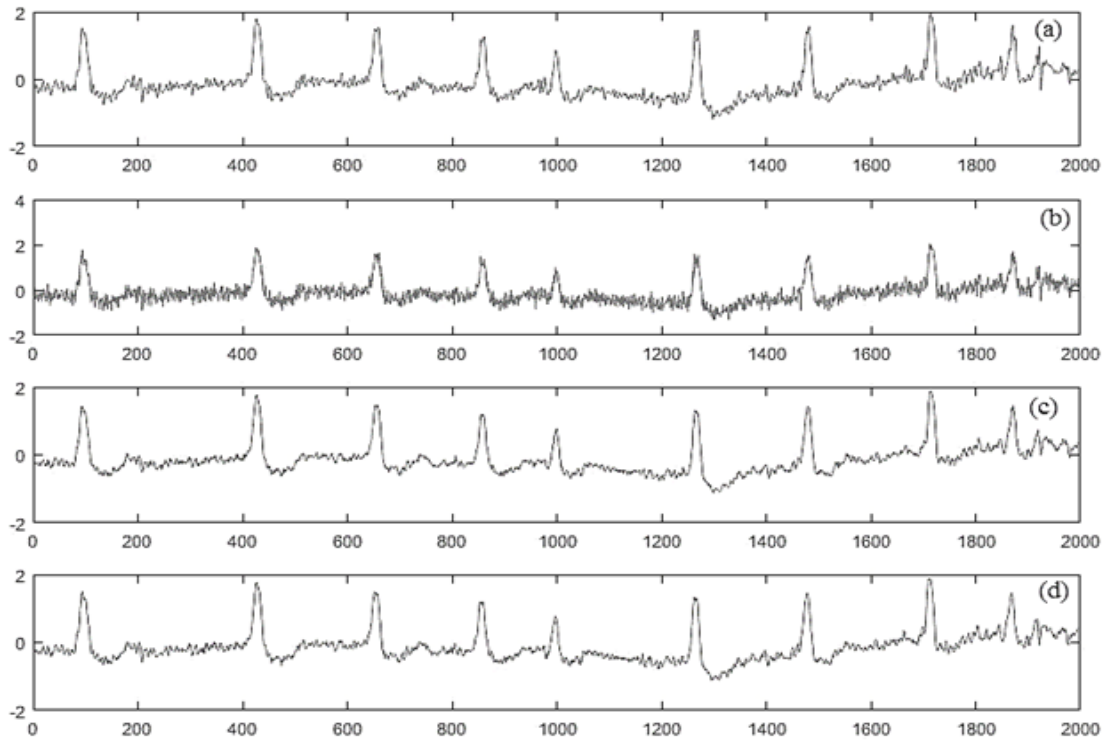


Figure 12: ECG signal denoising based on the ADTF: case of signal No. 100 with 20 dB of the WGN. (a) original signal, (b) noise-infected signal, (c) soft-ADTF corrected signal, (d) Hardware-ADTF corrected signal

Table 2 presents a results comparison of the SNR_{imp} parameter for a colored signal denoising in the case of the 203th MIT-BIH signal. The two noises proposed are the blue noise and the pink noise at 5 dB and 10 dB both. The blue noise is a colored noise with a spectral density proportional to its frequency. This means that the power and the energy of the noise signal increase as the frequency of the original signal increases. Unlike the blue noise, in the case of the pink noise, the power and the energy of the noise signal decrease as the frequency of the original signal increases. In Table 2, there is a little difference in terms of the SNR_{imp}-based statistical results between the Soft-ADTF and the Hardware-ADTF, in this case in favor of the hardware architecture. This supports the high performance of the proposed implementation.

Table 2: Comparison of the SNR_{imp}-based evaluation results of the colored noise denoising: case of the MIT-BIH signal No. 203

Methods	Blue (5 dB)	Blue (10 dB)	Pink (5 dB)	Pink (10 dB)
Soft - ADTF	9.37	1.43	6.91	1.18

Hardware - ADTF	9.54	1.39	7.98	1.22
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Fig. 13 shows a comparative diagram of the SNR_{imp}-based evolution of the ECG signal denoising based on the Soft-ADTF and the Hardware-ADTF. In this case, several signals were subject to this study for a WGN level of 5 dB. In this figure, there is a little difference between results of the Soft-ADTF and the Hardware-ADTF, in this case in favour of the Soft-ADTF.

In both cases of Table 2 and Fig. 13, this small difference in the statistical results does not reflect any improvement or changes in the overall concept of the ADTF process. This difference is related to the size of the data during the processing as well as the choice of the fixed point of 5 bits for the fractional part. The Soft-ADTF is built in a 64-bit machine with a floating-point processing. However, in the case of the Hardware-ADTF, this implementation proposes a fixed-point processing to reduce the complexity of the architecture as well as to further simplify the proposed architecture, which makes it implementable in different FPGA devices.

Table 3 shows a comparison of technical

resources used by different FPGA devices of INTEL-ALTERA for the implementation of the proposed ADTF architecture. This study concerns the total number of registers used, the percentage of logical elements used, the total number of pins used, the number of DSP blocks and the number of integrated elements for multiplication operations. As shown in this table, the proposed architecture occupies a moderate part for different FPGA devices.

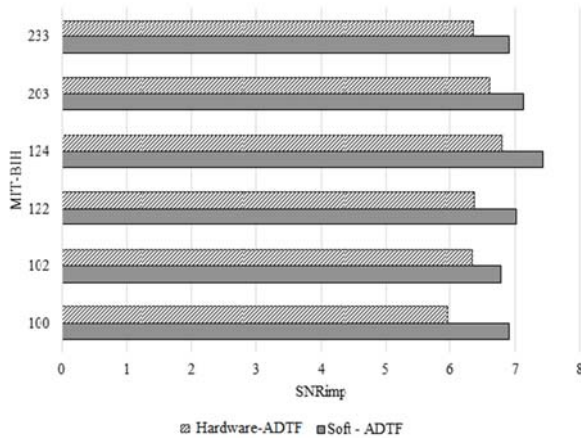


Figure 13: Comparative diagram of the SNRimp-based evolution of the ECG signal denoising based on the Soft-ADTF and the Hardware-ADTF.

Table 3: Comparison of technical resources used by different FPGA devices for the implementation of the proposed ADTF architecture

	Arria II GX	Cyclone IV E	Cyclone IV GX	Cyclone V	MAX 10
Total registers	245	244	245	251	244
Total logic elements	4%	1590 (25%)	1754 (17%)	662 (1%)	1579 (20%)
Total pins %	17%	33%	37%	11%	12%
Total block memory bits	0 %	0 %	0 %	0 %	0 %
DSP blocs	4 blocs (2 %)	-	-	2 blocs (1 %)	-
Embedded Multiplier 9-bit elements	-	4 (13%)	-	-	4 (8%)

The total number of logical elements used varies

between 1% only for the Cyclone V and 25% for the Cyclone IV E technology, knowing well that the two technologies, Cyclones IV and V, are classified as low-cost technologies according to their constructor INTEL-ALTERA. The total number of pins used is 30 pins. 11 pins for the cardiac data input, 2 pins for the two clocks used, 1 pin for the reset and 16 pins of the data output. The occupancy rate varies between 11% for the Cyclone V and 37% for the Cyclone IV GX. Concerning the memory blocks, the ADTF architecture does not propose a usage of these blocks.

The aim of the integrated multiplication elements is to optimize the multiplication operations in a given architecture. The DSP blocks include some calculation blocks with optimized units, including the integrated multiplication elements, for the arithmetic operations applied to signal processing. These blocks are available in a few technologies and they are not integrated in all the FPGA architectures of the INTEL-ALTERA.

The number of DSP blocks used is 4 blocks for the Arria II GX, which reflects 2% of the blocks proposed for this device and 2 blocks for the Cyclone V (1% only). The Arria II is a cost-optimized device offered by INTEL-ALTERA in the Arria family and it is the cheapest device in its family. Concerning FPGA architectures that doesn't contain the DSP blocks, the number of the integrated multiplication elements is 4 elements which reflect 13% of the occupation of these elements for the Cyclone IV E device and 8% for the MAX 10. The MAX 10 is a recent FPGA technology that has followed the production of the Cyclone family. Like its successor, the MAX 10 as the entire MAX family of INTEL-ALTERA, is a low-cost technology.

5. CONCLUSION

This paper proposes an implementation based on a hardware description of the adaptive dual threshold filter (ADTF) for the electrocardiogram signal denoising. This description is based on the VHDL language.

The paper begins with a description of the ADTF algorithm. Results of this algorithm show the high performances of the ADTF approach by comparing these results with related works recently published. This comparison makes it possible to judge and approve the choice of the proposed technique for the

hardware implementation task. Studying of the complexity of the ADTF technique allowed reducing its complexity, which makes it efficient for the implementation task.

The second part of this work described the different phases of the hardware description of the ADTF architecture. This description begins with the cardiac data loading in a real-time process, then the computation of the parameters of the ADTF and ends with the test and the assignment module. The qualitative and the quantitative results allows concluding the high performance of the proposed architecture by comparing these results to those of the soft-ADTF. A study of the implementation of the proposed architecture on different FPGA devices shows that this architecture occupies a modest space in these devices, which gives the possibility of adding other functional blocks to develop a real-time system of the cardiac data analysis based on FPGA devices.

CONFLICTS OF INTEREST

The authors declare that there is no conflict of interest.

FINANCIAL SUPPORT

We owe a debt of gratitude to the National Centre for Scientific and Technical Research of Morocco (CNRST) for their financial support and for their supervision (grant number: 18UIZ2015).

ACKNOWLEDGEMENTS

We gratefully acknowledge the valuable comments of the reviewers.

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