

# PROGRAMMABLE AMPLITUDE OF PORTABLE ELECTRICAL STIMULATOR FOR MULTI-CHANNEL FUNCTIONAL ELECTRICAL STIMULATOR (FES) SYSTEM

<sup>1</sup>RACHMAD SETIAWAN, <sup>2</sup>ACHMAD ARIFIN, <sup>3</sup>FAJAR BUDIMAN AND <sup>4</sup>ADI SOEPRIJANTO

<sup>1,3,4</sup>Department of Electrical Engineering, Institut Teknologi Sepuluh Nopember

<sup>2</sup>Department of Biomedical Engineering, Institut Teknologi Sepuluh Nopember  
SURABAYA, INDONESIA, 60111

E-mail: <sup>1</sup>rachmad@ee.its.ac.id, <sup>2</sup>arifin@bme.its.ac.id, <sup>3</sup>fajarbudiman@ee.its.ac.id, and <sup>4</sup>adisup@ee.its.ac.id

## ABSTRACT

Fundamental research about Functional Electrical Stimulation (FES) indicates that FES can be used to rehabilitate motoric system of patient experiencing damage at arrangement of central nerve resulted from cerebrospinal of cord injury (SCI) and also stroke. To generate impulse to human body organ activated by FES is difficult and very complex because of nonlinearity response from neuromuscular system, various response of musculoskeletal system such as having long time delay and fatigue phenomenon (muscle fatigue). Therefore, an open-looped control system is inappropriate to employ. Close-looped control is feasibly appropriate to overcome this constraint in FES appliance to yield accurate impulse generator. For the application of closed-loop control at clinical level, FES system must be designed using portable multi-channel device to pleasant the patient. In this research, the realized FES stimulator is designed by employing a highly linear boost converter circuit using fixed frequency and duty cycle ranging from 0% to 25%, because it yields relatively linear and higher output voltage swing than FES controlled by frequency.

**Keywords:** *Functional Electrical Stimulation, FES, closed-loop control, boost converter, duty cycle*

## 1. INTRODUCTION

Functional electrical stimulator (FES) has been widely used in rehabilitation of ability of motoric system of patient experiencing damage at arrangement of central nerve resulted from cerebrospinal of cord injury (SCI) and also stroke [1][2]. Researches about FES at clinical level include covers rehabilitation of kinetic performance on upper side of man kinetic organs (upper limb) and also under (lower limb) in everyday life, like grasping [3][4], standing up and walking / running (gait) [4][5]. In Indonesia, many paralysis patients experience losing of performance to run resulted by trouble in motoric nervous system as result of cerebrospinal of cord injury or damage at brain (brain damage). Therefore, FES is very potentially important to be developed as one of rehabilitation methods in motoric system [6]-[11]. The application of FES for rehabilitation of running performance at clinical level in general applies system is triggered manually by applying an open-looped control. This system is commonly used regarding to its simple and easy to develop.

Basically, an open-looped FES does not exploit muscle model to predict cupola from electrical stimulation intensity. FES system with control open-loop can yield good impulse only in condition of the controlled musculoskeletal system is unchanged. Human body organs activated by FES require a reliable operation method so it can yield desired impulse responses. However, controlling human body organ activated by FES is difficult and very complex because of the nonlinearity responses from neuro-muscular system, various from response musculoskeletal system to electrical stimulation, long time delay, and fatigue phenomenon (muscle fatigue). Therefore, to overcome constraints in FES controller, an application of closed-loop control system to yield accurate impulse is required. Typical closed-loop FES system consists of a controller, a stimulator and a sensor system, like depicted at Figure 1.

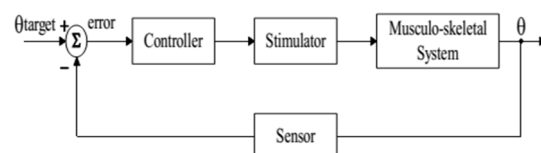


Figure 1: A closed-loop FES system diagram

In this research, a method to develop a portable multi-channel FES system to counterpart the problems in the lack of supporting facilities for rehabilitation motoric system at clinical level using closed-loop control is discussed. The linearity of the output voltage is concerned that can be further implemented in closed-loop control for FES that will comfort the patients.

## 2. LITERATURE REVIEW AND METHODS

As mentioned in introduction section, each motoric task has phases of standing up, standing, walking, and sitting down. This is usually controlled using crutch switches [3]. This FES systems is based on open-loop control that are addressed to problems related to lack of sensitivity to either external or internal disturbance or changes in the system parameters e.g. fatigue phenomena [12], muscle habituation, and muscle spasticity [13]. This non-linear response lead to developing FES systems based on closed-loop control [14] to produce real time measurement with sensors and obtain suitable modulated stimulation pattern. In this research, we focus on producing programmable linear electrical stimulator for multichannel FES.

Electrical stimulation frequency in FES that has a significant effect on the strength and smoothness of muscle contractions has also been conducted in many researches [15][16]. Frequency modulation is aimed to minimize fatigue while maximizing force [17] in which the effects is in fast attraction/twitch when the electrodes put on close to muscle nerve. Electrical stimulation frequency has different effects on the quality of sensation [18]. However, this frequency modulation approach has lack of linearity. Popovic et. All in [11] had put in the context of the current clinical application of the BION technology, in which patients are stimulated with a fixed frequency while the pulse duration or pulse amplitude are modulated in order to achieve the desired level of muscle activation. In this research, we proposed the stimulator using fixed-frequency that is suitably tuned with variable duty cycle to generate linear amplitude output stimulator to pleasant the patient.

Some methods to change DC voltage level to become DC voltage in which its amplitude differs among others are buck converter, boost/burst converter, buck-boost converter, and cuk converter [19][20]. Many former papers have discussed different methods of dc-to-dc conversion. From the earlier paper in [9], dc-to-dc conversion method in accordance with the desired design is a boost conversion method. In this research, we have

designed a boost converter circuit. The boost converter or step-up converter is a dc-to-dc converter functioned to boost-up a dc voltage level to higher level. Ideal boost converter circuit consists of principal components that is intrinsic semiconductor switches, diode, inductor and capacitor.

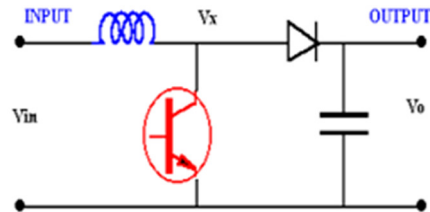


Figure 2: Basic Scheme of Boost Converter

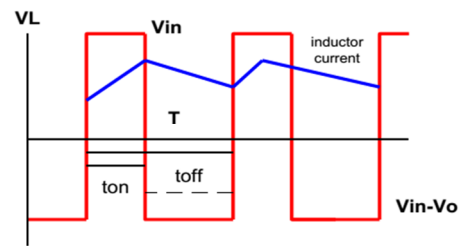


Figure 3: Voltage and current waveform

Figure 2 shows a boost fundamental converter circuit using a transistor as a switch. This circuit is applied when a higher level output voltage than input is required. Analytically, when transistor is in ON state, the voltage in node Vx is equal to Vin and the system state is in OFF condition, the inductor current flows towards to diode and gives Vx = Vo. The waveforms of the voltage and current are shown in Figure 3. To analyze this scheme, the inductor current is assumed to be flowing. Thus, the voltage passing through the inductor as shown in Figure 2 and its average current must be zero, so that it will be remaining at condition of steady state. It can be formulated as in equation (1).

$$V_{in}t_{on} + (V_{in} - V_o)t_{off} = 0 \quad (1)$$

Equation (1) can be rearranged become,

$$\frac{V_o}{V_{in}} = \frac{T}{t_{off}} = \frac{1}{(1-D)} \quad (2)$$

And for lossless circuit regarding to conservation of energy, Equation (2) can be expressed as

$$\frac{I_o}{I_{in}} = (1 - D) \quad (3)$$

Since the value of duty ratio "D" is between 0 and 1, the output voltage magnitudes must be always higher than its input voltage. The negative sign shows the inversed output voltage.

The FES which will be proposed uses a method of boost/burst converter in which:

- The desired output voltage is a dc voltage of 50 volts up to 120 volts, so this is a step-up converter.
- The desired design can be as small as possible regarding its wearability and portability.
- The capacitor value for the boost/burst converter circuit must be as small as possible to have a small size of capacitor.
- The inductor value must be small to have a small size.

In the scheme of boost converter circuit with above constraints of input voltage, output voltage and load current, the value of L is the first parameter to find which can be calculated using formula as in equation (4).

$$L = \frac{(V_{out} - V_{in} + V_D)(1-D)}{i_{load} \cdot f} \quad (4)$$

$$L = \frac{(100 - 5 + 0.7)(1 - 0.5)}{5 \cdot 10^{-3} \cdot 500} \quad (5)$$

$$L = 19.14 \text{ mH} \cong 22 \text{ m} \quad (6)$$

where  $V_D$  is diode voltage, D is duty cycle and f is frequency. In this paper, the boost converter designed is equipped with desired parameters as following:

- 1) Input voltage of 5 V
- 2) Output voltage of 100 V
- 3) Frequency between 0 - 500 Hertz
- 4) Duty cycle = 50 %
- 5) Load current 5 mA (Maximum current 60 mA)

From above parameters, the inductor value can be calculated by using the formula in equation (4) as shown in (5). As a result, the inductor value is

19.14 mH. Inductor of 22 mH is chosen which is easily found the availability in the market.

Furthermore, to find the capacitor value that is used for speeding up the circuit response, equation (7) is used. The calculation of the capacitor  $C_s$  is done in (8). To fulfill the required parameter, the value of  $C_s$  must be less than 2  $\mu\text{F}$  as shown in (9). Here, 100 nF capacitor is chosen to be applied regarding to its small size.

$$C_s < \frac{1}{20 \cdot R_B \cdot f_{max}} \quad (7)$$

$$C_s < \frac{1}{20 \cdot 50 \cdot 500} \quad (8)$$

$$C_s < 2 \mu\text{F} \quad (9)$$

Next step is to determine transistor type which will be applied to the circuit, a calculation using equation (10) is used.

$$f_{max} = \frac{0.35}{100 \cdot t_r} \quad (10)$$

where  $t_r$  (recovery time) is the time required by transistor for its transition condition from cut off becomes saturation. If we set the  $f_{max}$  to be 500 Hz, we will obtain  $t_r = 7 \mu\text{s}$  from calculation by equation (10). From this calculation of  $t_r$ , a MMBTA42 transistor is chosen and applied to the circuit, since the rise time ( $t_r$ ) of MMBTA42 from the datasheet is 15 ns.

### 3. DESIGN IMPLEMENTATION

The FES system design can be categorized into two parts which are hardware and software designs. The hardware design covers the circuit implementation in which the electrical components have been calculated in the previous section. The software design covers the program embedded in microcontroller and serial data transmission between the FES system and computer/laptop.

#### 3.1 Hardware Design

For multi-channel FES, each channel consists of two main parts: an amplitude generator as depicted in Figure 4 and a pulse generator as depicted in Figure 5. The core circuit of the proposed FES is capable to yield output signal in the form of modulation. An ATTiny2313 microcontroller is

employed to the pulse generator and amplitude generator.

Figure 4 is a boost generator circuit, the main components are Resistor R<sub>9</sub>, Transistor Q<sub>4</sub>, Inductor L<sub>1</sub>, Diode D<sub>2</sub> and Capacitor C<sub>4</sub>. The inductor value of 22 mH is chosen that has been analyzed and calculated in section 2. Capacitor C<sub>2</sub> is used as a speed up capacitor for fast time response. Diode D<sub>5</sub> is used to protect transistor Q<sub>4</sub> to avoid a damaged caused by failure of the system. Pin #14 (PB2) of microcontroller connected to the circuit is served as a signal generator PWM in which the duty cycle can be adjusted from 0% to 100%. Figure 5 illustrate that the output of pin #16 (PB4) is directly disjointed to become 2 lines. One line is channeled through a transistor MMBTA42 (Q1), while the other in advance is channeled to a transistor MMBTA42 (Q2) as an inverter before it is finally connected to MMBTA42 (Q3). In the second part (the lower part of the circuit), collector output of Q3 is connected to the base of MMBTA92 (P1). As a result, this combination with Q1 and P1 yields larger modulation of voltage output.

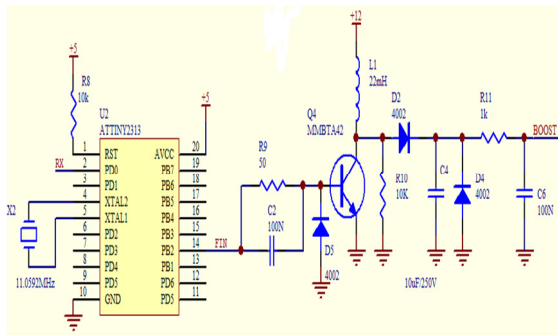


Figure 4: Amplitude generator circuit of FES

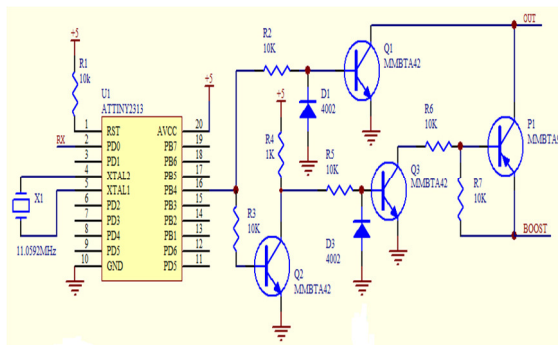


Figure 5: Pulse generator circuit of FES

The modulation duration can be easily controlled and adjusted through programming the software embedded in microcontroller. Meaning, the on time t<sub>ON</sub> of modulation is in rising edge and the off time t<sub>OFF</sub> of modulation is in falling edge, it is fully done by microcontroller commanded by user through a

personal computer/laptop. A Bluetooth tool is used to transmit and receive data to and from the FES module with baud rate setting of 115200 bps. Since the Bluetooth has a data input type of TTL level, it is required a USB to TTL converter for interfacing.

### 3.2 Software Design

The duty cycle data transmitted from computer must be converted into a string of data for following serial communication data format, while the duty cycle data of the microcontroller must be in form of hexadecimal data high and hexadecimal data low. To convert the data into a hexadecimal, it can be obtained by receiving a string of data first, and then converter into a decimal, afterward it is converted into hexadecimal data high and hexadecimal data low. Figure 6 shows the sequence of data conversion in string format to be hexadecimal.

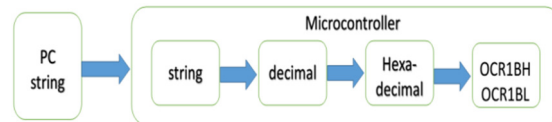


Figure 6: Data conversion flow of software design

To generate fixed frequency output, a crystal oscillator is used to generate oscillator clock frequency. The frequency output can be calculated by using factor scale and the maximum counter provided by the compiler of microcontroller as shown in equation (12) and equation (13). The result of frequency is saved in register OC1 divided into OC1A and OC1B.

$$f_{oc1a} = \frac{f_{osc}}{N \cdot (1 + TOP)} \quad (12)$$

$$f_{oc1b} = \frac{f_{osc}}{N \cdot (1 + TOP)} \quad (13)$$

$$D = \frac{OCR1X}{TOP} \times 100\% \quad (14)$$

where:

- f<sub>oc1a</sub> = Frequency output OC1A
- f<sub>oc1b</sub> = Frequency output OC1B
- N = Clock Scale (1, 8, 64, 256 and 1024)
- D = Duty cycle
- f<sub>osc</sub> = Crystal Frequency
- TOP = maximum counter (TCNT1),

TOP provided by the microcontroller compiler has 3 values that is 8 bits (0FF), 9 bits (1FF) and 10 bits (3FF).

To set and tune the duty cycle after we set the desired constant frequency, equation (14) is used. The goal is to find the register value of ORR1X in

hexadecimal which has maximum 16 bits. For example, to tune the duty cycle becomes 75%, we use equation (14) in which the calculation is shown as follows,

$$\begin{aligned} D &= (\text{OCR1X}/\text{TOP}) * 100\% \\ 75\% &= (\text{OCR1X}/1023) * 100\% \\ \text{OCR1X} &= 767 = 2\text{FF (in hexadecimal)} \end{aligned}$$

There is a flow of procedures coded in the software design embedded in the ATtiny 2313 microcontroller. First procedure, the microcontroller has to be initialized to activate its serial data communication with 115200 bps, with parameter of 8 data, 2 stops and no parity. The initialization code is expressed as following,

```
UCSRA=0x00;
UCSRB=0x98;
UCSRC=0x0E;
UBRRH=0x00;
UBRRL=0x05;
```

*UCSRA=0x00*, meaning that all USART registers are set in receive and transmit complete modes. Data Register is set empty with Frame Error, Data over run, and Parity Error. The USART Transmission Speed is doubled, while the MPCM (Multi-processor Communication Mode) is deactivated.

*UCSRB=0x98*, meaning that the RX Complete Interrupt Enable and TX Complete Interrupt Enable are activated. USART Data Register Empty Interrupt Enable is deactivated. Receiver Enable (RXEN) and Transmitter Enable (TXEN) are activated. Transmit Data Bit 8 (TXB8) is deactivated with character size of 8 bits.

*UCSRC=0x0E*, we select the URSEL (Register Mode Select) to choose UBRRH Register and UMSEL (USART Mode Select) to choose asynchronous mode, with the Parity Mode of even parity. USBS (Stop Bit Select) is 2 bit. UCSZ1 is the Character Size 8 bit. Finally, UCPOL (Clock Polarity) is set as rising edge for transmitting data and falling edge for receiving data. *UBRRH=0x00* and *UBRRL=0x05*, are for setting the URSEL (Register Select) to set the USART Baud Rate of 115200.

In the process of transmitting duty cycle data, the data has to be converted into string format which only can be sent one by one. Since the information of duty cycle from 0% to 100% has 3 digits, we divide the data into three parts, which are hundreds, tens and ones. Each digit is added by 30H. Furthermore, any data must be sent in the form of characters of different protocols, since we have 2

duty cycle data, we use two protocols which are 'a' and 'c'. The code programs to transmit the duty data with protocol can be seen in the following,

- Send data of first duty cycle in percent with protocol 'a'

```
sat := dutycycle1 mod 10;
pul := (dutycycle1 div 10) mod 10;
rat := dutycycle1 div 100;
rat := rat + $30;
pul := pul + $30;
sat := sat + $30;
Comport1.WriteStr('a');delay(1);
Comport1.Write(rat,1);delay(1);
Comport1.Write(pul,1);delay(1);
Comport1.Write(sat,1);delay(1);
```

- Send data of second duty cycle in percent with protocol 'c'

```
sat := dutycycle2 mod 10;
pul := (dutycycle2 div 10) mod 10;
rat := dutycycle2 div 100;
rat := rat + $30;
pul := pul + $30;
sat := sat + $30;
Comport1.WriteStr('c');delay(1);
Comport1.Write(rat,1);delay(1);
Comport1.Write(pul,1);delay(1);
Comport1.Write(sat,1);delay(1);
```

Where *sat* is variable for “ones”, *pul* represents the variable for “tens”, and *rat* represents variable for “hundreds”. The microcontroller receives the duty cycle data and omits the protocols. The data are received on by one in string format as follows,

```
rb = getchar();
p = getchar();
s = getchar();
```

The string format of duty cycle data are then converted into decimal format using codes as follows,

$$\begin{aligned} dt &= ((rb-0x30)*100)+((p-0x30)*10)+(s-0x30); \\ dt &= dt * 5.11; \end{aligned}$$

where *dt* represent the duty cycle in decimal format, *rb* is hundreds, *p* is tens, and *s* is ones. To get the original data, each digit is subtracted by 0x30 (30H) as we add 30H before the data are transmitted.

Second procedure, the microcontroller of ATtiny2313 has to be initialized to yield frequency output and duty cycle = 0%. For ATtiny 2313, timer 1 is used with fast Pulse Width Modulation



(PWM) mode. The initialization of timer 1 as Fast PWM Mode coded as follows,

```
TCCRI A=0x22;
TCCRI B=0x0B;
OCR1BH=0x00;
OCR1BL=0x00;
```

TCCRI A=0x22, it means that the Clock source is System Clock provided by internal microcontroller, with the value of 43.200 kHz. The fast PWM mode with TOP is equal to 01FFh. TCCRI B=0x0B is the timer set to have OC1A output is discontinue and OC1B output is Non-Inverted. Setting registers OCR1BH=0x00 and OCR1BL=0x00 are the first setting for duty cycle equal to 0%.

Third procedure, we create a software program to receive serial data in string and then convert the data string to decimal. In order to yield duty cycle, decimal data converted into hexadecimal with procedure coded as following,

```
void dectohex(unsigned int dat)
{
    hex_sat = dat % 16;
    hexs = hex_sat;
    if (hex_sat < 10)
        hex_sat = hex_sat + 48;
    else
        hex_sat = hex_sat + 55;
    hex_pul = (dat/16) % 16;
    hexp = hex_pul;
    if (hex_pul < 10)
        hex_pul = hex_pul + 48;
    else
        hex_pul = hex_pul + 55;
    hex_rat = ((dat/16)/16) % 16;
    hexr = hex_rat;
    if (hex_rat < 10)
        hex_rat = hex_rat + 48;
    else
        hex_rat = hex_rat + 55;

    hex_rib = ((dat/16)/16)/16;
    hexb = hex_rib;
    if (hex_rib < 10)
        hex_rib = hex_rib + 48;
    else
        hex_rib = hex_rib + 55;
}
}
```

Finally, the hexadecimal data is divided into 2 groups, high hexadecimal and low hexadecimal. The two data are send and saved to two registers of OCR1BH and OCR1BL as provided by microcontroller, as coded as following,

```
OCR1BH=(hexb*16)+hexr;
OCR1BL=(hexp*16) + hexs;
```

### 3. RESULTS

Figure 7 shows the photograph of the proposed multichannel FES stimulator. The size of the system circuit board is as big as a name card that makes handy for wearable FES. This size can be reduced and smaller as the microcontroller and some electrical components are replaced with surface-mount Device (SMD) type.

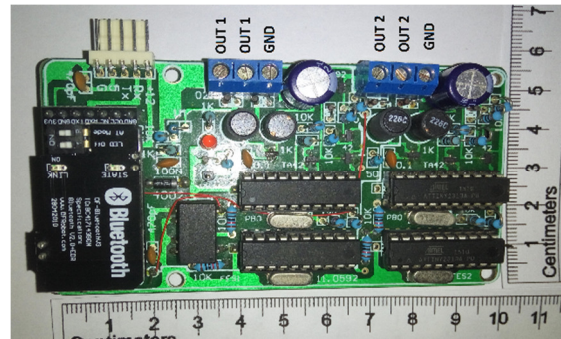


Figure 7: The proposed pulse generator circuit of FES

The beginning set up is to generate a constant frequency. As mentioned in section 2, we design the system to have a frequency input of 500 Hz. We use ATTiny2313 microcontroller with oscillator crystal of 11.0592. Refer to equation (11) and (12), we can find the Pulse Width Modulation (PWM) output frequency. Table 1 summarizes the output frequency and voltage for different clock scale (N) with maximum counter (TOP) of 0FF for 8 bits. Table 2 and Table 3 also summarize summarizes the output frequency and voltage for different clock scale (N) with maximum counter of 1FF for 9 bits and 3FF for 10 bits respectively.

Table 1 Mode of Fast PWM for maximum counter of 0FF for 8 bits

N (Clock Scale)	Output frequency (Hz)	Output Voltage (volt)
1	43.200	80.5
8	5.400	92.6
64	675	141.8
256	168,75	140
1024	42,1875	89.8

Table 2 Mode of Fast PWM maximum counter of 1FF for 9 bits

N (Clock Scale)	Output frequency (Hz)	Output Voltage (volt)
1	21.600	43.66
8	2.700	118
64	337,5	144
256	84,375	118
1024	21,094	64

20	100.70	20	132.60	20	140.1
21	100.70	21	132.60	21	140.6
22	100.70	22	132.60	22	140.9
23	100.70	23	132.60	23	141.2
24	100.70	24	132.60	24	141.5
25	100.70	25	132.60	25	141.7

Table 3 Mode of Fast PWM maximum counter of 3FF for 10 bits

N (Clock Scale)	Output frequency (Hz)	Output Voltage (volt)
1	10.800	46
8	1.350	144
64	168,75	140
256	42,1875	88
1024	10,54	47

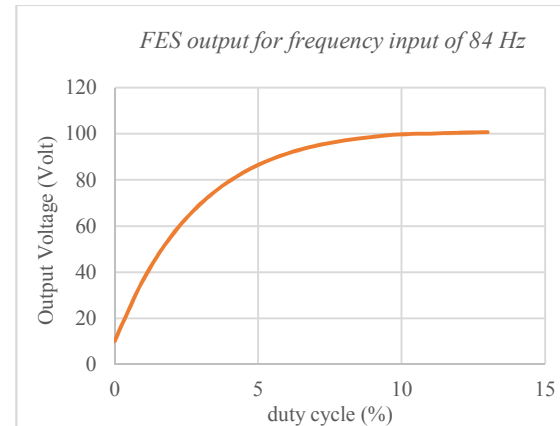


Figure 8: FES output for frequency input of 84 Hz with duty cycle 0% to 13%

To show the good performance of the proposed FES, experimental tests by giving frequency inputs of 84 Hz, 168 Hz, and 337 Hz with duty cycle 0% to 25%. Table 4 summarizes the measurement results. For input frequency of 84 Hz, the output voltage changes transiently from 0% until 12% duty cycle, while in duty cycle of 13% and above, the output voltage become constant as depicted in Figure 8. Linear output voltage is generated if the duty cycle input of 1% to 4%.

Table 4 Measurements of FES for three frequency inputs

Frequency = 84 Hz		Frequency = 168 Hz		Frequency = 337 Hz	
Duty Cycle (%)	Output Voltage (volt)	Duty Cycle (%)	Output Voltage (volt)	Duty Cycle (%)	Output Voltage (volt)
0	10.15	0	13.01	0	7.87
1	36.81	1	29.23	1	22.66
2	56.02	2	49.75	2	36.39
3	69.70	3	61.31	3	48.95
4	79.50	4	76.00	4	60.46
5	86.50	5	84.30	5	71.00
6	91.40	6	94.80	6	80.70
7	94.80	7	100.70	7	89.70
8	97.10	8	108.10	8	97.90
9	98.70	9	112.30	9	105.40
10	99.80	10	117.40	10	113.60
11	100.10	11	121.60	11	119.80
12	100.50	12	123.90	12	125.40
13	100.70	13	126.60	13	130.00
14	100.70	14	128.00	14	133.40
15	100.70	15	129.60	15	135.80
16	100.70	16	130.40	16	137.20
17	100.70	17	131.30	17	138.10
18	100.70	18	131.70	18	138.90
19	100.70	19	132.20	19	139.70

For input frequency of 168 Hz, the output voltage changes transiently from 0% until 19%, while in duty cycle of 20% and above, the FES generates constant output voltages as depicted in Figure 9. Linear output voltage is generated if the duty cycle input of 1% to 10%. For input frequency of 337 Hz, the output voltage changes transiently from 0% until 24%, while in duty cycle of 25% and above, the FES generates constant output voltages as depicted in Figure 10. Linear output voltage is generated if the input duty cycle of 1% to 15%. From this experiments, it shows that the higher the input of fixed frequency will produce the higher output voltage with the same input of duty cycle. This system has the highest frequency input of 337 Hz since the microcontroller counter is only 8 bit. However, the proposed stimulator is reliable for multichannel FES with fixed frequency and duty cycle tuning in which the common output voltage that is required for FES in rehabilitation is 70 volts to around 100 volts.

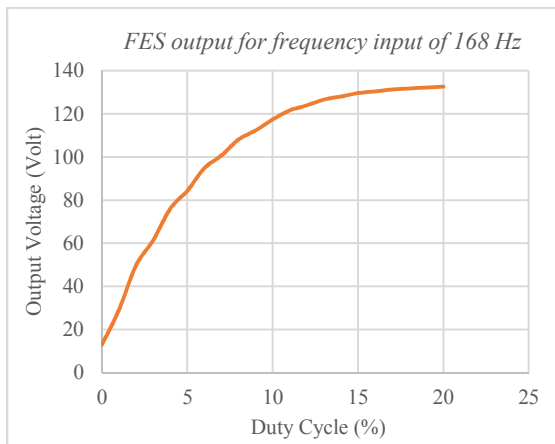


Figure 9: FES output for frequency input of 168 Hz with duty cycle 0% to 20%

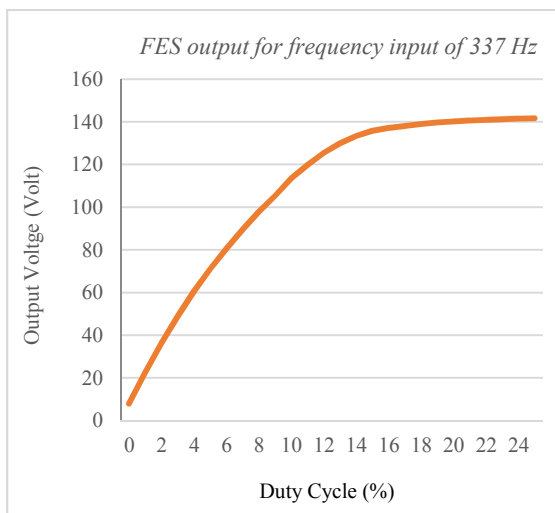


Figure 10: FES output for frequency input of 337 Hz with duty cycle 0% to 25%

#### 4. CONCLUSIONS

The proposed multichannel FES stimulator has a boost converter as a primary circuit. The output voltage can be adjusted with the boost converter input frequency and duty cycle. If the input frequency is used, the output voltage generated is not linear, whereas if the input is used duty cycle with a frequency fixed, the output voltage produced linear scale from 0% to a certain scale depending on frequency used. The linearity of the output voltage of the FES will be even wider, if the input frequency used is increasingly higher. However, a constraint encountered when raising the input frequency, the inductor will become hot that lead to inefficient loss in power dissipation. Besides this frequency generator is generated by the microcontroller which is limited by a timer

function. So, the realized FES stimulator was a boost converter with fixed frequency and duty cycle from 0 % to 25%, because it yielded relatively linear and higher output voltage than FES controlled by frequency. Therefore, FES will be used for the provision of the stimulus waveform using FES with input duty cycle. For the future work, this FES can be used portably and incorporated with wearable sensor for lower limb joint angle measurements using inertia MEMS sensors. The system will be developed for monitoring and rehabilitation using wireless connection for patient comfortability.

#### REFERENCES:

- [1] K. Subramanya, A. J. P. Pinto, M. K. A. Kumar, B. K. Arya, and M. Mahadevappa, "Surface Electrical Stimulation Technology for Stroke Rehabilitation: A Review of 50 Years of Research," *Journal of Medical Imaging and Health Informatics*, vol. 2, pp. 1-14, 2012.
- [2] B. K. Arya, K. Subramanya, M. Mahadevappa and R. Kumar, "Electrical stimulation devices for cerebral palsy: design considerations, therapeutic effects and future directions," in W. Yue, S. Chattopadhyay, T. C. Lim, and U. R. Acharya, Eds., *Advances in Therapeutic Engineering*. Boca Raton, FL: CRC Press, 2012.
- [3] A Kralj and T Bajd, "Functional Electrical Stimulation: Standing and Walking after Spinal Cord Injury," CRC Press, Boca Raton, 1989.
- [4] L. Vodovnik, T. Bajd, A. Kralj, F. Gracanin, P. Strojnik, "Functional Electrical Stimulation for Control of Locomotor System," *CRC Critical Review in Biengineering*, pp. 63-131, 1981.
- [5] N. Hoshimiya, A. Naito, M. Yajima, and Y. Handa, "A Multichannel FES System for the Restoration of Motor Function in High Spinal Cord Injury Patients," *IEEE Trans. Biomed. Eng.*, vol. 36, pp. 754-760, 1989.
- [6] T. Masuko, T. Watanabe, A. Arifin, M. Yoshizawa, "An Experimental Test of Knee Joint Control by Fuzzy FES Controller Based on Cycle-to-Cycle Control," *Trans. of the Japanese Society for Medical and Biological Engineering*, Vol.45, No.4, 313-318, Apr. 2007.



- [7] A. Arifin, T. Watanabe, T. Masuko, "Application of Knowledge Engineering and Fuzzy System in Realizing Cycle-to-Cycle Control Method for Swing Phase of FES-induced Gait," Invited Lecture on Neural Engineering Session, Proc. 3<sup>rd</sup> Intl. Symp. Medical, Bio-Nano Electronics, pp. 43-51, Sendai, Japan, 2008.
- [8] T. Watanabe, T. Masuko, A. Arifin, Preliminary Tests of a Practical FES Controller Based on Cycle-to-Cycle Control in the Knee Flexion and Extension Control, IEICE Trans. Information and Systems, Vol.E92-D, No.7. pp.1507-1510, Jul. 2009.
- [9] A. Arifin, T. Watanabe, and N. Hoshimiya, "Design of Fuzzy Controller of the Cycle-to-Cycle Control for Multi-Joint Movements of Swing Phase of Hemiplegic Gait Induced by FES," IEICE Trans. Information and Systems, Vol. E89-D, No. 4, pp.1525-1533.
- [10] P. H. Peckham and J. S. Knutson, "Functional electrical stimulation for neuromuscular applications," Annu Rev Biomed Eng, vol. 7, pp. 327-60, 2005.
- [11] D. Popovic, et al., "Recruitment and comfort of BION implanted electrical stimulation: implications for FES applications," IEEE Trans Neural Syst Rehabil Eng, vol. 15, pp. 577-86, Dec 2007.
- [12] H. B. K. Boom, A. J. Mulder, and P. H. Veltink, "Fatigue during functional neuromuscular stimulation," Progr. Brain Res., vol. 97, pp. 409-418, 1993.
- [13] A. Stefanovska, L. Vodovnik, N. Gros, S. Rebersek, and R. AcimovicJanezic, "FES and spasticity," IEEE Trans. Biomed. Eng., vol. 36, pp. 738-745, July 1989.
- [14] H. J. Chizeck, "Adaptive and nonlinear control methods for neural prosthesis," in Neural Prosthesis, Replacing Motor Function After Disease or Disability, R. B. Stein, P. H. Peckham, and D. P. Popovic, Eds. New York: Oxford University Press, 1992, pp. 298-328.
- [15] I. E. Brown, E. J. Cheng, and G. E. Loeb, "Measured and modeled properties of mammalian skeletal muscle II. the effects of stimulus frequency on force-length and force-velocity relationships," J. Muscle Res. Cell Motility, vol. 20, pp. 627-643, 1999.
- [16] I. E. Brown and G. E. Loeb, "Measured and modeled properties of mammalian skeletal muscle III. the effects of stimulus frequency on stretch-induced force enhancement and shortening-induced force depression," J. Muscle Res. Cell Motility, vol. 21, pp. 21-31, 2000.
- [17] S. A. Binder-Macleod, "Variable frequency stimulation patterns for the optimization of force during muscle fatigue. Muscle wisdom and the catch-like property," in Advances in Experimental Medicine and Biology. New York: Springer, 1995, vol. 384, ch. 16, pp. 227-240.
- [18] K. Koga, H. Furue, T. Toya, and N. Matsumoto et.al., "Selective activation of primary afferent fibers evaluated by sine-wave electrical stimulation," Molecular Pain, vol. 1, pp. 1-13, Mar. 2005.
- [19] Mohan, Ned; Undeland, Tore M., Robbins, William P. Power Electronics. Hoboken: John Wiley & Sons, Inc., ISBN 0-471-42908-2, 2003.
- [20] Basso, Christophe, Switch Mode Power Supplies: SPICE Simulations and Practical Designs. New-York: McGraw-Hill. ISBN 0-07-150858-9, 2008.
- [21] P.E. Cargo, P. H. Peckam, and G. B. Thrope, "Modulation of Muscle Force by Recruitment During Intramuscular Stimulation," IEEE Trans. Biomed. Eng., vol. BME-27, pp. 679-1980.
- [22] H. Saito, T. Watanabe, A. Arifin, "Ankle and Knee Joint Angle Measurements during Gait with Wearable Sensor System for Rehabilitation," Proc. World Congress on Medical Physics and Biomedical Engineering 2009, Munich, Germany, pp. 506-509, 2009.
- [23] M. Levy, J. Mizrahi, and Z. Susak, "Recruitment, Force, and Fatigue Characteristics of Quadriceps Muscles of Paraplegics Isometrically Activated by Surface Functional Electrical Stimulation," J. Biomed. Eng., vol. 12, pp. 150-156, 1990.
- [24] M. Ferrarin, A. Pedotti, "The Relationship between Electrical Stimulus and Joint Torque: A Dynamic Model," IEEE Trans. Rehabil. Eng., vol. 8, pp. 342-352, 2000.
- [25] R. Kobetic and E. B. Marsolais, "Synthesis of Paraplegic Gait with Multichannel Functional Neuromuscular Stimulation," IEEE Trans. Rehabil. Eng., vol.2, no. 2, pp. 66-79, 1994.