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ANALYTICAL MODEL OF THE THRESHOLD VOLTAGE V_{TH}, SUBTHRESHOLD SWING AND DRAIN INDUCED BARRIER LOWERING (DIBL) FOR A NEW DEVICE STRUCTURE OF CYLINDRICAL GATE MOSFET

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ABSTRACT

In this work, 2D analytical and numerical modeling of surface potential, threshold voltage V_{th} and drain induced barrier lowering (DIBL) for a new structure of surrounding gate MOSFET are presented. This new structure obtained by combined dual material gate graded channel and dual oxide thickness shows good immunity in the nanoscale regime versus short channel effects (SCE). The characteristic of the new model are investigated in terms of surface potential, threshold voltage and DIBL. The results of simulation show that the use of two oxide thickness with the small thickness at the source side could significantly reduce short channel effects such as threshold voltage, and DIBL. It is also revealed that a lowering gate oxide thickness, a small silicon channel radius are needed to improve device characteristic. Analytical models for all parameters are validated using a rigorous numerical calculation and compared to others devices engineering.

Keywords: *Dual Metal Gate (DMG), Dual Oxide Thickness (DOT), Graded Channel (GC), Drain Induced Barrier Lowering (DIBL)*

1. INTRODUCTION

The growth of the semiconductor industry depends for now on its ability to miniaturize transistors. The objective of the approach is to deliver better performances at lower cost. The increase of the integration density and improved performance are made possible by reducing the size of transistors. The characteristic size of a transistor which distinguishes a generation of transistors is the length of gate L [1] .The decrease of the dimension of channel generates some adverse effects; these effects are called short channel effects. SCE includes threshold tension roll-off and drain induced barrier lowering (DIBL), drive ability degradation and hot carrier effect (HCE) impose a physical limit on the ultimate performance of the traditional planar metal-oxide-semiconductor field effect transistors (MOSFETs).

To minimize short channel effects, the devices with multi-gate have been proposed, such as double gate, triple gate or surrounding gate MOSFET [2, 3, 4]. The surrounding-gate MOSFET structure offers a better control of the electrostatic potential while appearing with the other structures [5].

The quantum mechanical effects (QMEs) become significant and play a dominant role in determining the device performance when the dimension of the thin film silicon layer is thinner than 15nm. In this work, as the thickness of the Si film t_{Si} is considered to be equals to 20nm (larger than 15nm), thus it is a good approximation to ignore the channel quantization in this work.

The threshold voltage roll-off can be reduced using graded channel doping GC, the doping in the channel is kept high in region 1 near the source side and low in region 2 near the drain side [6].

The use of two gate materials with different work functions gives a step in the surface potential leading the electric field peak near the drain is lowered considerably, and therefore hot carrier effect HCE is reduced. In addition, the dual-

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material gate achieves simultaneous suppression of SCE, and the performance improvement is dependent on the work function difference [7, 8].

In this manuscript, dual-material gate and gradual Channel with two different thickness oxide [9] are combined in this new device structure as shown in Figure 1, which the gates has two metal (M_1 and M_2) with different work functions, an oxide structure with two different layers oxide t_{ox1} and t_{ox2} and a graded channel with two different doping (N_H and N_L) (H, high; L, low).

In this work, analytical model of threshold voltage V_{th}, subthreshold swing SS and drain induced barrier lowering (DIBL) are developed by solving 2D Poisson equation of surface potential. Moreover, to accurately predict the characteristics of DMG-GC-DOT, the effects of varying the device parameters (such as voltage drain/source and radius of channel) on the structure performance has also been studied. The analytical model demonstrates that the DMG-GC-DOT MOSFET structure presents the performance significantly improved. The results of analytical modeling are in good agreement with the numerical simulation.

This study aims to investigate threshold voltage, subthreshold swing SS and DIBL of the new device of MOSFET cylindrical gate. This paper is organized as follows: An analytical analysis of surface potential, threshold voltage and subthreshold swing for DMG-GC-DOT MOSFET will be presented in Section 2. Section 3 presents the results and discussion of new model on the basis of the solution of the Poisson equation. Finally, conclusion will be made in Section 4.

2. MODEL DERIVATION

Figure 1(c) shows the new structure (DMG-GC-DOT) MOSFET, the gate materials have two metal M_1 and M_2 with lengths L_1 and L_2=L-L_1 respectively, the Channel is divided into two regions, a first heavily doped on the side of the source, and a second weakly doped on the side of the drain and the thickness oxide t_{ox1} in the rest of the channel in region L_1 is large than t_{ox2} in region L_2=L-L_1.

Analytical and numerical analysis of surface potential and threshold voltage for DMG-GC-DOT MOSFET are compared to others device such as of DMG, and DMG-DOT MOSFET.

2.1 Surface Potential Model

To model the short channel effects, 2D Poisson equation is solved following the cross-sectional and longitudinal component of the channel. Presuming that the impact of fixed charges and charge carriers can be ignored on electrostatics of the channel.

The equation of the electrostatic potential $\varphi_i(r,z)$ of the canal in cylindrical coordinates is given as:

$$\frac{1}{r}\frac{\partial}{\partial}\left(r\frac{\partial\varphi_i(r,z)}{\partial r}\right)+\frac{\partial^2\varphi_i(r,z)}{\partial z^2}=\frac{qN_i}{\varepsilon_{si}} \quad (1)$$

$$0\le z\le L,\ 0\le r\le\frac{t_{si}}{2}$$

Where q is the load electrostatic ε_{si} represents the electrical permittivity of silicon, $\varphi_i(r,z)$ is the surface potential, N_i is the concentration of dopants: N_1=N_H and N_2=N_L.

To resolve (1), considering a profile of parabolic potential in the direction of the effect of the field, that is to say the radial direction to the channel. The potential is therefore written in the following manner:

$$\varphi_i(r,z)=p_{i0}(z)+p_{i1}(z).r+p_{i2}(z).r^2 \quad (2)$$

Where $p_{i0}(z)$, $p_{i1}(z)$ and $p_{i2}(z)$ are functions of z only, this coefficients are found by applying the boundary conditions for the potential as well as for the electric field at the level of silicon interfaces-oxide.

Then, the boundary condition for the electric field allows to obtain $p_{i1}(z)$ and $p_{i2}(z)$. In effect, by deriving (2), $p_{i1}(z)$ is obtained which corresponds to the electric field at the level of the interface between the silicon and the oxide from above. This field is also equal to the field through the oxide layer of gate above

$$\left(\frac{\partial\varphi_i(r,z)}{\partial r}\right)_{r=0}=0=p_{i1}(z)$$

At the oxide-silicon interface, the electric flux is given as

$$\left(\frac{\partial\varphi_i(r,z)}{\partial r}\right)_{r=\frac{t_{si}}{2}}=\frac{c_{ox_i}}{\varepsilon_{si}}\left(V_{GS}+V_{FB_i}+\varphi_{si}(z)\right)=p_{i2}(z)t_{si}$$

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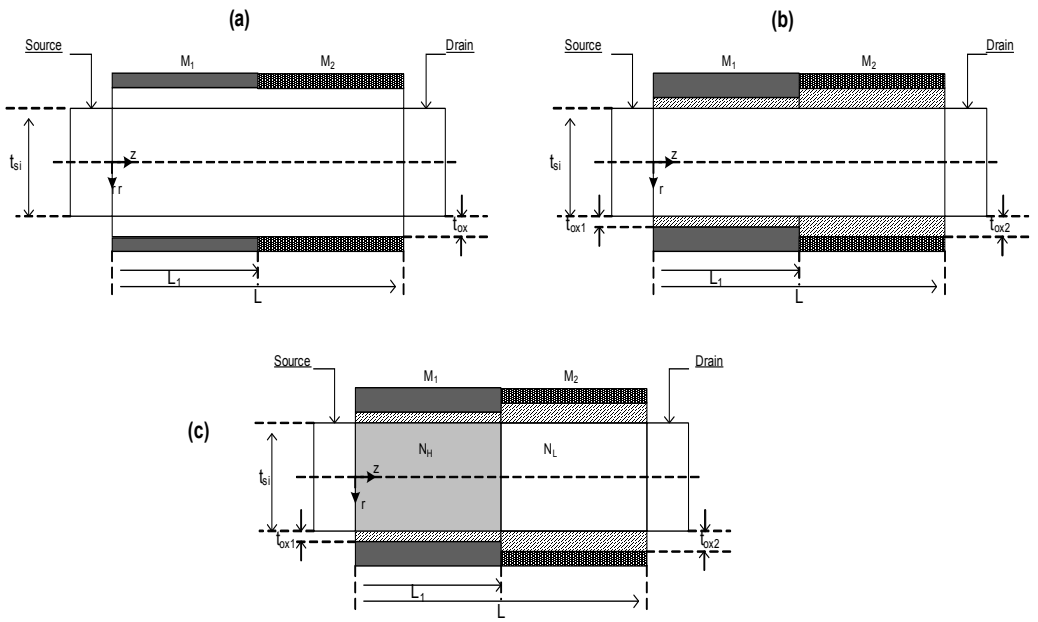

Fig. 1 Cross-Sectional Views Of Various Device Design Engineering On SG MOSFET. (a) DMG, (b) DMG-DOT, (c) DMG–GC–DOT

V_{FBi} defined as the voltage of flat band taking into account the difference of the work of the silicon and of the material of the electrode of the gate they are presented as:

$$V_{FB_1} = \varphi_1 - \varphi_{siH} \text{ , } V_{FB_2} = \varphi_2 - \varphi_{siL}$$

Where φ_1 is the work functions of M_1 and φ_2 is the work functions of M_2, respectively, and φ_{siH} and φ_{siL} are the work functions of the region L_1 and L_2, respectively.

Where: $c_{oxi} = \dfrac{2\varepsilon_{ox}}{t_{si} \ln\left(1 + \dfrac{2t_{oxi}}{t_{si}}\right)}$ is the oxide capacitance of slice oxide (i=1, 2), ε_{ox} the dielectric constant of SiO_2 gate oxide, and t_{ox1} and t_{ox2} are the oxide layers of region L_1 and $L\text{-}L_1$, respectively, V_{GS} is the gate voltage –Source.

In substituting (2) in (1), an ordinary differential equation on the single plan of the surface potential is obtained and is reduced as following:

$$\frac{\partial^2 \varphi_{si}(z)}{\partial z^2} - \lambda_i^2 \varphi_{si}(z) = D_i \quad \text{i=1, 2} \qquad (3)$$

Where $\lambda_i = \sqrt{4c_{oxi}/\varepsilon_{si}t_{si}}$ is characteristic length and $D_i = \dfrac{qN_i}{\varepsilon_{si}} - \lambda_i^2 \left(V_{GS} - V_{FBi}\right)$

The boundary conditions for the potential φ must meet the continuity of the potential and the continuity of the normal component of the vector electric displacement to interfaces $Si\text{-}SiO_2$

$\varphi_1(0,0) = V_{bi1}$, where V_{bi1} is the voltage of junction: Source / Channel or drain / Channel.

$\varphi_2(0,L) = V_{bi2} + V_{ds}$,Where V_{DS} is the drain source voltage and L is the device channel length.

The general solution for the surface potential has the form:

$$\varphi_{si}(z) = A_i \exp(-\lambda_i z) + B_i \exp(\lambda_i z) - \frac{D_i}{\lambda_i^2} \qquad (4)$$

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The use of boundary conditions, the coefficients A_i and B_i (i = 1, 2) can be determined as:

$$A_1 = V_{bi_1} + \frac{D_1}{\lambda_1^2} - B_1$$

$$A_2 = \left(\left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^2}\right) - B_2\exp(\lambda_2 L)\right)\exp(\lambda_2 L)$$

$$B_2 = \frac{U_2}{U_0},\ B_1 = \frac{U_1}{U_0},\ U_2 = a_0 C_2 - c_0 C_1,$$

$$U_1 = d_0 C_1 - b_0 C_2, U_0 = a_0 d_0 - b_0 c_0$$

$$C_1 = \left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^2}\right)\exp(-\lambda_2 L_1) - \left(V_{bi_1} + \frac{D_1}{\lambda_1^2}\right)\exp(-\lambda_2 L)\exp(-\lambda_1 L_1) + \left(\frac{D_1}{\lambda_1^2} - \frac{D_2}{\lambda_2^2}\right)\exp(-\lambda_2 L)$$

$$C_2 = -\lambda_2\left(V_{bi_2} + V_{ds} + \frac{D_2}{\lambda_2^2}\right)\exp(-\lambda_2 L_1) + \lambda_1\left(V_{bi_1} + \frac{D_1}{\lambda_1^2}\right)\exp(-\lambda_2 L)\exp(-\lambda_1 L_1)$$

The differentiation of surface potential is carried out along the channel to get the distribution of the Electric Field disposed by:

$$E_i(z) = -A_i\lambda_i\exp(-\lambda_i z) + B_i\lambda_i\exp(\lambda_i z)$$

$$0 \le z \le L,\quad \text{i=1, 2}$$

2.2 Threshold Voltage Model

The threshold voltage is determined from the expression of the surface potential by using the following condition:

$$\varphi_{si,\min}\Big|_{V_{gs}=V_{th}} = 2\varphi_B$$

Where φ_B represents the difference between the Fermi level and the intrinsic level of the substrate and is equal to $\varphi_B = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$.

$\varphi_{si,\min}$ represents the minimum of the surface potential also called virtual cathode, its location on the axis (z) can be analytically obtained by the resolution of the equation of $\frac{d\varphi_{s1,2}}{dz} = 0$ (estimated the minimum surface potential in the region L_1, where the doping concentration is high) to obtain the following expression:

$$z_{\min} = \frac{1}{2\lambda}\sqrt{\frac{B_1}{A_1}}$$

$\varphi_{si,\min}$ can be deducted from Equation (4):

$$\varphi_{si,\min} = 2\sqrt{A_1 B_1} - \frac{D_1}{\lambda_1^2} \qquad (5)$$

The threshold voltage can be given as:

$$V_{TH} = \left(-\eta + \sqrt{\eta^2 - 4\sigma\xi}\right)/2\sigma$$

Where:

$$a_0 = 2\exp(-\lambda_2 L)\sinh(\lambda_1 L_1),$$
$$b_0 = 2\sinh(\lambda_2(L - L_1))$$
$$c_0 = 2\lambda_1\exp(-\lambda_2 L)\cosh(\lambda_1 L_1),$$
$$d_0 = -2\lambda_2\cosh(\lambda_2(L - L_1)),$$
$$U_0 = a_0 d_0 - b_0 c_0, e_0 = \exp(-\lambda_1 L_1),$$
$$e_1 = \exp(-\lambda_2 L_1), e_2 = \exp(-\lambda_2 L)$$
$$a_1 = \frac{(qN_{aH})}{\varepsilon_{si}\lambda_1^2} + V_{FB_1}, \qquad a_2 = \frac{(qN_{aL})}{\varepsilon_{si}\lambda_2^2} + V_{FB_2},$$
$$b_1 = e_2 e_0(V_{bi_1} + a_1), \qquad c_1 = \lambda_1 b_1,$$
$$b_2 = e_1(V_{ds} + V_{bi_2} + a_2), c_2 = \lambda_2 b_2$$
$$E = (d(e_2 e_0 - e_1) + b(\lambda_1 e_2 e_0 - \lambda_2 e_1))/U_0$$
$$D = (d(b_2 - b_1 + e_2(a_1 - a_2)) + b(c_2 - c_1))/U_0$$
$$\sigma = -(4E^2 + 4E + 1)$$
$$\eta = 4(V_{bi_1} + a_1) + E4D - 8DE + 2a_1 + 4\varphi_B$$
$$\xi = 4(V_{bi_1} + a_1)D - 4D^2 - a_1^2 - 4a_1\varphi_B - 4\varphi_B^2$$

2.3 Subthreshold Swing

The subthreshold swing (SS) is defined by:

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$$SS = \frac{\partial V_{gs}}{\partial \log I_{ds}} = V_t \ln(10) \left[\frac{\int_0^{t_{si}/2} e^{\frac{\varphi_{\min}}{V_t}} \frac{\partial \varphi_{\min}}{\partial V_{gs}} dr}{\int_0^{t_{si}/2} e^{\frac{\varphi_{\min}}{V_t}} dr} \right]^{-1}$$

Unfortunately, it is almost impossible to obtain an analytical solution for this integral, so with a simplifying approximation of the equation, the subthreshold swing can expressed as:

$$SS = \frac{KT}{q} \ln(10) \left(\frac{\partial \varphi_{si,\min}}{\partial V_{GS}} \right)^{-1}$$

The Equation (5) is used to obtain:

$$\left(\frac{\partial \varphi_{si,\min}}{\partial V_{GS}} \right) = 1 + (A_1 B_1)^{\left(\frac{-1}{2}\right)} (A_1 P_1 + B_1 P_2)$$

Where

$$P_1 = \frac{d_0}{U_0} \left(\exp\left(-(\lambda_2 L + \lambda_1 L_1)\right) - \exp(\lambda_2 L_1) \right)$$

$$- \frac{b_0}{U_0} \lambda_2 \left(\exp(-\lambda_2 L_1) - \exp\left(-(\lambda_2 L + \lambda_1 L_1)\right) \right)$$

$$P_2 = -1 - P_1$$

3. RESULTS AND DISCUSSION

In order to analyze the validity of the DMG-GC-DOT MOSFET design, the DMG and DMG-DOT devices are studied, on the basis of the solution of the Poisson equation and the potential of surface that represents the first step of the model and therefore, must be as accurate as possible. Then the validity of the model of the threshold voltage is examined by using a new approach for the determination of the threshold condition. In final, the validation of the model of the drain induced barrier lowering.

To verify the proposed analytical model, surface potential distribution versus the channel length was plotted and compared with numerical results. For analytical modeling, the doping concentrations in two regions are: $N_H = 3.10^{17} cm^{-3}$, $N_L = 4.10^{16} cm^{-3}$.

In the figure (2), the variation of the surface potential is described for the model DMG-GC-DOT in comparison with DMG and DMG-DOT for:

$L = 100nm$, $L_1 = 25nm$, $t_{si} = 20nm$,

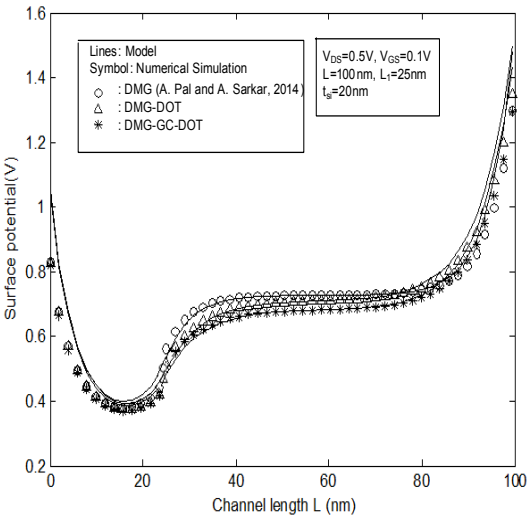

Fig. 2 Surface Potential Along The Channel For DMG-GC-DOT, DMG-DOT And DMG (A. Pal and A. Sarkar)

$t_{ox1} = 2nm$, $t_{ox2} = 4nm$, $V_{GS} = 0.1V$,
$V_{DS} = 0.5V$, $N_d = 2.10^{20} cm^{-3}$,
$N_L = 4.10^{16} cm^{-3}$, $N_H = 3.10^{17} cm^{-3}$,
$\varphi_1 = 4.8$ and $\varphi_2 = 4.4$.

It can see according to the figure that the minimal surface potential occurs in the first region of DMG-GC-DOT. For DMG-GC-DOT, there is an additional step of potential near the limit of the two metal gates which indicates a better control of the silicon region near the source from drain voltage of DMG-GC-DOT.

Figure 3 shows the variation of the surface potential according to the channel length for different values of V_{GS} and t_{si}, the decrease of the diameter of the cylindrical channel causing the potential of surface with dish on the region more channel which indicates a better control of the loads of the channel. Besides, a good concordance between the results of the new model and those of digital simulation.

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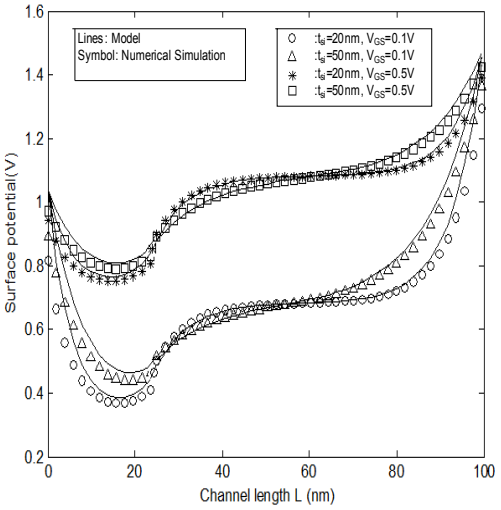

Fig. 3 Variation Of The Surface Potential Along The Channel For Different Values Of t_{si} And Different Values Of V_{GS}

Figure 4 illustrates the threshold voltage along the channel for DMG–GC–DOT, DMG and DMG-DOT. It is clear that the degradation of the threshold voltage increases with the narrowing of the canal, also the threshold voltage decreases quickly in DMG-DOT and DMG compared to DMG-GC-DOT, this is due to a loss of the controllability of the gate on the load of the channel.

Figure 5 shows the variation of threshold voltage for various polarization of drain voltage. Nevertheless, there is a decrease in the degradation of the threshold voltage, relatively to the decrease in the value of drain voltage. Thus, a reduction of V_{DS} is necessary to obtain a reduction of the effects of short channel (SCE).

The figure 6 illustrates the threshold voltage of DMG-GC-DOT versus channel length with various radius of the silicon channel. A small radius of the silicon channel leads to less threshold voltage.

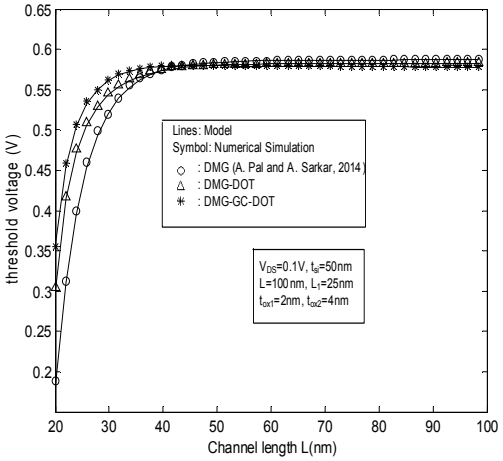

Fig. 4 Comparison Of Threshold Voltage V_{TH} As A Function Of Channel Length L For DMG–GC–DOT, DMG And DMG-DOT

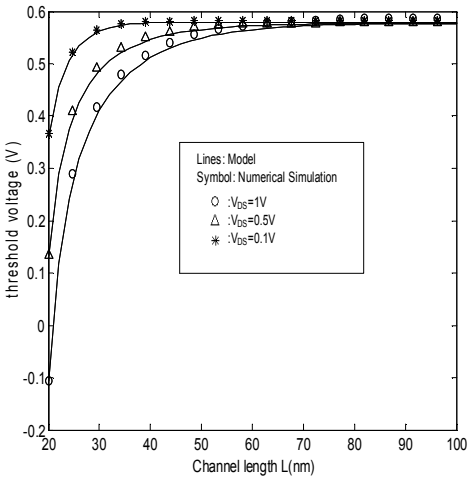

Fig. 5 Variation The Threshold Voltage On The Length Of The Channel For Different Values Of Drain Voltage

Figure 7 presents the subthreshold swing according to the length for different values of silicon radius. The subthreshold swing is perceptible within 40nm and becomes very important for a length of 20 nm. Then observe the impact of silicon radius on the decrease in the subthreshold swing.

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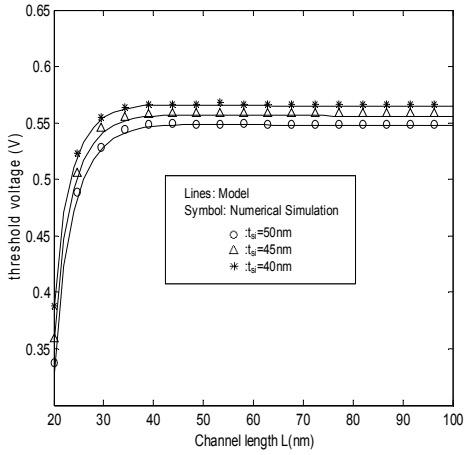

Fig. 6 Threshold Voltage Along The Channel Length For Different Values Of Silicon Radius

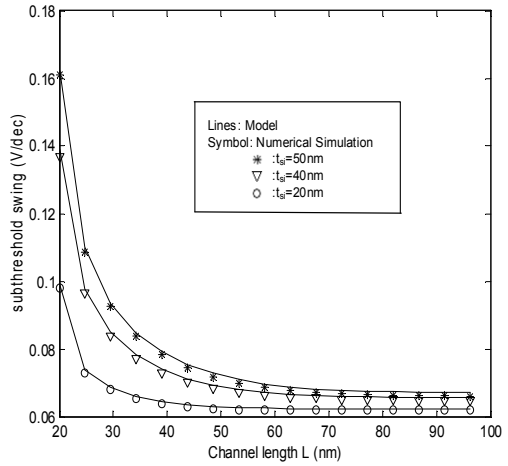

Fig. 7 Subthreshold Swing Versus The Channel Length For Different Silicon Radius

The figure 8 below shows the effect DIBL as a function of the length for DMG-GC-DOT, DMG and DMG-DOT. The DIBL is a very important parameter which reflects the effect of boring on the short canals, it is obtained by performing the difference on the threshold voltage for two drain voltages, a first high enough and a second very low such as $\Delta V_{th}/\Delta V_{ds}$ where $\Delta V_{th} = V_{th}\big|_{V_{ds}=0} - V_{th}\big|_{V_{ds}=2}$ and $\Delta V_{ds} = 2V$ .The phenomenon of the lowering of the barrier is perceptible to less than 40 nm and becomes very important for a length of 20 nm. There is then the impact of the use of two layers of oxide on the decrease in the DIBL in the Channels ultracourts and of this fact, the improvement of the controllability of the gate.

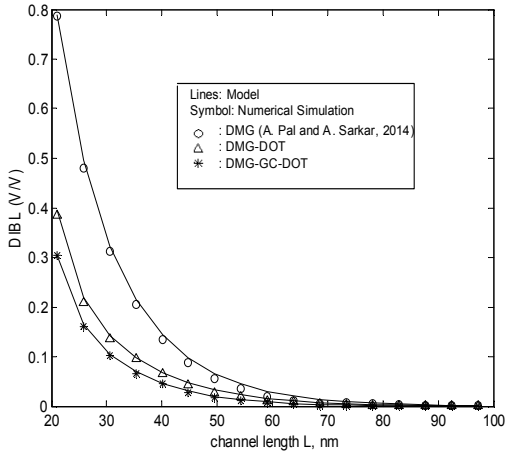

Fig. 8 Variation Of DIBL As A Function Of Channel Length L For DMG-GC-DOT, DMG-DOT And DMG MOSFET

It is evident from figure 9 that a reduction in channel radius not only improves threshold voltage performance, but it also improves the DIBL performance considered as major SCEs. A nice agreement is observed between our proposed model and numerical simulation

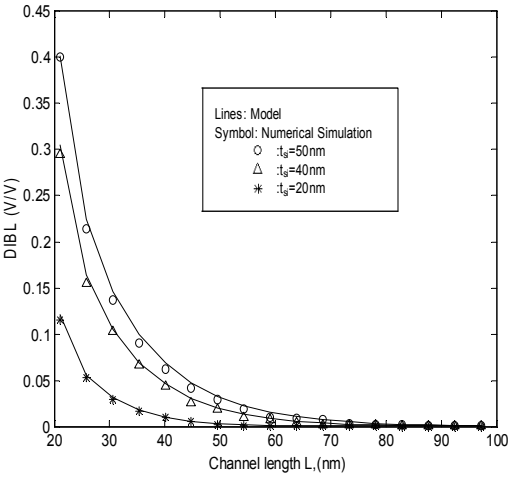

Fig. 9 Compares the Variation of DIBL versus Channel Length for DMG-GC-DOT MOSFET for Different Radius Silicon with t_{ox1}=2nm and t_{ox2}=4nm

4. CONCLUSION

In summary, an analytical analysis of the surface potential, threshold voltage and DIBL are developed for the new structure MOSFET (DMG-GC-DOT), by solving 2D Poisson's equation in the two channel regions. It has been demonstrated that

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DMG-GC-DOT MOSFET provides a better immunity to SCEs as compared to other structure MOSFET. It can be concluded, that reduction in oxide thickness, channel radius and bias voltage causes better threshold-voltage and DIBL performance of DMG-GC-DOT devices. The validity of the model was proved using numerical simulations. The results obtained showed a good Performance of the DMG-GC-DOT transistor up to a length of 30 nm, below this length, the short channel effects become very important.

The results also uncovered the contribution of two layers of oxide (one smaller than the other) in increasing the controllability of the gate and thereby reducing the short-channel effects. This gives the possibility of a stronger Integration, up to less than 20nm.

This study also revealed the possibility of a high value of the dielectric constant which makes it possible to reduce the thickness of the equivalent oxide and to increase the physical thickness of the dielectric, beyond the injection length of the load carriers by tunneling.

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