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OPTIMIZATION OF 60-GHZ DOWN-CONVERTING CMOS DUAL-GATE MIXER USING ARTIFICIAL BEE COLONY ALGORITHM

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ABSTRACT

In this article, we present an application of the Artificial Bee Colony (ABC) Algorithm for the optimal design of RF analog circuit designed to the telecommunication systems. This work illustrates down-conversion CMOS mixer with high conversion gain and improved Noise Figure (NF). After a presentation of the used algorithm, an application the optimum sizing of a dual-gate mixer (DG-MOSFET) is introduced. The proposed mixer converts input radio frequency signal of 60GHz to frequency output signal of 10GHz. The local oscillator frequency is 50GHz and a local oscillator power considered at 0dBm. The conversion gain of this mixer is -1.87dB and noise is 0.97dB. The results are validated by simulation under ADS and compared with already published works.

Keywords: *Optimization, ABC Algorithm, DG-MOSFET, Frequency Mixer, CMOS 45nm.*

1. INTRODUCTION

Miniaturization and integration of device and electronic circuits continue to increase which makes the circuit design, more and more, very complicated. Optimal sizing of analog circuitry remains the bottleneck in the flood of analog design, which grows designers to invoking conventional engineering methods and approaches based on statistics [1].

The problem with these methods is that they are often very slow and they do not guarantee convergence to a global optimum. The use of an automatic method of sizing of analog components, to accelerate efficiently the process of analog design circuits is required.

Methods based on the use of heuristics appeared then to resolve optimization problems [2]. Among these heuristics, some are adaptable to many different problems referred to as Meta heuristics. They always offer approximate solutions for optimization problems at a very reasonable times [3]. Some (meta-) heuristics are also proposed in the literature and are used by the designers, such as Tabu Search [4], Genetic Algorithms (GA) [5], local search (LS) [6], etc. However, the metaheuristics that gave the best results are those of nature inspired, they are inventive, resourceful, efficient, and easy to use and are known as SI: ‘Swarm Intelligence Techniques’ [7]. The SI techniques focus on animal conduct in order to develop some meta-heuristics which can mimic their problem resolution abilities, such as Particle Swarm Optimization (PSO) [8], Ant Colony Optimization (ACO) [9,10,11] and, recently, Artificial Bee Colony (ABC) [12].

In this work, we focus on the use of an Artificial Bee Colony (ABC) to the optimal sizing of CMOS dual-gate frequency mixer for the Radio Frequency (RF) field.

The remainder of the paper is structured as follows: The second section deals with an overview of the ABC technique. The third section presents an application example dealing with the optimal sizing of a CMOS dual-gate mixer.

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The forth section highlights the results of the optimization, finally, concluding remarks are given in the last section.

2. ARTIFICIAL BEE COLONY ALGORITHM

Artificial Bee Colony (ABC) algorithm was proposed by Karaboga in 2005, for optimizing numerical problems [13, 14]. It is a population based stochastic optimization algorithm inspired by the intelligent collective foraging behavior observed in the bee colony.

The position of a food source represents a possible solution to the optimization problem and the nectar amount of a food source represents the quality (fitness) of the associated solution. The colony of artificial bees contains three groups of bees [15]:

The employed bees
The onlooker bees
The scout bees

First of all, the set of food source positions is generated randomly as $x_i(i=1,\ldots,SN)$, which is a D-dimensional vector. D corresponds to the number of optimization parameters. The variables contained in each vector must be optimized.

After initialization, the population of solutions is subjected to repeated cycles, MCN is C=1, 2…MCN the maximum cycle number. These cycles represent the research process made by the employed bees, the onlooker bees and scout bees. At the end of the research process, the employed bees share information on nectar food sources and their locations with onlooker bees that evaluate these information from all employed bees and choose food sources according to the Pi probability value, associated with this source, calculated by the following expression (1):

$$p_i = \frac{fit_i}{\sum_{n=1}^{SN} fit_n} \qquad (1)$$

Where fit_i is the fitness value of the solution (i) which is proportional to the amount of the nectar of the food source in the position (i).The employed bees looking in the vicinity of the previous source x_i. New sources v_i that offer more nectar. So as to produce a candidate food position from the old one in memory, the ABC uses the following expression (2):

$$v_{ij} = x_{ij} + \phi_{ij}\left(x_{ij} - x_{kj}\right) \qquad (2)$$

Where $k \in \{1,2,\cdots,BN\}$ (BN is numbers of employed bees) and $j \in \{1,2,\cdots,SN\}$ are randomly selected indices. Although k is randomly determined, it must be different from i. ϕ_{ij} is a random number belonging to the interval [-1, 1], it controls the production of a food source in the vicinity of x_{ij}.

The food source whose nectar is abandoned by the bees, scouts replace it with a new source: If, during a predetermined cycle number called limit, a position cannot be improved, then this food source is assumed to be abandoned. Assume that the abandoned source is x_i and $j \in \{1,2,\cdots,D\}$, then the scout discovers a new food source to be replaced with x_i. This operation can be defined as in (3):

$$x_i^j = x_{min}^j + \text{rand}(0,1)\left(x_{max}^j - x_{min}^j\right) \qquad (3)$$

The increase in the number of scouts encourages the exploration process while the increase of onlookers on a food source encourages the exploitation process.

The main procedures of the algorithm are given below:

Initialize
REPEAT

- Move the employed bees into their food sources and determine their nectar amounts.
- Place the onlookers into the food sources and determine their nectar amounts.
- Move the scouts for searching new food sources.
- Memorize the best food source found so far.

UNTIL (the requirements are met).

It is clear, from the above explanation, that in the ABC algorithm, there are four control parameters

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used: The number of the food sources which is equal to the number of employed or onlooker bees (SN), the value of limit and the maximum cycle number (MCN) [15].

Detailed pseudo-code of the ABC algorithm is given below [15]:

Initialize the population of solutions
$x_{i,j} \quad (i = 1 \cdots SN, \quad j = 1 \cdots D)$
Evaluate the population
Cycle=1
Repeat

- ✓ Produce new solutions $v_{i,j}$ for the employed bees by using (2) and evaluate them.
- ✓ Apply the greedy selection process.
- ✓ Calculate the probability values $P_{i,j}$ for the solutions $x_{i,j}$ by equation (1).
- ✓ Produce the new solutions $v_{i,j}$ for the onlookers from the Solutions $x_{i,j}$ selected depending on $P_{i,j}$ and evaluate them.
- ✓ Apply the greedy selection process.
- ✓ Determine the abandoned solution for the scout, if exists, and replace it with a new randomly produced solution $x_{i,j}$ by equation (3).
- ✓ Memorize the best solution achieved so far
- ✓ Cycle=cycle+1

Until cycle=MCN

ALGORITHM 1: Pseudo Code for The ABC Algorithm

3. APPLICATION EXAMPLE

The proposed MATLAB implemented algorithm parameters are given in Table 1. The number of iterations of the ABC algorithm is equal to 10000.

Table 1: The ABC Algorithm Parameters

Parameter name	Value
Swarm size(NP)	100
Number of Onlooker bees	50% of The swarm
Number of employed bees	50% of The swarm
Number of food sources	NP/2

The ABC algorithm is applied to optimal sizing of the frequency mixer presented by the figure1 (See fig 1 in the appendix (A)).

In this structure, the RF signal is applied to RF gate transistor, and LO signal at LO gate transistor. This topology can realized with two cascode transistors. RF transistor operate in saturation region for giving the high transconductance (gm_rf) that is in function with drain voltage(Vds) of RF transistor and controlled by LO signal which its operated in linear region and work as switch.

One of advantages stated above cascode mixer has another major advantage over single device mixer is that the RF and LO signals can be applied to the separate gate to achieve improved isolation [16].

3.1 Calculations and Equations of Mixer

Output resistor calculation of mixer is determinate using the equivalent model of mixer circuit in small signal presented by the figure2 (See fig 2 in the appendix (A)):

The conversion gain is done by equation (4):

$$Conv\_Gain = \frac{\left| V_{IF}(t) \right|_{a(w_{RF} - w_{OL})}}{\left| V_{RF}(t) \right|_{a(w_{RF})}} \quad (4)$$

$$= \frac{\frac{2}{\pi} R_{out} \cdot g_{m\_rf} V_{RF}}{V_{RF}}$$

Then

$$G_v = \frac{2}{\pi} g_{m\_rf} R_{out}$$

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And we have:

$$R_{out} = \frac{V\_IF}{If}\Big|_{V\_RF=0} \qquad (5)$$

To calculate R_{out} of our circuit, we must short-circuit the entrance V_RF, then the equivalent model becomes (See fig 3 in the appendix (A)).

To simplify the calculations, we use:

$$Z_1 = [(R_S // C_{gs\_rf}) + C_{gd\_rf}] // r_{0\_rf} // C_{gb\_rf} // C_{gs\_ol} \qquad (6)$$

$$Z_2 = C_{gd\_ol} // R_2 // C_{gb\_ol} \qquad (7)$$

The schema of Fig.3 becomes:

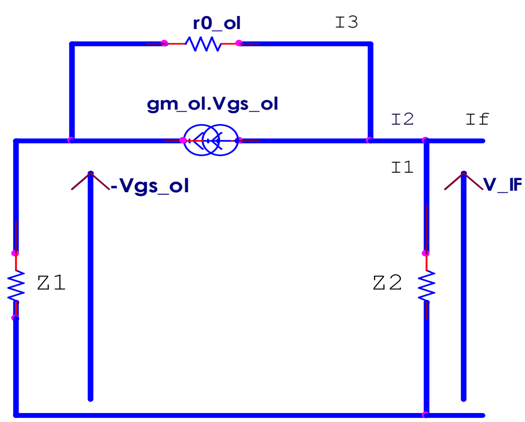

Fig 4: Equivalent model using equivalent Impedances

Finally, the expression of Rout will be after the calculations:

$$R_{out} = \frac{1}{\left[\frac{r_{0\_ol}+Z_2}{r_{0\_ol}Z_2} + \left(\frac{1+g_{m\_ol}r_{0\_ol}}{r_{0\_ol}}\right)\cdot\frac{-Z_1}{r_{0\_ol}+Z_1 \cdot r_{0\_ol} \cdot g_{m\_ol}+Z_1}\right]} \qquad (8)$$

Therefore, the conversion gain is:

$$G_V = \frac{2}{\pi} g_{m\_rf} \frac{1}{\left[\frac{r_{0\_ol}+Z_2}{r_{0\_ol}Z_2} + \left(\frac{1+g_{m\_ol}r_{0\_ol}}{r_{0\_ol}}\right)\frac{-Z_1}{r_{0\_ol}+Z_1 \cdot r_{0\_ol}g_{m\_ol}+Z_1}\right]} \qquad (9)$$

g_{m_rf} and g_{m_ol} are transconductance of RF and LO transistors respectively and R_s resistor of source. C_{gs}, C_{gd} and C_{gb} refer to parasitic grid to source capacitance, the grid to drain capacitance and the parasitic grid to bulk capacitance respectively.

3.2 Design Requirement and Specifications for Optimization

For analyzing the dual gate mixer performance, the gain function can be treated as multivariable nonlinear constrained optimization problem and is taken as the objective function for optimization with constraints.

Consider the optimization problems as follows:

Find X= { $x_1, x_2, x_3 \ldots x_d$ }

where $x_{lower\,(n)} \le x_n \le x_{upper\,(n)}$
$n = 1, 2, \ldots, d$

Minimize $F(\vec{X}),\ F(\vec{X}) \in R$

Subject to: $\vec{G}(\vec{X}) \le 0\ \ \vec{G}(\vec{X}) \in R^P$ And
$\vec{H}(\vec{X}) = 0\ \ \vec{H}(\vec{X}) \in R^Q$ (10)

(P) inequality constraints to satisfy, (Q) equality constraints to assure, m parameters to manage. $x_{Lower\,(n)}$ and $x_{upper\,(n)}$ are lower and upper bound vectors of the variable parameters, respectively.

In this section, we deal with the optimal sizing of a CMOS dual-gate Mixer structure regarding the voltage gain presented by the S21 parameter. The input and output matching (via the scattering parameters S11 and S22) and H(x) presents the imposed constraints (saturation of MOS transistors, NF, S11, S22, etc.).
Former to optimize the performances of Mixer, we considerate:

- F(x): The conversion gain function (Objval).
- X: Number of parameters of the problem to be optimized (d=13: $x_1, x_2, \ldots x_{13}$):

$W_{1,2}= x_1$, $L_{1,2}= x_2$, $W_{3,4}= x_3$, $L_{3,4}= x_4$, $L_{out}= x_5$, $R_{out}= x_6$, $Ce= x_7$, $Lg\_rf= x_8$, $L_s= x_9$, $R\_mirror= x_{10}$, $I_0= x_{11}$, $Lg\_ol= x_{12}$, $C_{out}= x_{13}$,

With:
(W_1, L_1), (W_3, L_3) are widths and lengths of RF and LO transistors respectively.
R_mirror: Resistor of current mirror
C_{out}, R_{out}, L_{out}: (LRC) tank parameters.
G(x) represents a set of inequality constraints
L_s inductor for source degenerated to be choice in consideration with linearity parameter
(Decreasing our mixer gain see APPENDIX (B)):

$$g_{meff}(Z_{deg}) = \frac{g_{m\_rf}}{1+g_{m\_rf}.Z_{deg}} \quad (11)$$

(See APPENDIX (B))

Minimization expressions of losses for LO signal:

$$(C_{OL}*L_{OL})-1/\omega^2=0$$

- H(x) represents equality constraints such as input and output matching (S11 and S22 to be less the -10dB, etc.) of the Mixer.

➢ The conditions of saturation of transistors, are presented by following expressions :

❖ Condition of saturation of M_{RF} transistor :

$$(V_{dd} - V_{tn}) \geq [\text{sqrt}(2*I_{ds(OL)}*L_{OL}/Un*Cox*W_{OL}) + \text{sqrt}(2*I_{ds(RF)}*L_{RF}/W_{RF}*Un*Cox) + I_0*R_{mirror}]$$

❖ Condition of saturation of M_{OL} transistor :

$$(I_0 * R_{mirror} - R_{out} * I_{ds(RF)}) + V_{tn} \leq 0$$

The others constraints required for the CMOS Mixer design was the following:

✓ F_{input}: $V\_RF = 0.001\sin(2*\pi*f_{RF}*t)$
$f_{RF} = 60$GHz
✓ LO : $V\_LO = 0.69+0.2\sin(2*\pi*f_{LO}*t)$
f_{LO}=50GHz with, Power_LO=0dBm
✓ Frequency range: 5~62 GHz
✓ Input impedance Zin: |Zin| = 50 ohm
✓ Voltage gain: To maximize
✓ NF with 50 ohm input matching < 3 dB

Therefore, to have optimal performances, the mixer circuit should satisfy the following conditions:

➢ The small size for M_LO transistor could certify a good switching comportment.

➢ The M_LO transistor must be in the linear area.

➢ The M_LO transistor must have a common mode equal to or proximate to its threshold voltage (V_{th}=0.69V) in order to better exploit the excursion of LO signal and to improve the switching operation.

➢ The M_RF transistor must operate in the saturation zone to ensure a high g_m transconductance and then a good conversion gain as will be demonstrated in the next section.

Table 2 presents the specifications of the circuit

Table 2: setting out

Parameter	Constraint
NF	< 3dB
||S11|&|S22|	< -10dB
|S21|	To maximize

4. RESULTS

The application of ABC algorithm gives the optimal values of the different variables of the circuit, which are represented in the table3.

Table 3: Optimal Dimensions

W_{RF}/L_{RF}	(µm/nm)	331.33/43.1
W_{OL}/L_{OL}	(µm/nm)	68.831/40
W_2/L_2	(µm/nm)	331.33/43.1
W_4/L_4	(µm/nm)	68.831/40
L_{Out}	(nH)	3.77
R_{Out}	(Ω)	695.95
Ce	(pF)	0.183
Lg_rf	(nH)	0.014
L_S	(nH)	0.993
R_mirror	(kΩ)	1.3877
I_0	(mA)	10.6
L_{g_ol}	(nH)	0.0932
C_{Out}	(pF)	17

In order to verify the validity of the results of simulations, which are shown in the following figure, are made in ADS 45nm technology with intermediate frequency F_IF = 10GHz, using the optimal values generated by the application of the ABC algorithm:

4.1 Conversion Loss (S21)

Fig 5 shows that the mixer has a conversion loss of -3.178dB.

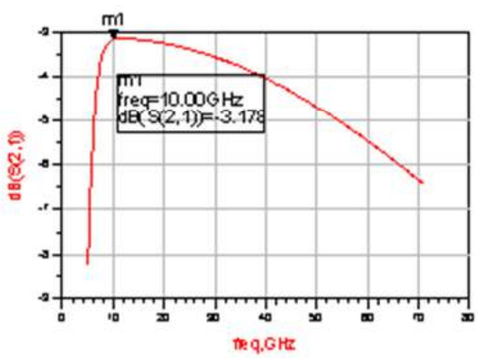

Fig 5: The Simulated Return Loss For The Proposed Cascode Mixer

4.2 Noise Figure (NF)

The Mixer noise figure simulated at 10 GHz is 1.241dB as shown in Fig 6.

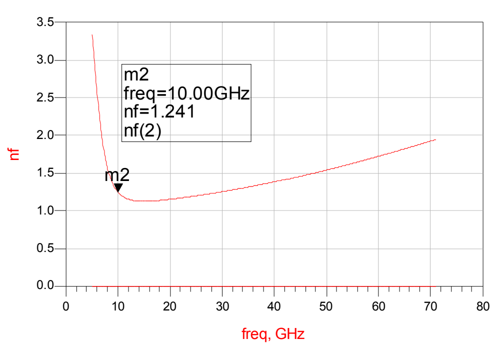

Fig 6: The Simulated Noise Figure For The Dual-Gate Mixer

4.3 S11-Forward Reflection

As shown in fig.7, we have good isolation and good matching input impedance less than -10dB in the RF frequency. The S11 parameter simulated at 60GHz is -14.399dB.

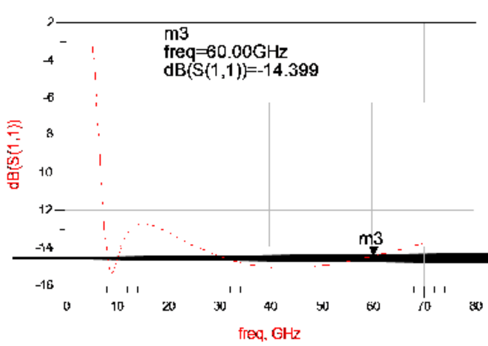

Fig 7: S11 Parameter versus Frequency

4.4 S22-Reverse Reflection

As shown in fig8, we have good isolation and good matching output impedance less than -10dB in the IF frequency (S22 at 10GHz is -10.056dB).

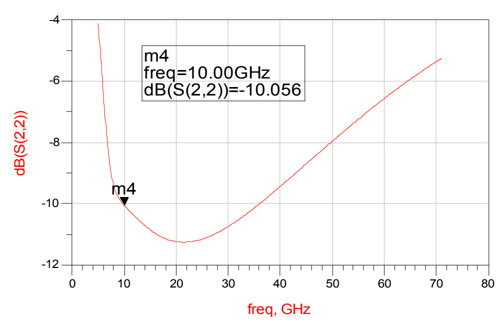

Fig 8: S22 Parameter versus Frequency

First, The S21 value in Figure5 is approximately near than the desired gain of [-3 to 2] dB in millimeter frequency range. Therefore, we notice that the result is relatively good for our circuit design in 45nm technology. Secondly, the most important design specification was getting a noise figure of 3dB or less. As shown in Figure 6, the NF measured for this particular design is about 1.241dB and hence meets the design requirement. Finally, The Mixer designed using

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the model has shown good matching at the input (S11≈-14dB) and output (S22≈-10dB).

To confirm the validity of the results generated by the ABC method. Figures 5, 6, 7, and 8 show ADS simulations performed using the sizes given in Table 3and they correspond to the results summarized in Table 4. The technology under consideration is 45nm CMOS technology with power supply equal to 1.2 V. We notice that simulation results are in good agreement with those obtained using ABC-matlab technique.

Table 4: Theoretical and Simulation Results

Parameter (dB)	ADS (Simulation)	ABC (Matlab)
S21	-3.178	-1.86623
NF	1.241	0.9687
S11	-14.399	-15.431
S22	-10.560	-10.024

In this case, the conversion gain has assumed to get much higher priority among other design specifications. Table 5 presents a comparison between results obtained using the proposed ABC algorithm and those proposed in the published works [17-18-19]. So, one can easily notice that ABC performances are the competitive (See table 5 in the appendix (A)).

5. CONCLUSION

The presented work proposes an approach for the optimal design of dual-gate Mixer using the Artificial Bee Colony optimization algorithm. The ABC technique was used to optimally sizing of elements forming the Mixer while satisfies the inherent and imposed constraints and maximizes the objective function (conversion gain). Obtained sizing and reached results were first validated through ADS simulations and then compared to those presented in published works. It is shown that the mixer circuit is optimally designed for power gain of -1.87dB and noise figure of 0.97dB. Thus, the design with this optimization approach is useful in finding circuit element values speedily reducing the RF circuit designer time. Now, we are focusing on transforming the proposed ABC mono-objective algorithm into a multiobjective one.

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APPENDIX (A)

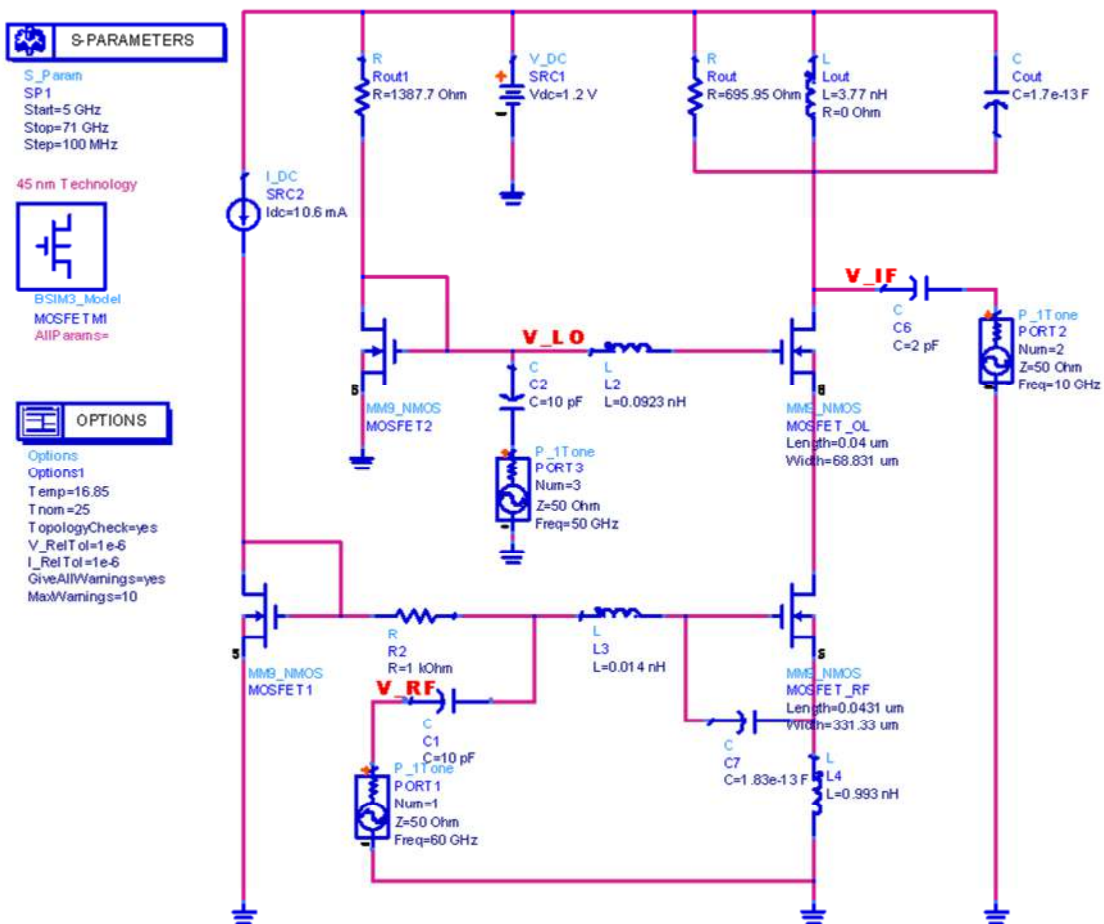

Fig 1: CMOS Dual-Gate Mixer (DG-MOSFET)

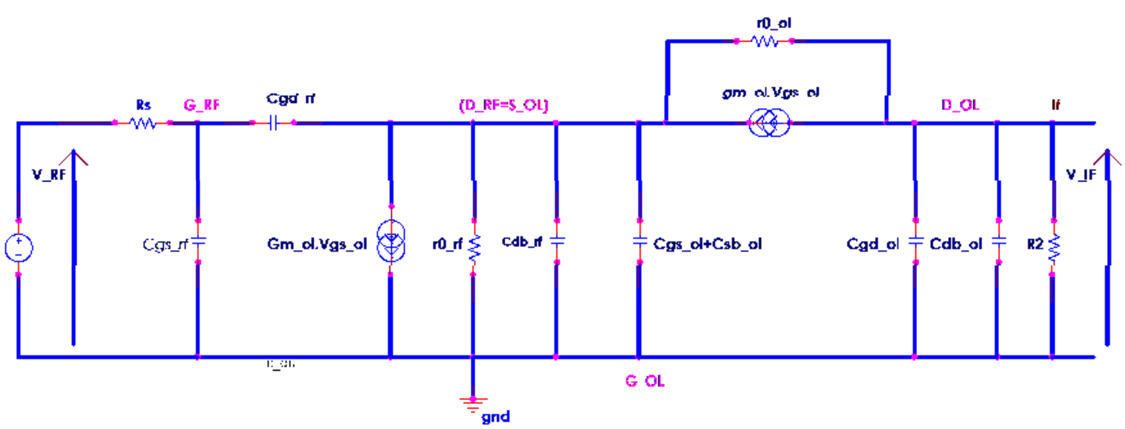

Fig 2: Equivalent Model of CMOS Dual-Gate Mixer in Small Signals

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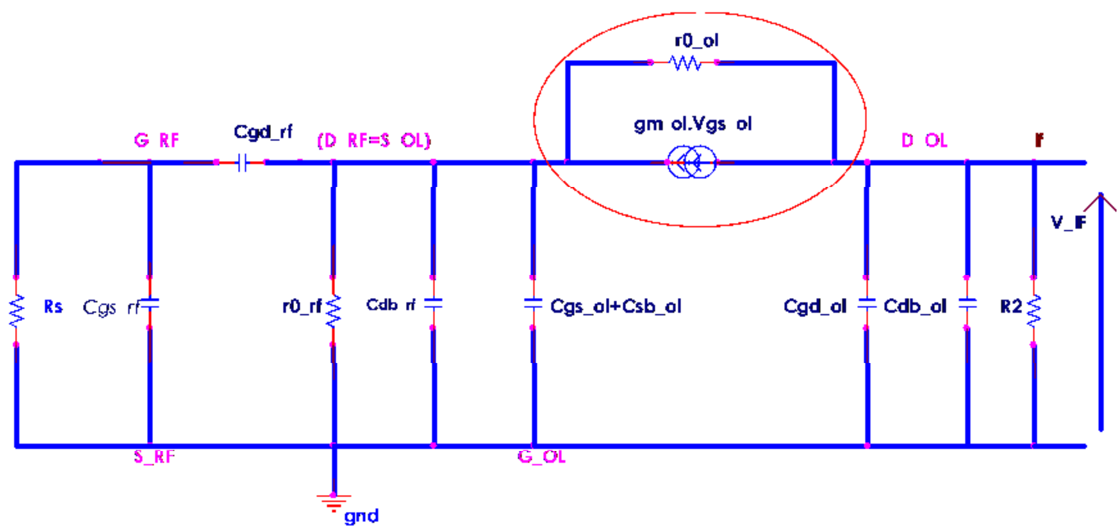

Fig 3: Equivalent Model of CMOS Dual-Gate Mixer.

Table 5: 60-GHz Mixer Performance Comparison

Reference	**[17]RFIC 2005**	**[18] ASSCC 2006**	**[19] EuMC 2009**	**This work**
Process	0.13um CMOS	90nm CMOS	0.13um CMOS	**45nm CMOS**
Topology	Single-gate	Dual- gate	Dual-gate	**Dual-gate**
RF(GHz)	60	60	60	**60**
IF(GHz)	2	4	5	**10**
Conversion Gain(dB)	2	1.2	-2.7	**-3.178**
NF(dB)	NA	N.A	18.9	**1.241**

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APPENDIX (B)

Calculation of effective transconductance (g_{meff}):

Consider the figure 9 below of the transistor charged by a resistor Rc with inductive source degeneration:

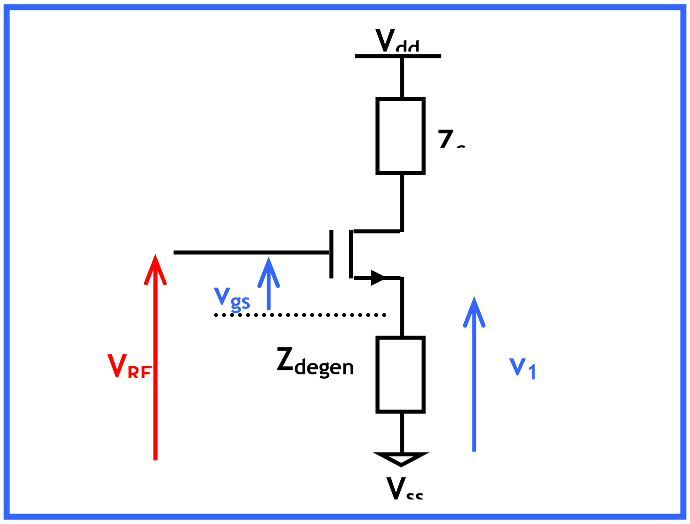

Fig 9: MOS transistor with inductive source degeneration

Equivalent model of this circuit in small signal is presented by the figure10 below:

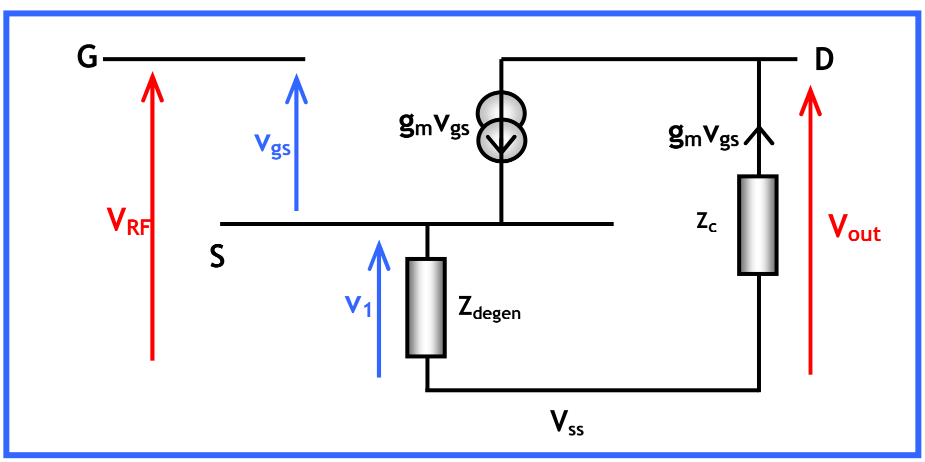

Fig.10: Equivalent model of MOS Transistor circuit in small signal with inductive source degeneration

We have: $v_{RF} = v_{gs} + v_1$ Then $v_{gs} = v_{RF} - v_1$

$v_{gs} = v_{RF} - Z_{degen} \cdot g_m v_{gs}$ Then $v_{RF} = (1 + Z_{degen} \cdot g_m).v_{gs}$

$v_{gs} = \frac{1}{(1 + Z_{degen} \cdot g_m)}.v_{RF}$ and we have already $v_{out} = -Z_C g_m v_{gs}$

$v_{gs} = -\frac{1}{(Z_C g_m)} v_{out}$ $\frac{1}{(Z_C g_m)} v_{out} = \frac{1}{(1 + g_m.Z_{deg\,en})}.v_{RF}$

Then i.e

So
$$A_v = \frac{v_{out}}{v_{RF}} = -\frac{Z_C g_m}{1 + g_m.Z_{degen}}$$

$$A_v = \frac{v_{out}}{v_{RF}} = -\frac{g_m}{1 + g_m.Z_{degen}} Z_C$$

Finally
$$g_m(Z_{degen}) = \frac{g_m}{1 + g_m.Z_{degen}} \quad (11)$$

We notice, by pushing the reasoning to the extreme, and increasing enough Z_{degen} ($Z_{degen} >> \frac{1}{g_m}$), the previous equation becomes:

$$g_{meff}(Z_{degen}) \approx \frac{1}{Z_{degen}}$$

Where $Z_{deg} = L_s$

Finally, L_s inductors for source degenerated to be choice in consideration with linearity parameter

(Decreasing our mixer gain see figure11 below):

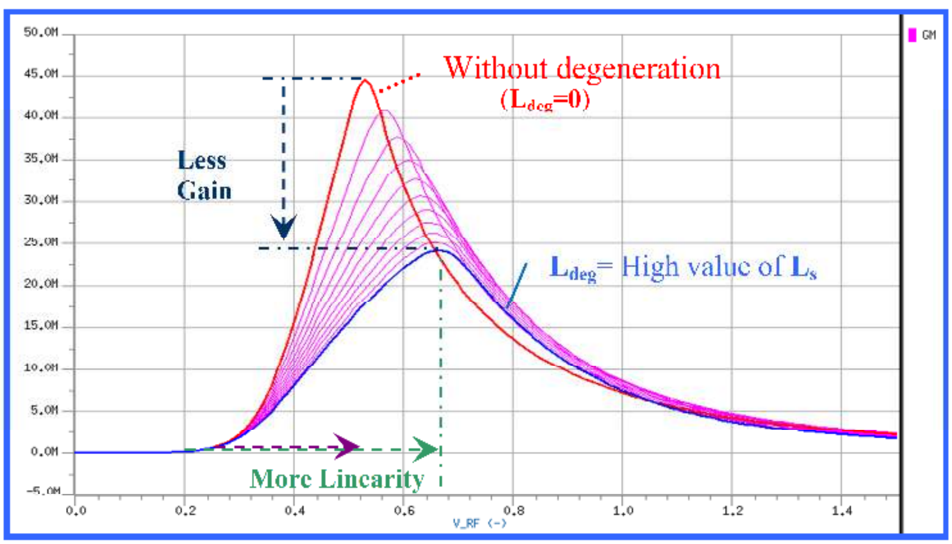

Fig 11: g_m versus input signal (V RF)

When L_{deg} increases, then we have more one gain in terms of linearity, however, this to the detriment of which g_m is attenuated, affecting subsequently the conversion gain, which is, as we have already demonstrated, Proportional to g_m.