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# COMPARISON BETWEEN INTERLEAVED BOOST CONVERTER BASED 6-SWITCH AND 4-SWITCH VSI FED PMBLDC MOTOR DRIVE

**V. RAMESH [1]*, Y. KUSUMA LATHA[2]**
[1]Research Scholar & Student Member IEEE, Department of Electrical & Electronics Engineering, KL University,
Guntur, A.P, India
[2]Professors, Department of Electrical and Electronics Engineering, K L University, Vaddeswaram, India
E-mail:sitamsramesh@gmail.com, kusumalathay@gmail.com,

**ABSTRACT**
In this paper, an improved interleaved boost converter topology for PMBLDC Motor has been proposed. The proposed interleaved boost converter topology has been used for 6-switch and 4-switch VSI fed PMBLDC motor drive and details are presented. The proposed research work has been implemented under Matlab/Simulink environment and tested for different operating conditions. The performance of 4-switch VSI fed PMBLDC motor drive compared with the performances of 6-switch VSI fed PMBLDC motor. From the results, it is observed that 4-switch VSI fed PMBLDC motor performance is superior to 6-switch VSI fed drive in certain aspects. In some other aspects performance of 6-switch VSI fed drive is superior to 4-switch VSI fed drive. Merits and demerits of each one of the schemes are investigated thoroughly under different operating conditions and corresponding results are presented.

***Keywords:*** *BLDC Motor, Interleaved Boost Converter, Torque Ripple, 4-switch VSI, 6-switchVSI*

**NOMENCLATURES**

BLDC- Brushless DC motor
CCM - Continuous Conduction Mode
DCM - Discontinuous Conduction Mode
FSTPI - Four Switch Three Phase Inverter
IBC - Interleaved Boost Converter
PFC - Power Factor Correction
PI - Proportional Integral
SSTPI - Six Switch Three Phase Inverter
ZCS - Zero Current Switching
ZVS - Zero Voltage Switching

## 1. INTRODUCTION

Brushless DC (BLDC) motors are widely used for various applications. BLDC motors are having certain advantageous compared to other contemporary drives due to more efficiency, higher flux density, less maintenance cost, lower interference (EMI), rugged and wide- range of speed control. A typical BLDC motor consists of three phase concentrated stator windings and permanent magnet rotor [1]-[2]. Hence, this motor is called electronically commutated motor due to electronic commutation based on hall Effect sensors to sense rotor position of the motor. It is different from conventional DC motor due to absence of mechanical brushes and commutated assembly. The conventional control scheme of BLDC motor draws currents from ac mains it may contain harmonics, in order to minimize the effect of harmonics on the performance of the BLDC Motor, there some control schemes proposed by some researchers. Normally, the power factor of the BLDC Motor is low. In order to achieve higher power factor, power factor correction converter are proposed for BLDC motor[3]-[4]. Generally hysteresis current control technique is employed to produce gate pluses for inverter switches of the BLDC Motor drive. In the hysteresis current control technique, actual motor currents controlled to follow rectangular reference currents[5].The BLDC Motor drive is becoming popular for variable speed applications, in that aspect, there are some speed control methods of BLDC motor proposed in [6]-[7],where PI controller is used as a speed controller, of course the PI controller can be implemented easily because of its simplicity. The necessity of speed control of a drive is to maintain the speed of the motor drive at its desired value and making the speed independent of the load of the motor and to make it less sensitive to external disturbances [8]-[9].

The main disadvantage of BLDC motor drive is high torque ripple. There are different methods which are available in the literature for torque ripple minimization of BLDC motor drives. But there is always a scope to carry out further research on torque ripple minimization of the BLDC motor.

In this paper, an interleaved boost converter topology has been proposed to minimize the torque

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ripple of BLDC motor by controlling the dc link voltage of 3-phase voltage source inverter of the BLDC motor. Further, in this paper a 4-switch VSI for BLDC motor has been proposed and comparison is also made between 4-switch VSI and 6-switch VSI fed BLDC Motor drive. Merits and demerits of each control scheme have been investigated thoroughly.

## 2. DESCRIPTION OF INTERLEAVED BOOST CONVERTER FOR VSI FED PMBLDC MOTOR

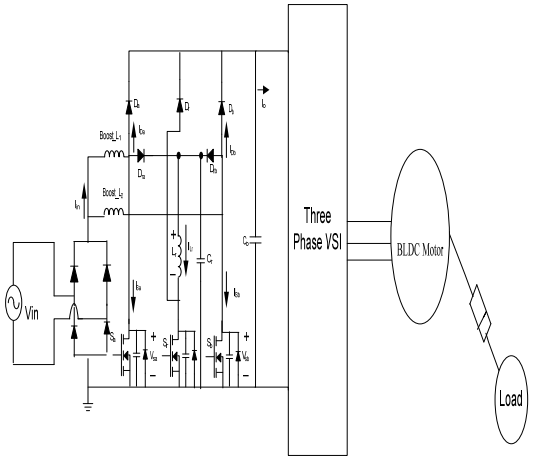


*Figure 1 Proposed interleaved boost converter for BLDC Motor drive*

Figure 1 shows the circuit diagram of the proposed Interleaved Boost Converter, it consists of inductor $L_r$, capacitor $C_r$, which is the resonance elements along with $C_{sa}$, $C_{sb}$ which represent the parasitic capacitances. Resonance occurs with the help of auxiliary switch. The components of interleaved boost converter are given in Table-1. The proposed interleaved boost converter gives high voltage gain; it is a combination of two 2- phase interleaved boost converters. For the figure 1, from KVL, voltage equation is given by equation (1)

$$V_0 = V_{sa} + V_{sb} - V_{in} \quad (1)$$

Where, $V_s$ = Supply voltage, $V_o$= Output voltage,
$V_{sa}$ = Voltage across Capacitor "$C_{sa}$",
$V_{sb}$ = Voltage across Capacitor "$C_{sb}$" ,
$V_{in}$ =Input voltage

Voltage gain (G) for the proposed interleaved boost converter is given by equation (2)

$$G = \frac{V_0}{V_s} = \frac{1 + D}{1 - D} \quad (2)$$

Where D = Duty cycle

In the proposed high voltage gain interleaved DC boost converter, there is a considerable reduction in input current ripple and inductor size. The output voltage ripple of the circuit depends on the size of capacitor. The proposed converter will be operated in Continuous Conduction Mode (CCM). Inductance and capacitance values can be selected from the equations (3) and (4).

$$L = \frac{DV_S}{4\Delta I_L f_S} \quad (3)$$

$$C = \frac{DI_{out}}{2\Delta V_{bus} f_S} \quad (4)$$

***Table -1***

| | | |
|---|---|---|
| Input Voltage | $V_{in}$ | 100V |
| Duty Cycle | $D$ | >50% |
| Out Put Voltage | $V_0$ | 265V |
| Output Current | $I_0$ | (0.5-1.5)A |
| Output Power | $P_0$ | (200-600)W |
| Switching Frequency | $f_s$ | 50KHz |
| Boost Inductor | $L_1$and $L_2$ | 2.4mH |
| Output Capacitor | $C_0$ | 470µF |
| Resonant Inductor | $L_r$ | 10mH |
| Resonant Capacitor | $C_r$ | 1.5nF |

***Parameters of the Interleaved Boost Converter***

Where, $\Delta I_L$= Maximum current ripple
$\Delta V_{bus}$ = Output voltage ripple
$I_{out}$ = Output current,
$f_s$ = Switching frequency for the proposed converter

The main advantage of the proposed interleaved boost converter topology is that it changes from a second order
system to first order system when the mode of operation changes from CCM to DCM. This feature is not present in the earlier interleaved boost converter topologies.

### 2.1. Modes of operation with D >50%

Figure 2 shows the related waveforms for the duty cycle greater than 50% for various modes of operation. The operation of the proposed interleaved boost converter is divided into seven modes. The

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following are the various assumptions made:
1. The diode switches are ideal,
2. Inductor, capacitors are assumed to be lossless. The inductors $L_1$, $L_2$ are identical. The duty cycle of main switches $S_a$ and $S_b$ are same.

**Mode-1 [$t_0$-$t_1$]**

Equivalent circuit of mode-1 operation is shown in figure 3(a) in mode-1, $S_a$, $S_b$, $S_c$ are switched ON and the rectifier diodes $D_a$ and $D_b$ and clamped diode $D_r$ are turned OFF. The main switch currents $I_{sa}$ and $I_{sb}$ are less than zero. The current through $S_a$, $S_b$, $S_c$ are zero or less than zero at the end of the previous mode ends. If equation (5) is satisfied, '$S_b$' exhibits ZCS characteristics at t=$t_1$ if the condition in (6) can be met. The interval time $t_{01}$current through resonant Inductor is give by

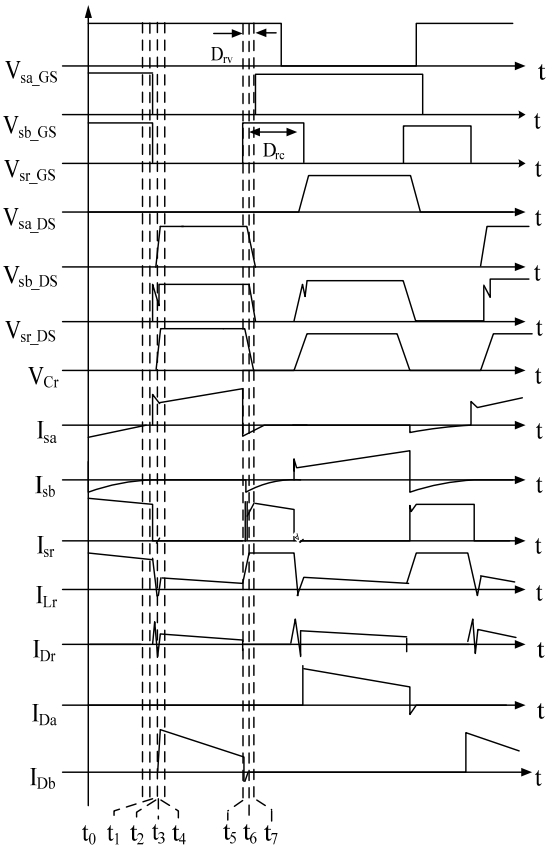


*Figure 2 Related waveforms (D > 50%)*

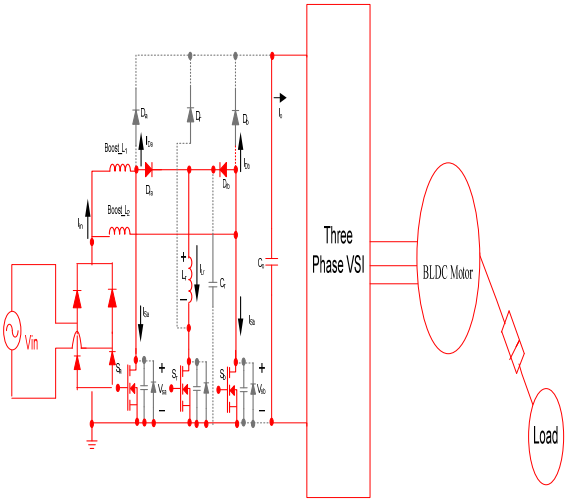


*Figure 3(a) Equivalent circuit for Mode-1[$t_0$-$t_1$]*

$$t_{01} = (D_1 - 0.5)T \quad (5)$$

$$i_{Lr}(t_1) = i_{L2}(t_a) + \frac{V_0}{\sqrt{\frac{L_r}{C_{sb} + C_r}}} \geq I_{in} \quad (6)$$

**Mode 2 [$t_1$ –$t_2$ ]**

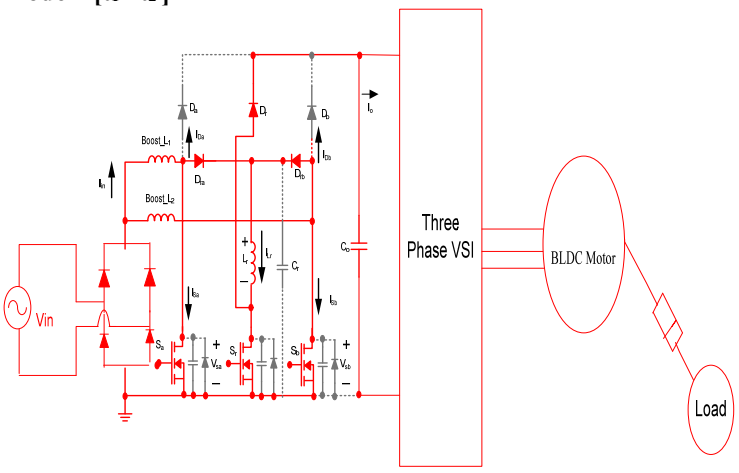


*Figure 3(b) Equivalent circuit for Mode-2[$t_1$-$t_2$]*

In this figure 3(b) in mode-2, the energy stored in resonant inductor $L_r$ ,is transferred to output load by clamped diode $D_r$ because the '$S_r$ ' (auxiliary switch) is switched OFF, the resonant inductor energy is transported to load with the help of clamped diode '$D_r$'. The current through $L_r$ gradually decreases to zero and the $D_r$ are switched off at time instant t = $t_2$.The interval time $t_{12}$of this mode given by

$$t_{12} = \frac{L_r}{V_0} I_{in} \quad (7)$$

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**Mode 3 [$t_2$ –$t_3$]**

In this figure 3(c) in mode-3 the energy transfer takes place between $L_2$ and $L_r$, $C_r$ and also between $C_{sr}$ and $C_{sb}$ .The '$D_r$' retains its pervious switching state and '$D_b$' is turned ON, when voltage across main switch (rectifier diode),'$V_{sb}$' and the voltage across resonant capacitor, '$V_{cr}$','C' is constant gradually increase to output voltage at time instant t=$t_3$.The resonant inductor current is

$$i_{Lr}(t)=-Vo\sqrt{\frac{CC_{sr}}{L_r(C+C_{sr})}}\,Sin\sqrt{\frac{C+C_{sr}}{L_r(C+C_{sr})}}t+\frac{I_{L2}C_{sr}}{C+C_{sr}}\times \quad (8)$$

$$(1-\cos\sqrt{\frac{C+C_{sr}}{LrCC_{sr}}}t)$$

Where $C=C_r+C_{sb}$

The resonant time $t_{23}$ is

$$t_{23}=\pi\sqrt{\frac{L_rCC_{sr}}{C+C_{sr}}} \quad (9)$$

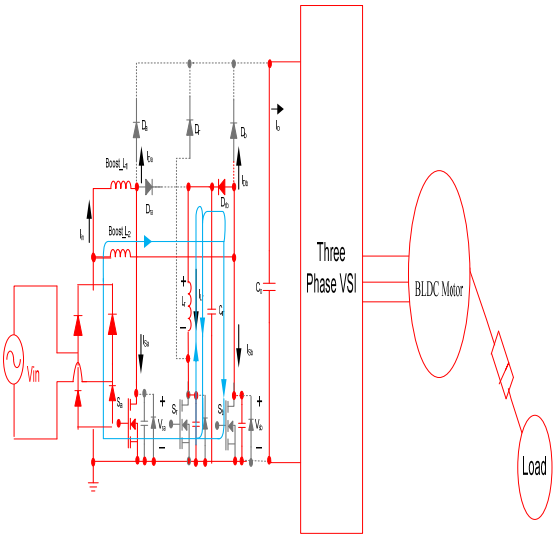


*Figure 3(c) Equivalent circuit for Mode-3[$t_2$-$t_3$]*

**Mode 4 [$t_3$ –$t_4$]**

In this figure 3(d) in mode-4 after $t_3$, parasitic capacitor $C_{sr}$ of the auxiliary switch is linearly changed by $I_{L2}$-$I_0$ to $V_o$ At $t_4$, clamped diode is turned ON. The interval time $t_{34}$ in this mode is given by

$$t_{34}\approx\frac{C_{sr}.V_o}{I_{L2}-I_0} \quad (10)$$

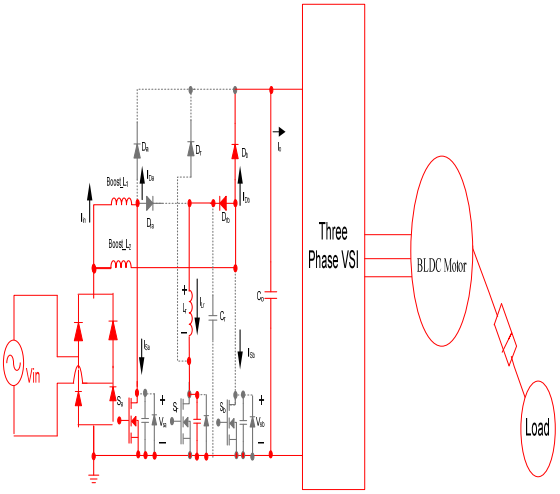


*Figure 3(d) Equivalent circuit for Mode-4[$t_3$-$t_4$]*

**Mode 5 [$t_4$ –$t_5$]**

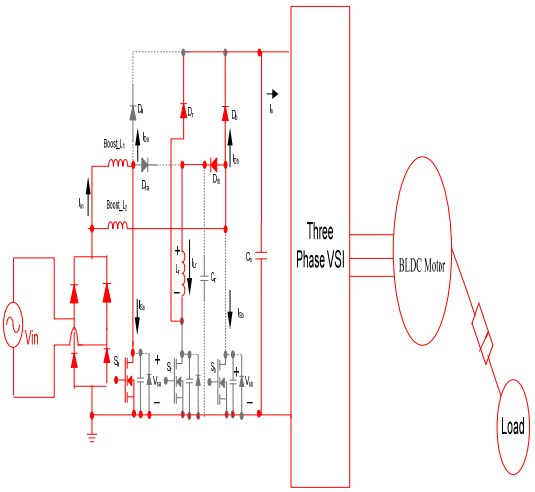


Figure 3(e) Equivalent circuit for Mode-5[$t_4$-$t_5$]

In this figure 3(e) in mode-5 the stored inductor energy is transported to the load through $D_r$.At time instant $t_5$, $D_r$ is turned is switched OFF, $S_r$ is switched ON. From figure5 (b), simplified waveform, the interval time $t_{45}$ and resonant inductor current are

$$t_{45}=0.5T-t_{04}-D_{rv}T \quad (11)$$

$$i_{Lr}(t_5)=i_{Lr}(t_4) \quad (12)$$

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## Mode 6 [$t_5 - t_6$]

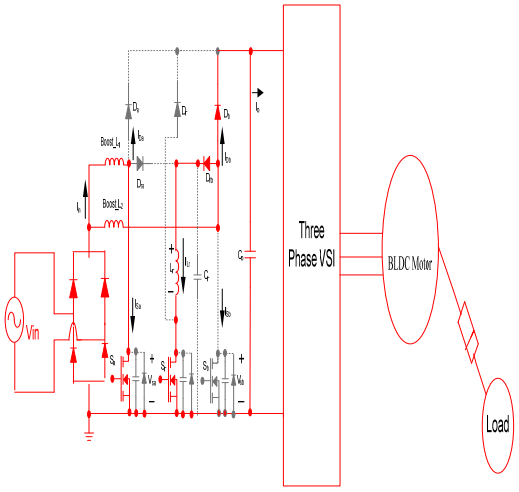


*Figure 3(f-a) Equivalent circuit for Mode- 6 [$t_5 - t_a$]*

In this figure 3(f-b) in mode-6(f-a) the current through $L_r$ increase linearly till. it is equal to the current through $L_2$. The current through rectifier diode $D_b$ diminishes to zero at t=$t_a$, and $D_b$ is switched OFF. The interval time $t_{5a}$ is given by

$$t_{5a} = \frac{I_0}{V_0} L_r \qquad (13)$$

figure mode-6(f-b)In the interval $t_a$-$t_5$, the $I_{Lr}$ gradually increase to peak value and $V_{sb}$ reduces to zero due parasitic capacitances. The $D_{sb}$ of $S_b$ are switched ON at time instant $t_6$. The interval time $t_{6a}$ is

$$t_{6a} = \frac{\pi}{2w_1} = \frac{\pi}{2}\sqrt{L_r(C_{sb} + C_r)} \qquad (14)$$

And the interval time $t_{56}$ is

$$t_{56} = t_{5a} + t_{6a} = \frac{I_0}{V_0} L_r + \frac{\pi}{2}\sqrt{L_r(C_{sb} + C_r)} \qquad (15)$$

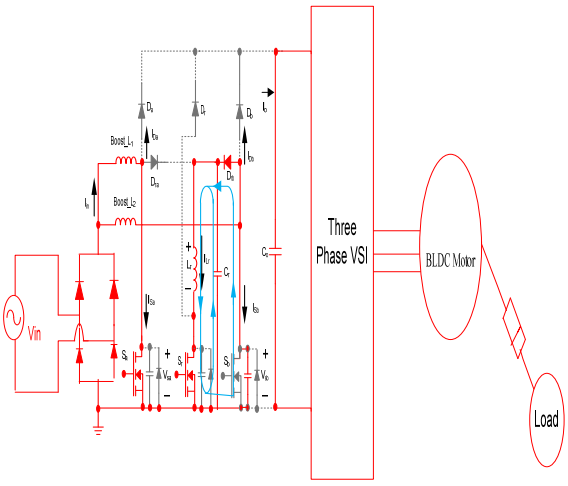


*Figure 3(f-b) Equivalent circuit for Mode- 6 [$t_a - t_6$]*

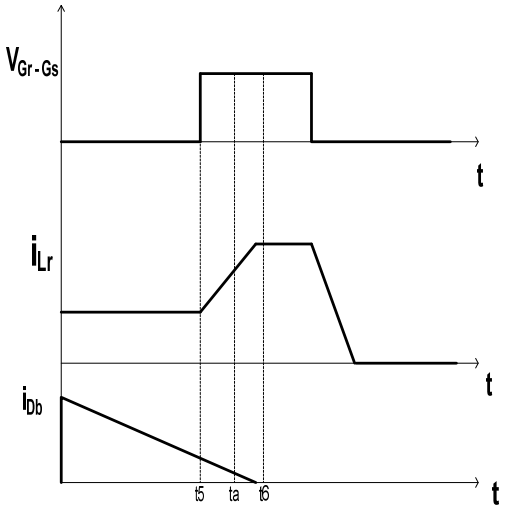


*Figure 3(f-c) Detailed waveform of the Mode- 6*

## Mode7 [$t_6 - t_7$]

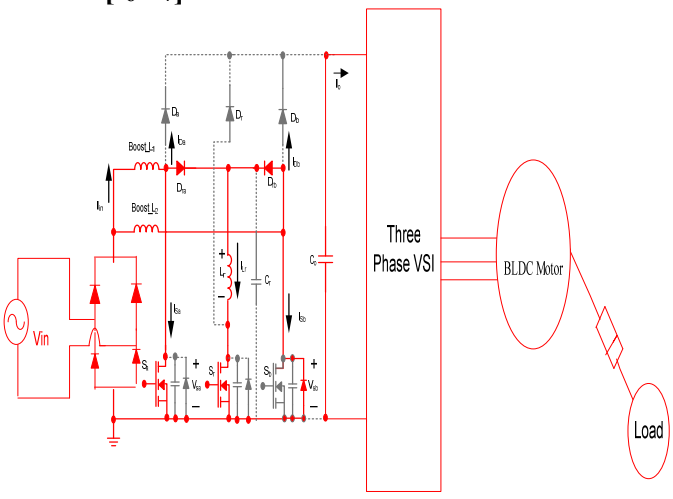

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*Figure 3(g) Equivalent circuit for Mode-7 [$t_6$ –$t_7$]*

In this figure 3(g) in mode-7 when $V_{sb}$=0 and $V_{cr}$ =0, $D_{sb}$ is switched ON. In this mode resonant inductor is realised using constant current source. We have $I_a$ , $I_{sb} \leq 0$ if $I_{Lr}$ at time $t_6$=$I_{Lr}$ time $t \geq I_{in}$ . Under ZCS condition, $S_a$ can be switched OFF. Due to Condition of $D_{sb}$, $S_b$ reaches ZVS condition.
The interval time during the mode is

$$t_{67} = 0.5T - t_{06} \quad (16)$$

During zero-current switching conditions are

$$(1)\ i_{Lr}(t) = i_{L2}(t_a) + \frac{V_0}{\sqrt{\frac{L_r}{(C_{sb} + C_r}}} \geq i_{in}(t) \quad (17)$$

2) $D_{rc}$, $T > t_{56}$

### 2.2 Voltage Ratio Of D > 50% Mode

The related waveforms with $D$ >50% are shown in the simplified form in figure 4. The duty cycles of the main switches are equal $D_1T$ and $D_2T$.The current through boost inductor when switched ON is given by

$$\sum_{sa=on} \Delta i_{L1} = \frac{V_{in} \times (D_1 + D_{rv})}{L_1} T \quad (18)$$

Similarly, the current when switched OFF

$$\sum_{sa=off} \Delta i_{L1} = \frac{(V_{in} - V_0) \times [1 - (D_1 + D_{rc} + 2D_{rv})]}{L_1} T \quad (19)$$

Conversion ratio is given by

$$\frac{V_0}{V_{in}} = \frac{1}{1 - (D_1 + D_{rv})} \quad (20)$$

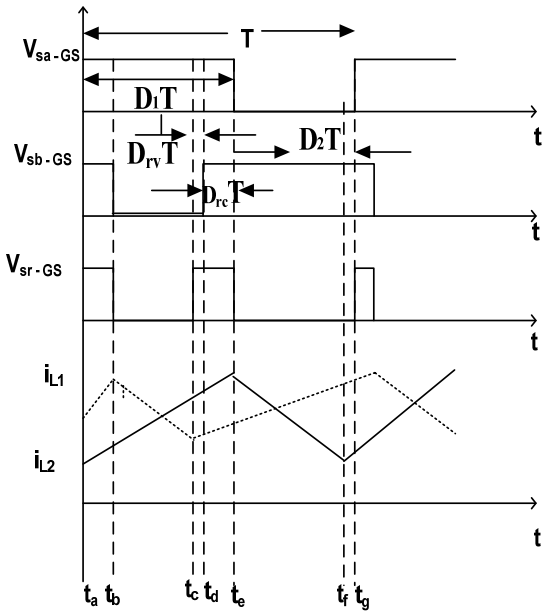


*Figure 4 Simplified waveform D>50%*

### 2.3. Calculation Of The Boost Inductors And Output Capacitor

The output capacitor is a high voltage bulk capacitor (490μF, 290V). Their considerations can refer to the minimum boost inductor when D>50%.

$$L_{min}/L = L_1 or L_2 = \frac{(D_1 + D_{rv})[1 + (D_1 + D_{rv})]^2 R}{f_s} \quad (21)$$

=2.4Mh

### 2.4. CONTROL STRATEGY FOR INTERLEAVED BOOST CONVERTER

The main aim of control scheme of interleaved boost converter is to produce gate pulses for the converter switches. The gate pulses are generated by comparing the actual dc link voltage of the converter with its reference value. Reference voltage $V_{dc}^*$ is obtained by multiplying the reference speed(w*) with the motor's voltage constant ($K_v$) as follows

$$V_{dc}^* = K_v W^* \quad (22)$$

And error voltage ($V_e$) is obtained is:

$$V_e(K) = V_{dc}(K)^* - V_{dc}(K) \quad (23)$$

Where "$K$" is the $K_{th}$ sampling instance. Then the error voltage $V_e$ is fed to a voltage proportional

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integral (PI) controller to generate controlled output voltage ($V_{cc}$).

which can be expressed as follows

$$V_{cc}(K)=V_{cc}(K-1)+K_P\{V_e(K)-V_e(K-1)\}+K_iV_e(K) \quad (24)$$

Where $K_P$ and $K_i$ are proportional and integral gains of the PI controller. Finally, PWM gate signals are generated by comparing the output of the PI controller ($V_{cc}$) with the high frequency sawtooth signal ($A_d$) for the interleaved boost converter switches $S_a$ and $S_r$ and $S_b$.

For

$$V_{in} > 0; \begin{cases} \text{if } A_d < V_{cc} \text{ then } S_a = \text{'ON'} \\ \text{if } A_d \geq V_{cc} \text{ then } S_a = \text{'OFF'} \\ \text{if } A_d < V_{cc} \text{ then } S_a = \text{'ON'} \end{cases} \quad (25)$$

$$V_{in} < 0; \begin{cases} \text{if } A_d < V_{cc} \text{ then } S_b = \text{'ON'} \\ \text{if } A_d \geq V_{cc} \text{ then } S_b = \text{'OFF'} \\ \text{if } A_d < V_{cc} \text{ then } S_b = \text{'ON'} \end{cases} \quad (26)$$

The interleaved boost converter is operating in CCM; therefore, the input current shaping is in phase with the supply voltage that means inherently unity power factor is achieved with ac mains.

## 3. COMPARISON BETWEEN 4-SWITCH AND 6-SWITCH VSI FED BLDC MOTOR

### 3.1 6-switch VSI fed BLDC motor drive

Figure 5 shows the block diagram of Interleaved Boost Converter based VSI fed BLDC motor with 6 switch VSI configuration. There are two control loops, one is the speed control loop which is outer loop and another one is inner current loop. The speed error is obtained by comparing the actual speed with the desired reference speed. The speed error is fed to the PI voltage controller to obtain the reference dc link voltage and compared with actual value to produce the current. Gate pulses are obtained for 6-switch VSI through hysteresis current control technique. As we know that torque ripple of BLDC motor drive is mainly depends on speed and phase current during commutation. The commonly used commutation in 3 phase BLDC motor is the six-step, in which each phase voltage is energized for interval of $120^0$ electrical according to the rotor electrical position. In this paper, a new circuit topology to achieve dc link voltage control has been proposed to keep phase current changing at the same rate during commutation. The desired commutation voltage accomplished by the interleaved boost converter. The specifications of PMBLDC Motor are given in Table-2.

***Table -2***
***Parameters of BLDC Motor***

| | | |
|---|---|---|
| Stator resistances/Phase | $R_s$ | 2.850Ω |
| Stator inductance/Phase | $L_s$ | 8.5mH |
| Voltage Constant | $K_v$ | 146.6077 (V_peak L-L / krpm) |
| Torque Constant | $K_t$ | 1.4(N.m / A_peak) |
| Back EMF | $E_b$ | 120Volt |
| Pole pairs | P | 4 |
| Friction factor | B | 1N.ms |
| Inertia | $J_n$ | 1.2kg.m$^2$ |

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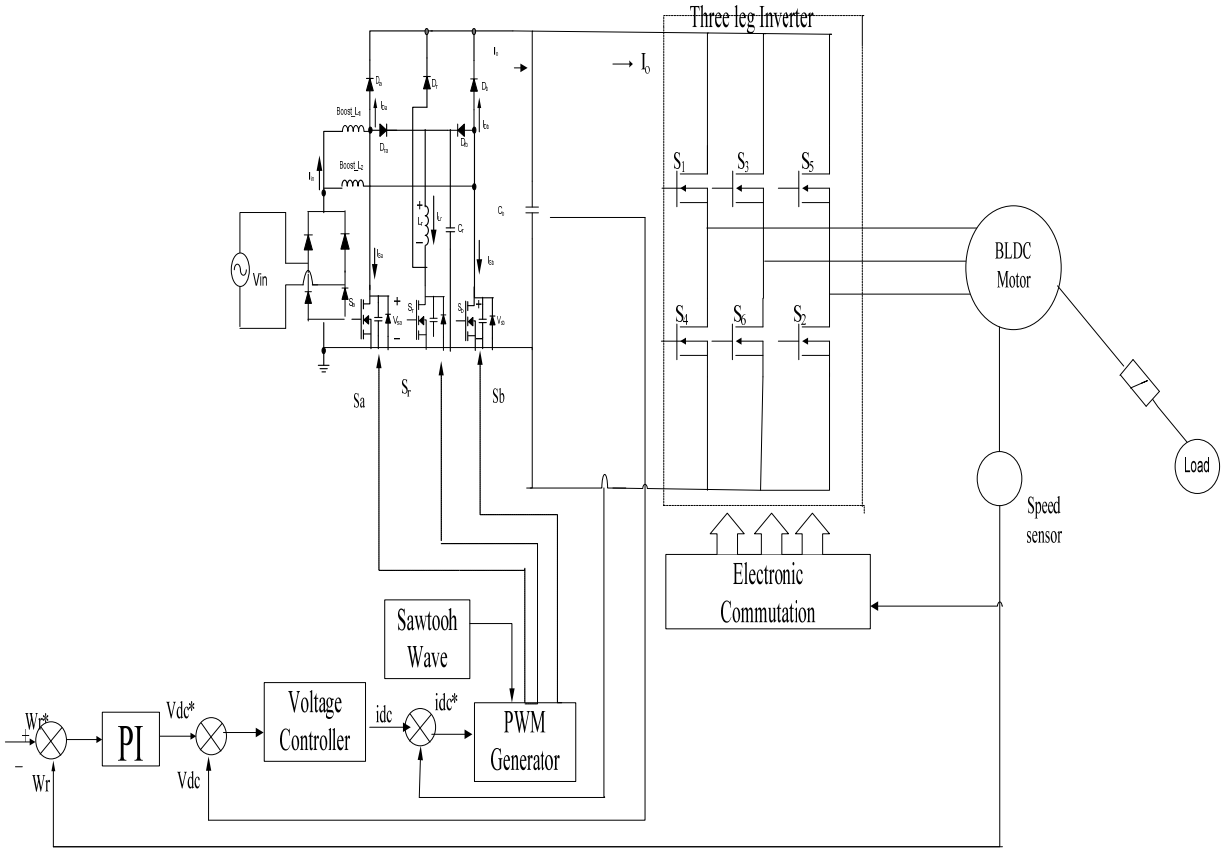


*Figure 5 Interleaved Boost Converter with six switch three phase VSI fed PMBLDC Motor*

The three phase voltage equations of BLDC Motor are as follows

$$V_{as} = \mathrm{R}i_a + L\frac{di_a}{dt} + e_a + V_{no} \quad (27)$$

$$V_{bs} = \mathrm{R}i_b + L\frac{di_b}{dt} + e_b + V_{no} \quad (28)$$

$$V_{rs} = \mathrm{R}i_c + L\frac{di_c}{dt} + e_c + V_{no} \quad (29)$$

Due to the interaction of the current in stator winding and the magnetic field from rotor magnets, the electromagnetic torque of BLDC motor produced as follows:

$$T_e = \frac{e_a i_a + e_b i_b + e_c i_c}{W_m} \quad (30)$$

Where Wm is the mechanical speed of the rotor .The equation of motion is given by

$$\frac{dW_m}{dt} = \frac{T_e - T_l - BW_m}{J} \quad (31)$$

Where $T_l$ = Load torque ,
B = Damping constant ,
J=Moment of inertia of motor and load
For six- step motor control, at each step the instantaneous output power will be will delivered from two phase in series, and is given by

$$P_0 = \omega_m T_e = 2V_{\max} I_m \quad (32)$$

Where 'I' is the current amplitude and E is the induced Back EMF .From (30) and (32),the output torque can be also be expressed as

$$T_e = 2K_t T_m \quad (33)$$

Where,Kt is the motor torque constant.The three phase voltage equations can be rewritten as

$$0 = \mathrm{R}i_a + L\frac{di_a}{dt} + e_a + V_{no} \quad (34)$$

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$$V_{dc} = \mathrm{Ri}_b + L\frac{di_b}{dt} + e_b + V_{no} \quad (35)$$

$$0 = \mathrm{Ri}_c + L\frac{di_c}{dt} + e_c + V_{no} \quad (36)$$

$$V_{no} = \frac{1}{3}(V_{dc} - \mathrm{V}_{\max}) \quad (37)$$

$$T_e = \frac{e_a i_a + e_b i_b + e_c i_c}{W_m} = \frac{2I_m V_{\max}}{W_m} \quad (38)$$

$$\frac{di_a}{dt} = \frac{V_{dc} + 2V_{\max}}{3L_s} \quad (39)$$

$$\frac{di_b}{dt} = \frac{2(V_{dc} + 2V_{\max})}{3L_s} \quad (40)$$

$$\frac{di_c}{dt} = \frac{V_{dc} - 4V_{\max}}{3L_s} \quad (41)$$

The time taken for $i_a$ to from the initial value $I_m$ is

$$t_1 = \frac{3L_s I_m}{V_{dc} + 2V_{\max}} \quad (42)$$

The time taken for $i_b$ to increase from 0 to $I_m$ is

$$t_1 = \frac{3L_s I_m}{2(V_{dc} - V_{\max})} \quad (43)$$

Accordingto(34)(42),and$i_a+i_b+i_c=0$,during commutation, the electromagnetic torque can be calculated as

$$T_e = \frac{2V_{\max}}{W_m}(I_m + (\frac{V_{\max} - 4V_{\max}}{3L_s}) \quad (44)$$

The relative torque ripple is given by

$$\Delta T_e = T_e - T_{e-pre}(\frac{V_{\max} - 4V_{\max}}{3L_s})t \quad (45)$$

According to (33) and (41)-(44),the following conclusion can be drawn

1.If $V_{dc}>4V_{max}$, then $t_1>t_2$, and the torque keeps increasing during commutation .

2. If $V_{dc}>4V_{max}$, then $t_1<t_2$, and the torque keeps decreasing during commutation.

3.If $V_{dc}>4V_{max}$, then $t_1<t_2$, and the torque is constant during commutation .

### *3.4. 4-switch VSI fed BLDC motor*

Figure 6 show the interleaved boost converter based 4-switch VSI fed PMBLDC motor drive. Here, the 6- switch voltage source inverter is replaced by 4-switch voltage source inverter to reduce number of switches which reduces switching losses as numbers of switches are less. The remaining part of the diagram shown in figure 5 is same. By reducing the number of switches from 6 to 4 in VSI, the requirement of the dc link voltage gets reduced.

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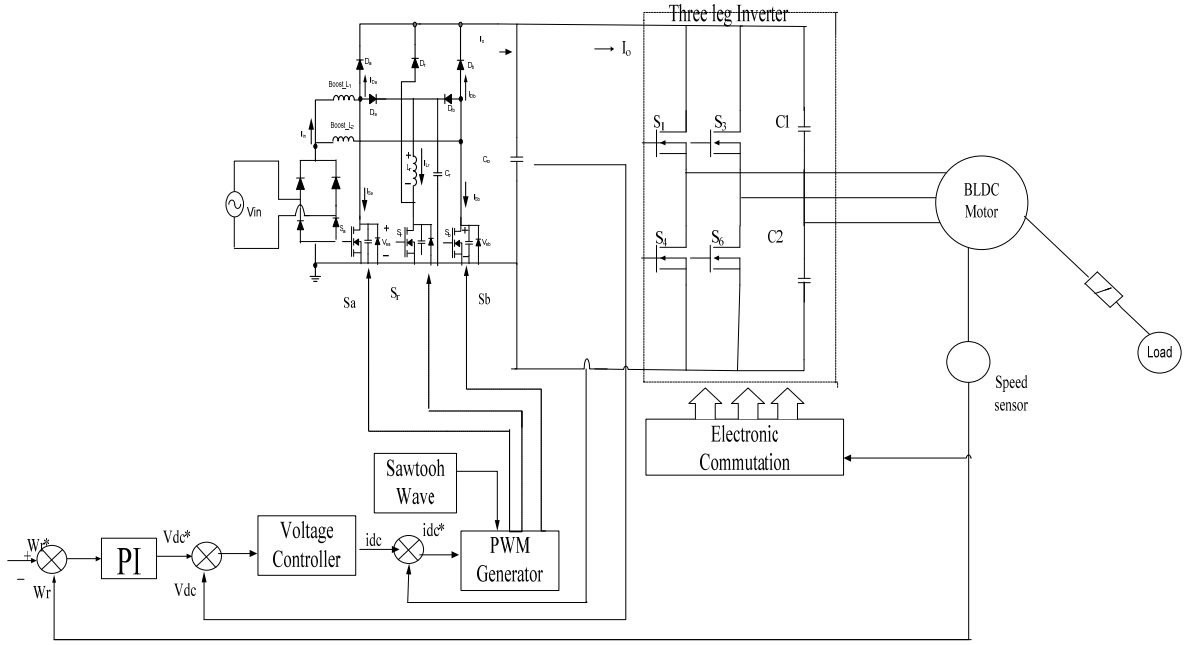


*Figure 6 Interleaved Boost Converter based 4- switch three phase VSI fed PMBLDC Motor*

## 4. RESULTS AND DISCUSSION

The proposed work has been implemented under Matlab/Simulink environment and corresponding results are presented for both 6-switch VSI fed BLDC motor and 4-switch VSI fed BLDC motor. Results are taken for different load torques and speed conditions and relevant waveforms are presented from figure 7 to figure 10. figure 7 shows the performance Analysis of 6-Switch and 4-switch VSI fed PMBLDC Motor for $T_L$=2N-m and 1000rpm, figure 8 shows the performance Analysis of 6-Switch and 4- switch VSI fed PMBLDC Motor for $T_L$=5N-m and 1000rpm.figure 9 shows the performance Analysis of 6-Switch and 4-switch VSI fed PMBLDC Motor for $T_L$=2N-m and change of speed from 500 rpm to 1000rpm and figure 10 shows the performance Analysis of 6-Switch and 4-switch VSI fed PMBLDC Motor for $T_L$=5N-m and change of speed from 500 rpm to 1000rpm respectively. Fromm all the waveforms, it is noticed that the dynamic performance of 6-switch VSI fed BLDC Motor is superior to 4-switch VSI fed BLDC motor because of more power with large dc link voltage support from 6-switch VSI. As per as the torque ripple is concerned, 4-switch VSI fed BLDC Motor is superior to 6-switch VSI fed BLDC motor because of less requirement of dc link voltage which is responsible in control of torque ripple of BLDC motor. The same is noticed in all the figures from 7 to 10 under all operating conditions.

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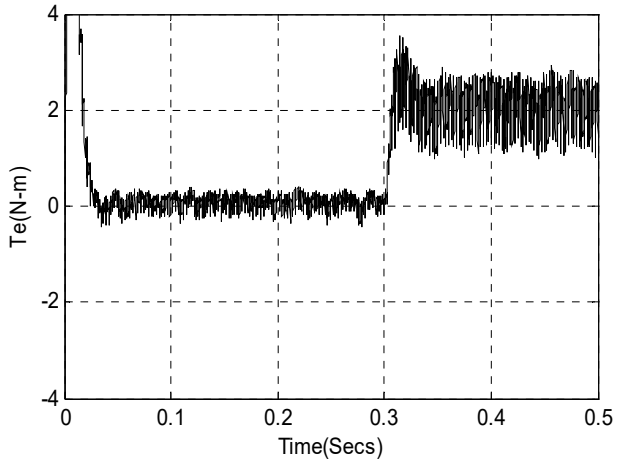
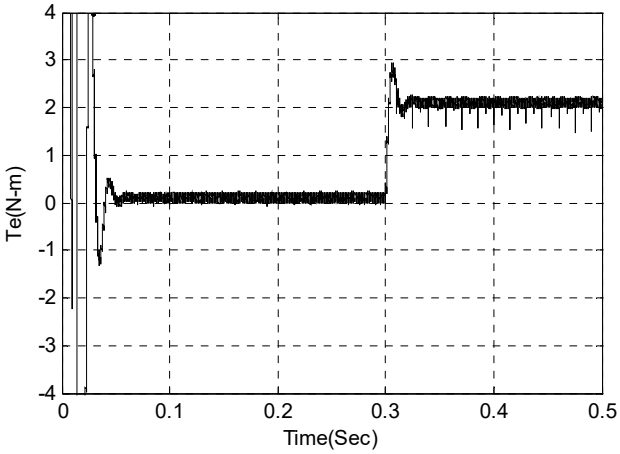



*Figure7(a) Motor torque response of 6-switch VSI fed drive with load torque, $T_L$=2Nm*




*Figur7(b)Motor torque response of 4- switch VSI fed drive with load torque, $T_L$=2N-m*

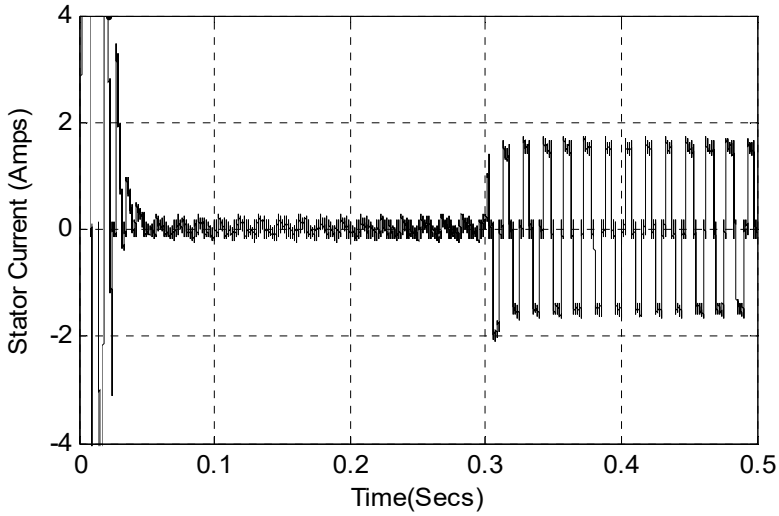



*Figure7(c)Stator current response of 6-switch VSI fed drive with load torque, $T_L$=2N-m*

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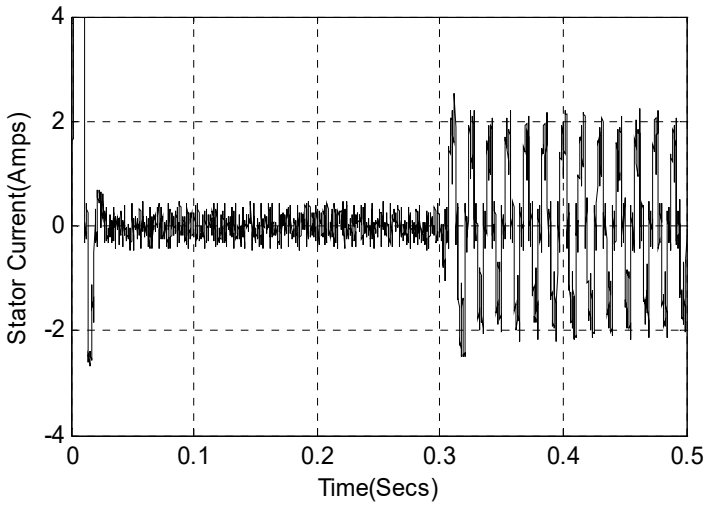


*Figure7(d) Stator current response of 4- switch VSI fed drive with load torque, $T_L$=2N-m*

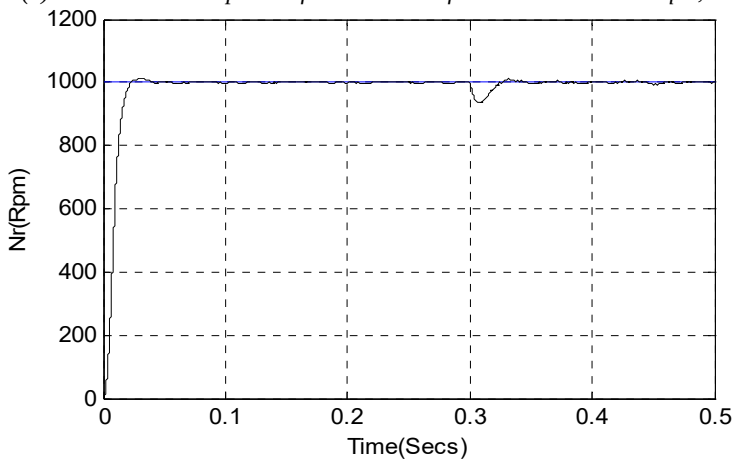


*Figure 7(e) Speed response of 6-switch VSI fed drive with load torque, $T_L$=2N-m*

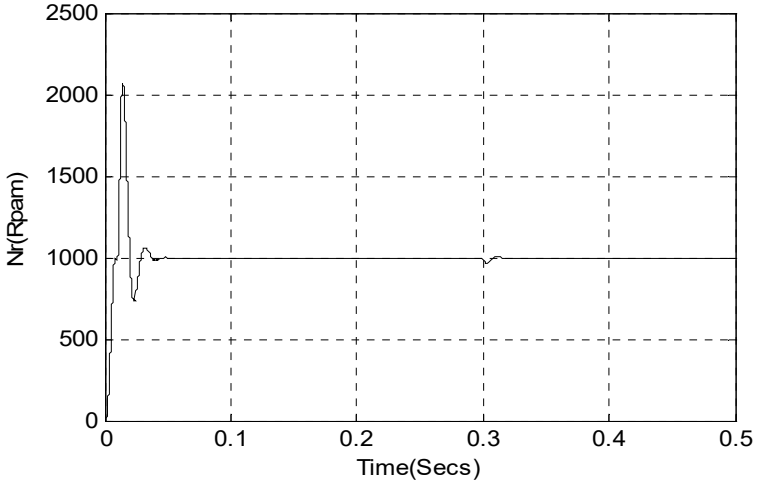


*Figure 7(f) Speed response of 4- switch VSI fed drive with load torque, $T_L$=2N-m*

*Figure 7 Performance Analysis of 6-Switch and 4-switch VSI fed PMBLDC Motor for $T_L$=2N-m and 1000rpm*

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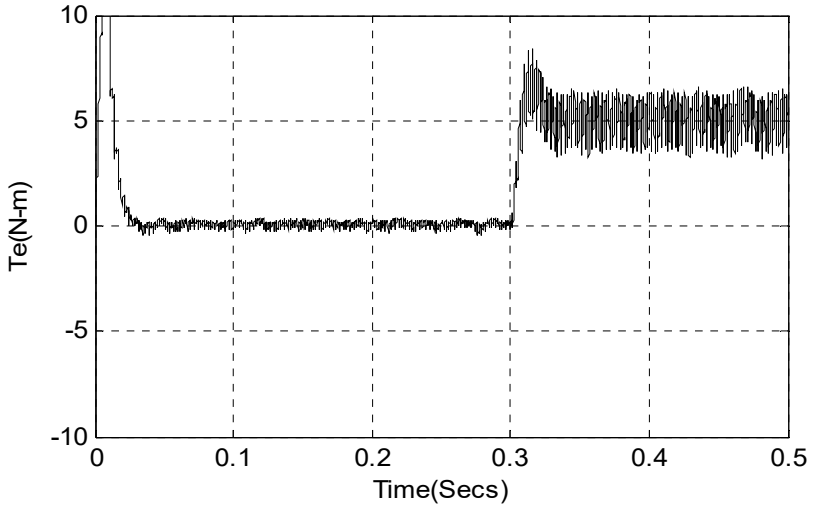


*Figure8(a) Motor torque response of 6-switch VSI fed drive with load torque, $T_L$=5N-m*

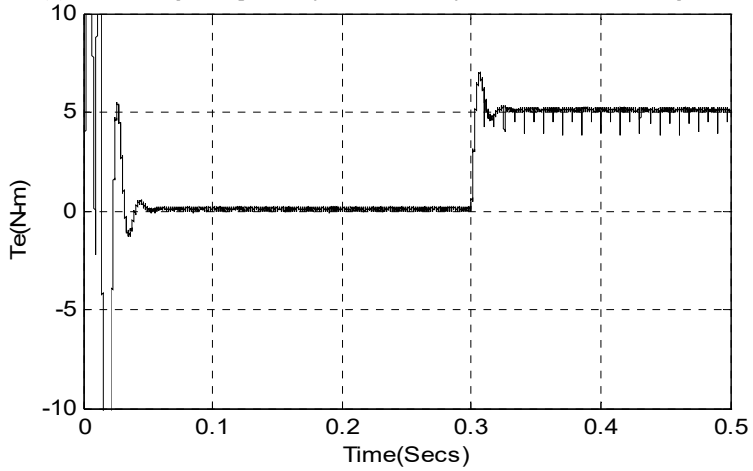


*Figure 8(b) Motor torque response of 4- switch VSI fed drive with load torque, $T_L$=5N-m*

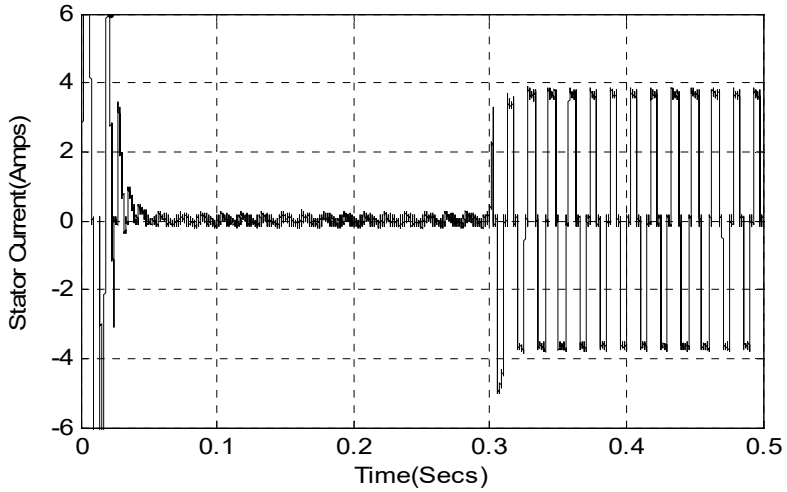


*Figure8(c) Stator current response of 6-switch VSI fed drive with load torque, $T_L$=5N-m*

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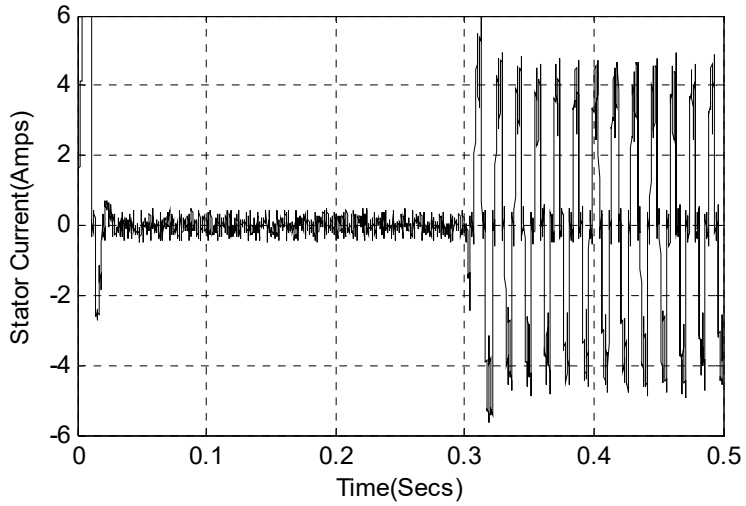


*Figure8(d) Stator current response of 4- switch VSI fed drive with load torque, $T_L$=5N-m*

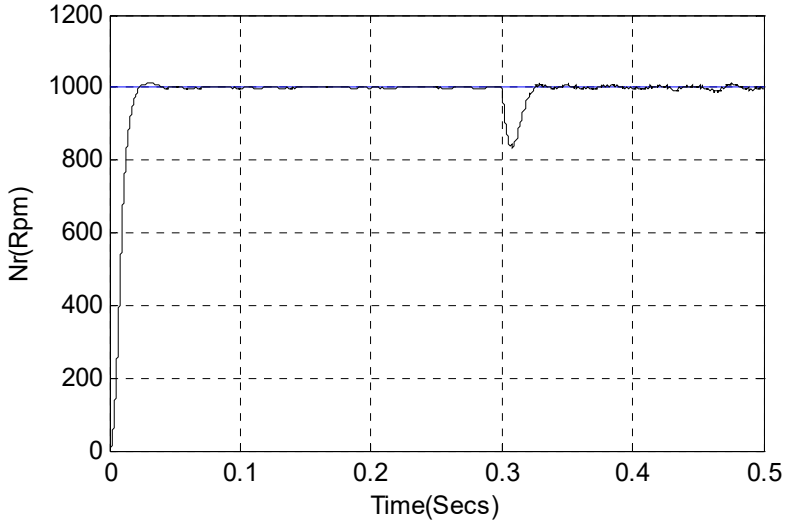


*Figure 8 (e) Speed response of 6-switch VSI fed drive with load torque, $T_L$=5N-m*

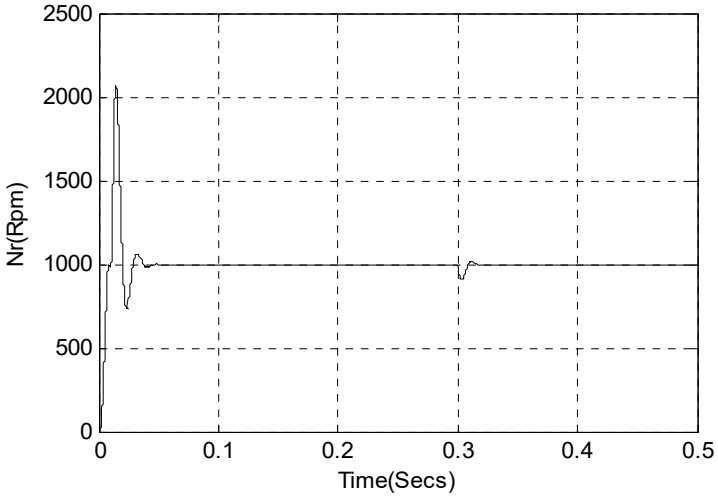


*Figure 8(f) Speed response of 4- switch VSI fed drive with load torque, $T_L$=5N-m*

*Figure 8 Performance Analysis of 6-Switch and 4- switch VSI fed PMBLDC Motor for $T_L$=5N-m and 1000rpm*

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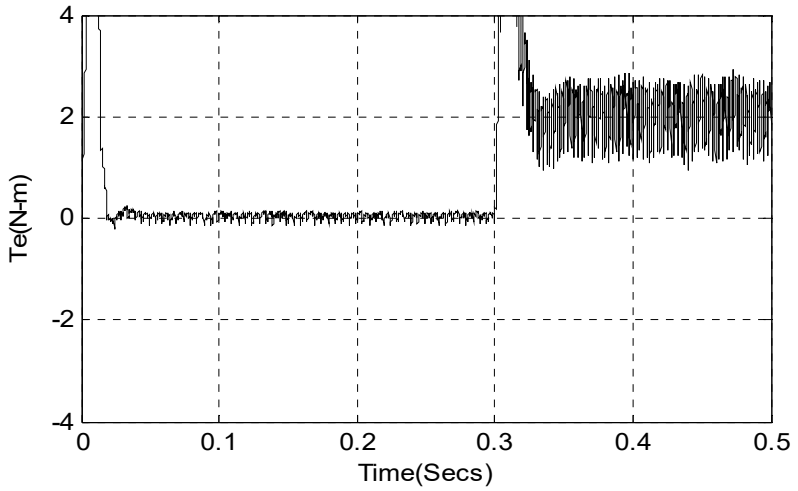


Figure 9(a) Motor torque response of 6-switch VSI fed drive with $T_L$= 2N-m and change of speed

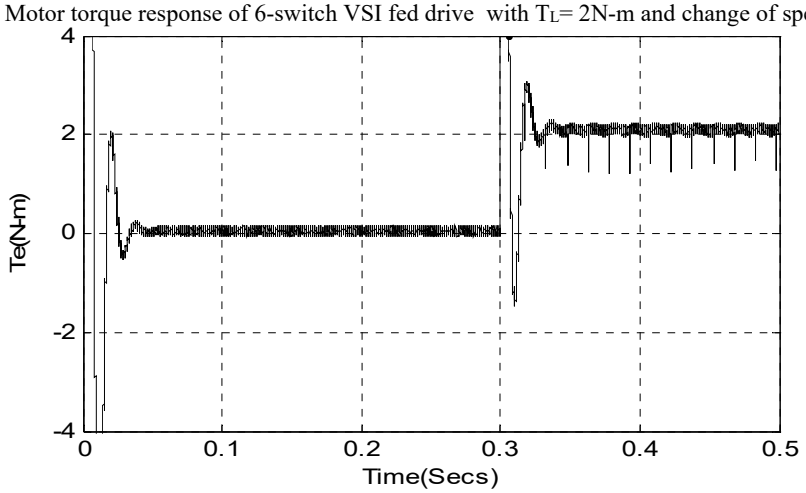


Figure9 (b) Motor torque response of 4- switch VSI fed drive with $T_L$= 2N-m and change of speed

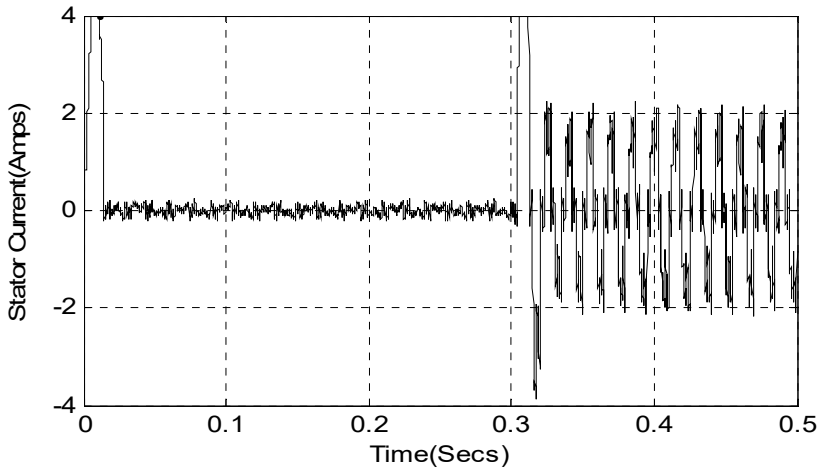


*Figure9(c) Stator current response of 6-switch VSI fed drive with $T_L$=2N-m and change of speed*

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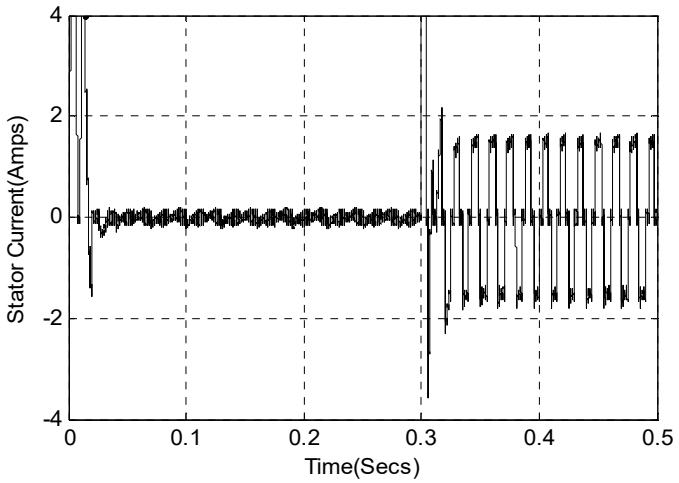


*Figure 9(d) Stator current response of4- switch VSI fed drive with $T_L$=2N-m and change of speed*

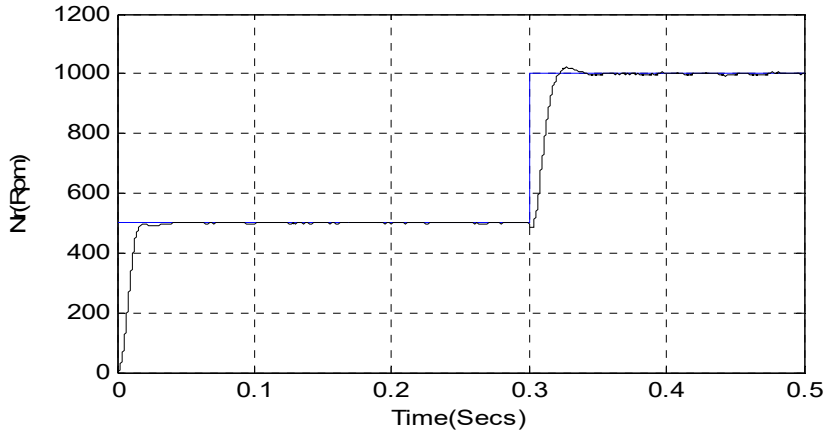


*Figure 9(e) Speed response of 6-switch VSI fed drive with $T_L$=2N-m and change of speed*

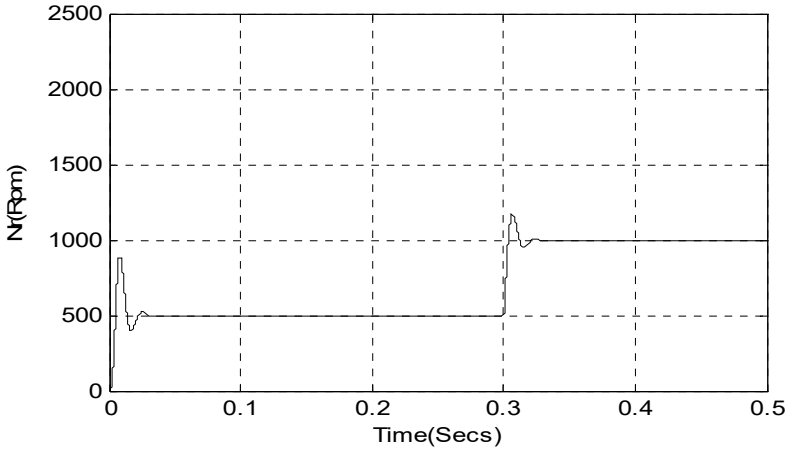


*Figure 9(f) Speed response of 4- switch VSI fed drive with $T_L$= 2N-m and change of speed*

*Figure 9 Performance Analysis of 6-Switch and 4-switch VSI fed PMBLDC Motor for $T_L$=2N-m and change of speed from 500 rpm to 1000rpm*

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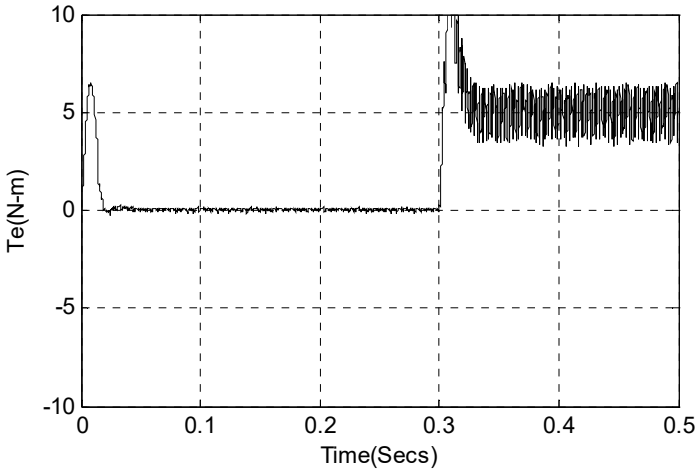


*Figure 10(a) Motor torque response of 6-switch VSI fed drive with $T_L$=5N-m and change of speed*

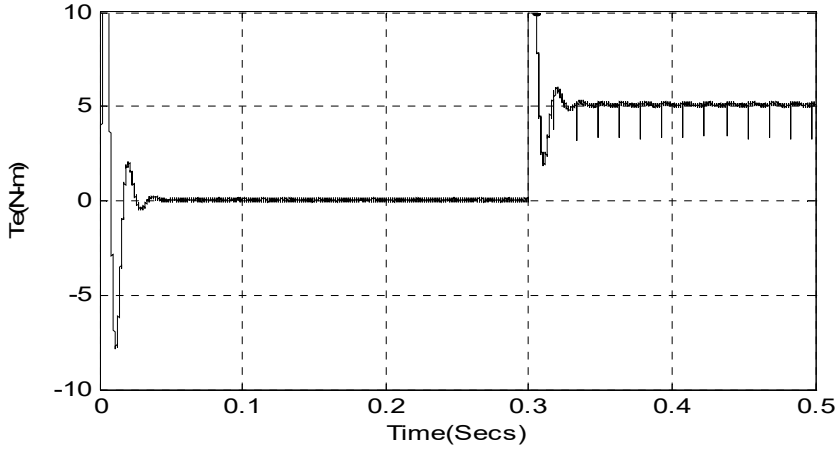


*Figure 10(b) Motor torque response of 4- switch VSI fed drive with $T_L$=5N-m and change of speed*

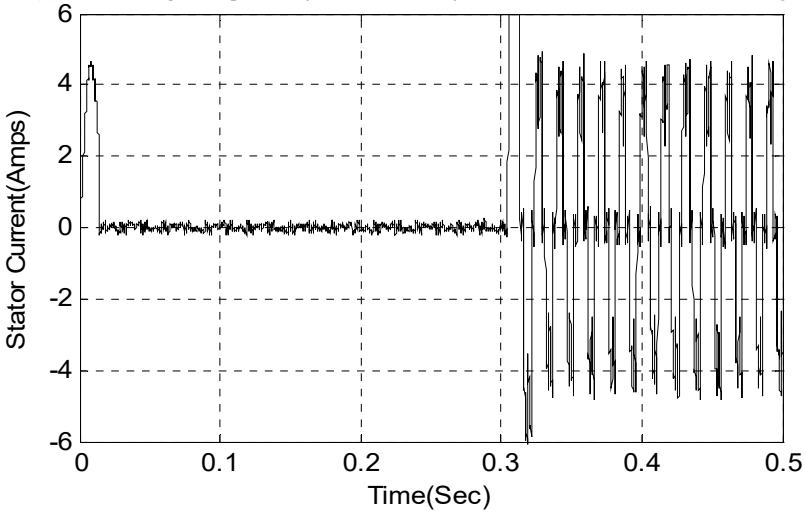


*Figure 10(c) Stator current response of 6-switch VSI fed drive with $T_L$=5N-m and change of speed*

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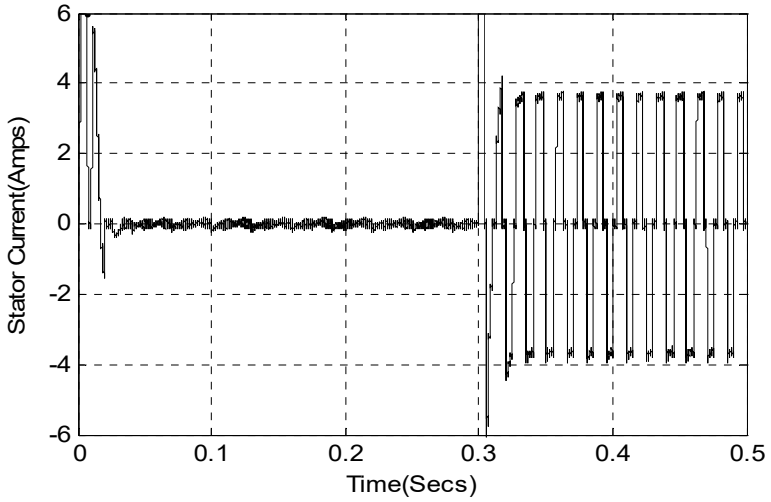


*Figure 10(d) Stator current response of 4-switch VSI fed drive with $T_L$=5N-m and change of speed*

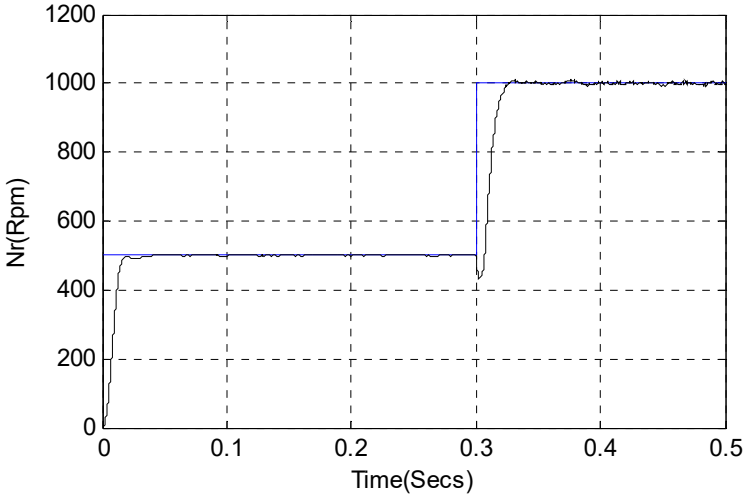


*Figure10(e) Speed response of 6-switch VSI fed drive with $T_L$=5N-m and change of speed*

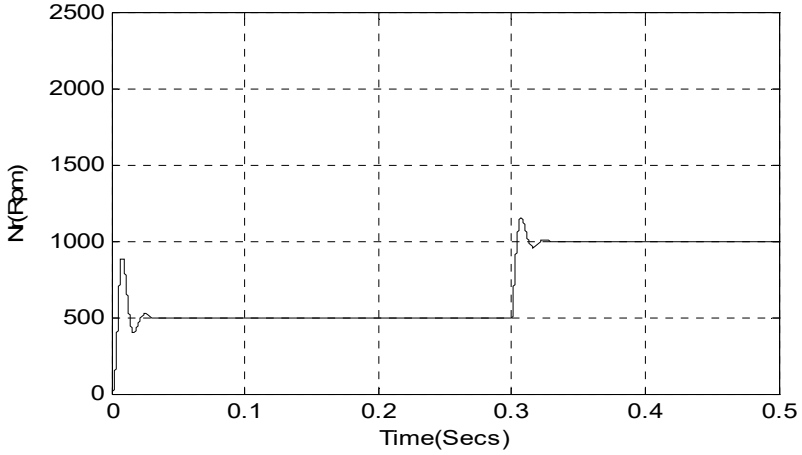


*Figure 10(f) Speed response of 4- switch VSI fed drive with $T_L$=5N-m and change of speed*

*Figure 10 Performance Analysis of 6-Switch and 4-switch VSI fed PMBLDC Motor for $T_L$=5N-m and change of speed from 500 rpm to 1000rpm*

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## 5. CONCLUSION

In this paper, comparison has been made between interleaved boost converter based 6-switch and 4-switch VSI fed PMBLDC motor drive. The performance evaluation of the proposed work is investigated under different operating conditions. From the results, it is observed that transient performance of 6-switch VSI fed PMBLDC motor drive is superior to 4-switch VSI fed PMBLDC motor drive but its steady state response is poor. As for as torque ripple minimization is concerned, the 4-switch VSI fed PMBLDC motor is better compared to 6-switch VSI fed BLDC motor because of less requirement of dc link voltage for 4-switch VSI. The torque ripple depends on dc link voltage of VSI. Number of switches are less in 4 –switch VSI, so, switching losses are also very less.

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