Journal of Theoretical and Applied Information Technology
31st August 2017. Vol.95. No.16

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

FLEXIBLE CHANNEL EXTRACTOR FOR WIDEBAND SYSTEMS BASED ON POLYPHASE FILTER BANK

[1]S. CAPPELLO, G.C. CARDARILLI, L. DI NUNZIO, R. FAZZOLARI, M. RE
[2]P. ALBICOCCO,

[1] University of Rome Tor Vergata, Via del Politecnico 1, 00133, Rome, Italy;

[2] INFN - Laboratori Nazionali di Frascati Via Enrico Fermi, 40, 00044 Frascati RM Italy;

E-mail: stefano.cap91@gmail.com, g.cardarilli@uniroma2.it,

di.nunzio@ing.uniroma2.it,fazzolari@ing.uniroma2.it, re@ing.uniroma2.it, pietro.albicocco@uniroma2.it

ABSTRACT

Some applications as Software Defined Radio (SDR) and Cognitive Radio require the analysis of wideband signals and/or the processing of multiple channels that can be located anywhere in the available band. These requirements can be satisfied using hardware platforms based on fast Analog to Digital Converters (ADCs) and reconfigurable hardware, such as FPGAs.
Unfortunately, while modern ADCs allow the acquisition of wideband signals at high sampling rates (many Gsps), FPGAs are not able to work with very high rates. In this work, authors propose a solution to overcome this problem in a class of applications. The solution is based on the coupling of a Time-Interleaved ADC (TI-ADC) with an FPGA front-end, exploiting the properties of a perfect reconstruction polyphase filter bank. The proposed system is able to select and process channels located anywhere in the input wide band and to re-aggregate two or more of them obtaining a new channel with variable width.

Keywords: *SDR, Cognitive radio, Polyphase filter bank, FPGA, TI-ADCs*

1. INTRODUCTION

Technology advances have a great impact on the architecture and the performance of the electronic systems. The connection is particularly evident in the case of telecom systems. For example, the performance improvements of the ADC and the digital circuit allow to develop innovative architectures where the boundary between the analog and the digital parts is constantly moved toward the first one.

In this way, a number of advantages are obtained: the number of the analog components used in the design is reduced, with the consequent reduction of the related issues and the power consumption. The obtained architectures are less expensive and more reliable, and present higher performance and flexibility. At the present, the Software Defined Radio (SDR) [1], [2] and, in particular, the cognitive radio [3], [4] represent the most extreme examples of this trend toward flexible architectures in radio systems. These two approaches normally use high-performance ADCs, for the analog to digital front-end, and high-performance FPGA, for the reconfigurable high-speed processing. In these new architectures, a critical point is the interface between the ADC and the FPGA. The speed of this interface strongly impacts on the system flexibility, in terms of operating frequency range, of the resulting system. Frequently, such systems require to analyze a very wide frequency band for selecting and processing one or more smaller portions, where the information is really present. For example, some SDR systems can have a channel allocation variable in the time (in a given frequency band) [5]. The frequency flexibility is even a more critical parameter in the cognitive radio systems, where the device must be able to verify autonomously the spectrum usage, detecting the available channels and their quality. Then, according to the above verification results, the system selects the proper communication frequency band [3], [4] and the other parameters of the transmission. From the above scenario, we can derive three main characteristics that an advanced system architecture must own:

- Capability to deal with a wide frequency band where the channels are allocated.

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

- Use of reconfigurable hardware in order to allow the implementation of different communication standards during the system life.
- Capability to extract and process any channels located anywhere in the available wide band.

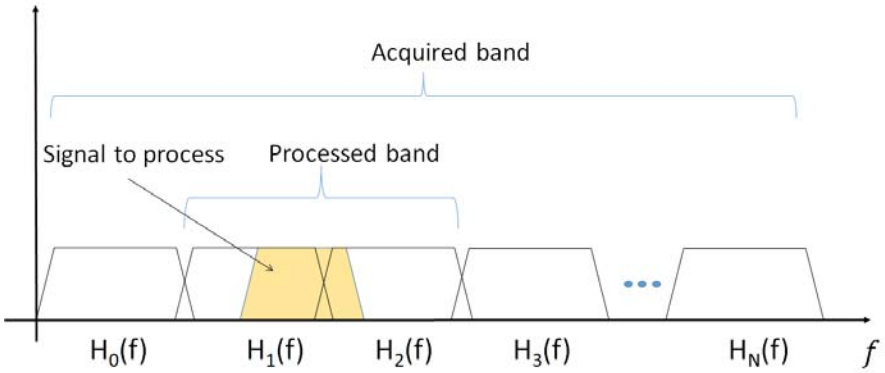

Fig. 1. Operation overview

The wide band capability can be obtained by using the modern RF-ADCs, based on Time Interleaved ADC (TI-ADC) [10]. The reconfigurability can be obtained using reconfigurable devices such as the FPGAs [11]. However, FPGAs processing speed is limited if compared with the sampling rate of the RF-ADC, that can reach sampling frequency of some GHz. Although modern FPGAs are equipped with gigabit transceivers for high-speed data transmission, their clock frequency is limited to few hundreds of MHz. Consequently, the GHz signals cannot be processed directly and it is needed to study suitable techniques that make possible the processing with a lower clock frequency.

This paper proposes a technique for increasing the bandwidth of the explored spectrum, overcoming the effects related to the limited clock speed of the modern FPGAs. The solution exploits the interleaved parallel organization of the TI-ADC outputs, which is very suitable for the input of a polyphase filter bank [14].

Our solution proposes the cascade of a TI-ADC with a near perfect reconstruction polyphase filter bank. The latter is used for decomposing the wide band in a number of elementary channels.

Using the polyphase implementation, the filter bank allows to increase the ADC sampling rate maintaining the FPGA processing rate sufficiently low, this aspect will be discussed in Section 2.

A remarkable peculiarity of our proposal is the possibility to re-aggregate two or more of such elementary channels for obtaining a wider channel with variable width. In this way, we obtain a very flexible structure, while the clock frequency is minimized.

This aspect is very important, for increasing the width of the analyzed band but maintaining the processing clock suitable for a FPGA implementation. Moreover, the proposed structure allows to overcome the performance limitations on the overall spectrum width present in previous works. In fact, the digital front ends proposed in literature for SDR and Cognitive radio are unable to increase the bandwidth of the analyzed spectrum since they don't reduce the sample rate required for the processing [8], [9]

The paper organization is the following. In Sec. 2 the proposed solution is explained and analyzed, while the hardware implementation and the experimental results are discussed in Sec. 3. Finally, in Sec. 4, some conclusions are drawn.

2. PRINCIPLE OF OPERATION

In our study, we suppose to process one or more channels having bandwidth smaller than the overall analyzed band that is acquired by the ADC. The proposed technique performs the extraction of the useful channels in two steps. In the steps the overall band is divided in a number

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

of sub-bands of fixed bandwidth. In the second step the sub-bands containing the information are extracted and eventually re-aggregate (if the channel belongs to more than one sub-band). The processing, both in the step one and step two, is based on a near-perfect reconstruction polyphase filter bank [14].

Polyphase Filter banks are used in many applications, as radar [17],[18],[19], voice analysis, satellite telecommunications etc.. They are able to reduce the processing rate in every point of the system, reducing also the number of operations to perform. This allows to reduce the hardware resources required for the realization of the filter banks.

With reference to Fig. 1 the "acquired band" is the band provided by the TI-ADC (i.e. the band we can analyze that, as discussed above, can reach some GHz) meanwhile the "processed band" is the sub-band (corresponding to one or more channels) where the information is present. This band will be extracted by the FPGA and processed in the SDR/cognitive radio applications.

In the proposed approach, the acquired band is decomposed in N elementary channels using a perfect reconstruction poly-phase filter bank. The processed band of the interest signal is then obtained by aggregating one or more of these elementary channels, depending on the signal bandwidth.

This structure has the flexibility required by the SDR and the cognitive radio applications and reduces the processing rate of FPGA. The only limitation present in this approach is that the processed channel is obtained aggregating an integer number of elementary channels and, consequently, the processed band can be quite greater than the band of the signal. This drawback can be reduced increasing the number of elementary channels N and consequently reducing their bandwidth.

In the following these operations will be discussed in details.

2.1 Channelization

In our system, we obtain an efficient implementation of the channelizer exploiting the interleaved data structure provided by the modern TI-ADC. Time interleaved ADCs send the analog input, in parallel, to several converters (ADC cores) that sample the signal at a certain frequency but with a different phase and convert it independently (see Fig. 2). This data structure can be directly used for feeding a filter decomposed in polyphase form [14]. Looking at the output interface of modern RF-ADCs, they provide a data frame suitable for the poly-phase decomposition, with an order equal to the number of the ADC channels (typically two or four channels). This approach allows to increase the ADC sampling rate, limiting the data rate of the polyphase components [12], [13]. For example, the converter used in this work, the EV8AQ160 TI-ADC, has 4 cores and provides the output of each core on a separate bus. Using these devices, a system composed of a N-Channel ADC and a FPGA, can reach a sampling rate of N*Fmax, where Fmax is the maximum frequency of the FPGA. For example, assuming Fmax = 400 MHz and an 8-channels TI-ADC, it's possible to reach 3.2 GHz of sampling rate (corresponding to a maximum bandwidth of 1.6GHz). For N input channels, the polyphase Filter Bank divides the overall band in N sub-bands. Small values of N can lead to high clock frequency and/or small granularity in the sub-band width. For this reason, it is possible to use the SERDES interfaces, present in the FPGA, for splitting each of the N channels in M sub-channels, obtaining a filter bank that divides the overall band in N*M sub-bands.

Because in SDR and cognitive radio applications data can be located anywhere in the available band, there is the possibility that the signal band, to extract and process, spans more adjacent elementary channels. As a consequence, two or more elementary channels must be aggregated in a macro-channel (processed channel). This operation can be accomplished only if the polyphase filter bank involved in the processing owns the perfect reconstruction property. This property is discussed in [14] and requires the fulfillment of two constraints:

- The filter bank must be not critically sampled, in order to avoid aliasing.
- No amplitude and phase distortion are present.

When one of these properties is not satisfied, the system is said Nearly Perfect Reconstruction (NPR). In our case, both the prototype filter used for the channelizer and the prototype filter used for the aggregator respect these constraints.

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

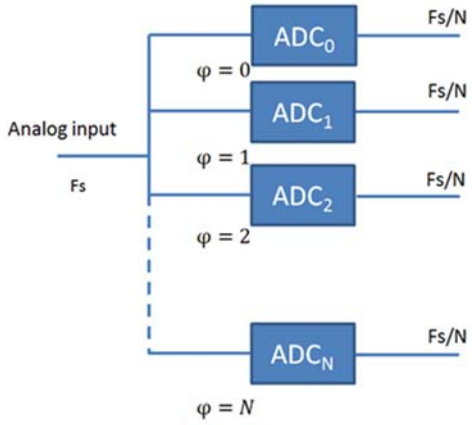

Fig. 2. General Time Interleaved ADC functional block

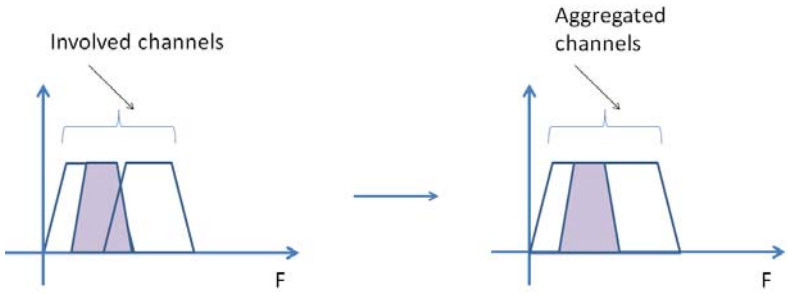

Fig. 3. Adjacent channel aggregation

Channel aggregation

As previously discussed, SDR and cognitive radio systems must be able to operate on channels located anywhere in the available band. From the above discussion, this constraint implies the capability to extract signals located on adjacent channels.

These adjacent elementary channels must be re-aggregated to reconstruct the signal to be processed. We propose to aggregate these channels using a M-channels synthesis filter bank, where M is the number of channels to aggregate. Fig. 3 shows an example of aggregation of two adjacent channels.

3. HARDWARE IMPLEMENTATION

The validation of the proposed method has been performed through the following steps

- Floating Point Simulink simulation
- Fixed Point Simulink Implementation
- Detailed design of the structure
- Hardware implementation and test

The devices used for the implementation are a Xilinx FPGA Virtex6 and a EV8AQ160 TI-ADC [15]. The latter is a 4-cores ADC with 4-interleaved 8-bits channels, a maximum sampling rate of 5 GSPS and an analog bandwidth of 2 GHz. In order to simplify the implementation, only 2 of the 4 interleaved cores have been used, reaching half of maximum allowed sampling rate (i.e., two-channel mode with a sampling rate of 1.25 Gsps).

Journal of Theoretical and Applied Information Technology
31st August 2017. Vol.95. No.16

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

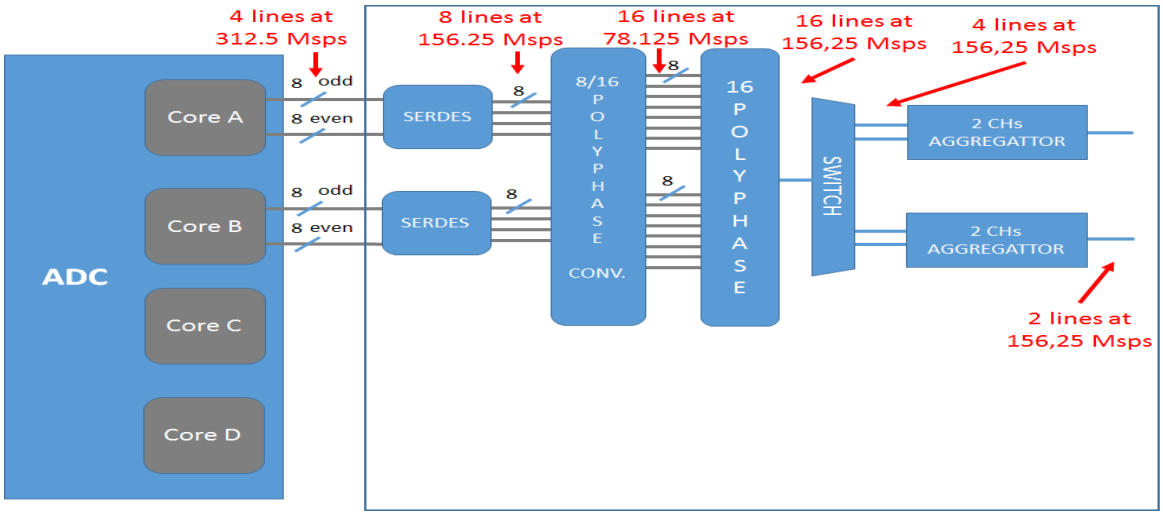

Fig. 4. System Block diagram

The channel re-aggregation has been performed only on two adjacent channels. However, the proposed technique can be extended in order to exploit all the four ADC cores and/or to aggregate more than two channels. The block diagram of the system is shown in Fig. 4.

Signals are sampled by the TI-ADC and are sent to the FPGA, where the proposed algorithm has been implemented. In the FPGA, we also implemented a MicroBlaze [16] soft processor, for debug purposes.

MicroBlaze is a 32-bit Reduced Instruction Set Computer (RISC) soft processor, that can be used in several application fields such as industrial, medical, automotive, consumer, and communication infrastructure markets among others. MicroBlaze is a highly configurable and easy to use processor and can be used across FPGAs and All Programmable (AP) SoC families

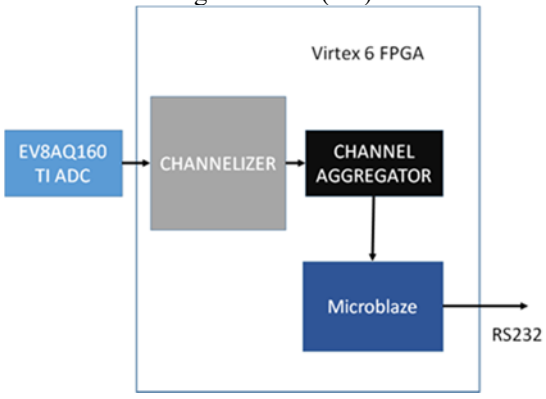

Fig. 5. Detailed architecture of system

This Microprocessor support more configuration options. Some of the key configuration options are Instruction/Data Cache, Floating Point unit, Memory Management Unit etc. With highly flexible and configurable core, user can implement virtually any processor use case, from a very-small-footprint state machine or microcontroller to a high-performance, compute-intensive micropro-cessor-based system running Linux. It is very suitable for the implementation, inside the FPGA, of mixed digital systems composed by a Processor and a reconfigurable architecture [20], [21], [22], [23]. In our application the MicroBlaze microprocessor is used to read data from a FIFO memory, where the processing results are stored, and to send them to a PC, using an RS232 serial interface. The results are finally evaluated on a PC, using MATLAB. Fig. 5 shows the structure of the implemented processing system.

Each core of the ADC has two 8-bits buses at 312.5 Msps. In order to decrease the sample rate, the two 8-bits buses of each core are down-sampled in four 8-bits buses using the SERDES of FPGA [24]. In this way eight 8-bits signal buses, at a rate of 156.25 Msps, are obtained. In order to further reduce the sampling rate, a block for increasing by 2 the polyphase input components is introduced. It resamples and rearranges the 8 input components for obtaining 16 parallel inputs. In this way, the sample rate of the obtained 16 buses of input is reduced to 78.125 Msps. After this rate reduction, the signal is channelized by a 16 channels perfect reconstruction poly-phase filter bank of analysis.

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

The architecture of a perfect reconstruction filter bank is shown in Fig. 6 and discussed in [25]. This filter bank is composed, for each elementary channel, of one sub-filter, one interpolator and a final IFFT.

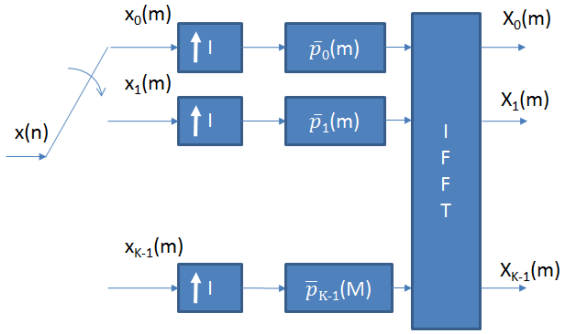

Fig. 6. Not critically sampled polyphase filter bank

The design parameters of the prototype filter are: cutoff-frequency (39.0625 MHz), stop-band frequency (78.125 MHz) and number of taps (128). The frequency impulse response of the prototype filter is shown in Fig. 7. It has been obtained using the rules presented in [27]

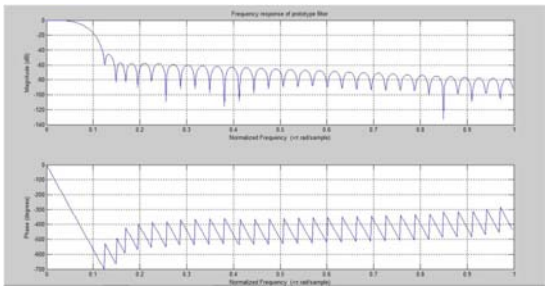

Fig. 7. Frequency response of the prototype filter

The sub-filters coefficients have been obtained using the following expression presented in [25]:

$$\bar{p}_\rho(m) = h(Mm - \rho), \rho = 0,1...K-1 \quad (1)$$

where *h(m)* is the impulse response of the prototype filter, *K* is the number of sub-bands and *M* is the overall decimation ratio.
The interpolation factor I is introduced in order to implement the non-critical sampling. This operation increases the sampling rate of a factor *I* with *K=I*M*.
The 16-points IFFT is based on a Decimation in Time architecture. For the IFFT implementation, we started from a single butterfly Radix-2 and then replicated it in order to obtain the complete 16 IFFT.

The re-aggregation is performed by a 2-channel synthesis filter bank. As for the channelizer, the prototype filter used for the re-aggregator must satisfy the condition of perfect reconstruction. The impulse response of the prototype filter used for the re-aggregation, has been obtained by sub-sampling the impulse response of the prototype filter used for the channelizer. In our implementation, we realized two re-aggregator blocks able to aggregate 2 channels each one. In this way, it is possible to re-aggregate up to 2 macro-channels, located everywhere in the initial band. Re-aggregator outputs are sent to a PC by the Microblaze soft-processor, that is also used for configuring all the registers of the EV8AQ160. The entire system has been implemented on a Xilinx Virtex 6 XC6VLX240T FPGA using the tool Xilinx System Generator.

System Generator for DSP is a high-level tool for the design of high-performance DSP systems using Xilinx It provides system modeling and automatic code generation from Simulink and MATLAB [26]. All the processing elements have been implemented using this tool. Since the IP cores available for the FFT computation, in Xilinx environment, implement serial transform, we needed to realize a custom architecture. The 16-point IFFT has been realized using the Decimation in Time structure. Implementation started with a single Radix-2 butterfly and then it has been replicated to obtain the 16-point IFFT. The resulting architecture is shown in Fig. 8.

All elements are pipelined to increase timing performance, since the parallel implementation of IFFT presents the congestion of interconnects.

Synthesis and Place & Route has been performed using the Xilinx ISE IDE.
Tab. 1 shows the implementation results in terms of hardware resources and maximum clock frequency.

Table 1: Resource utilization

Resources	Used
Slice Reg	29,797 out of 301,440
Slice LUTs	21,169 out of 150,720
DSP48E	371 out of 768
Maximum frequency	159.109MHz

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

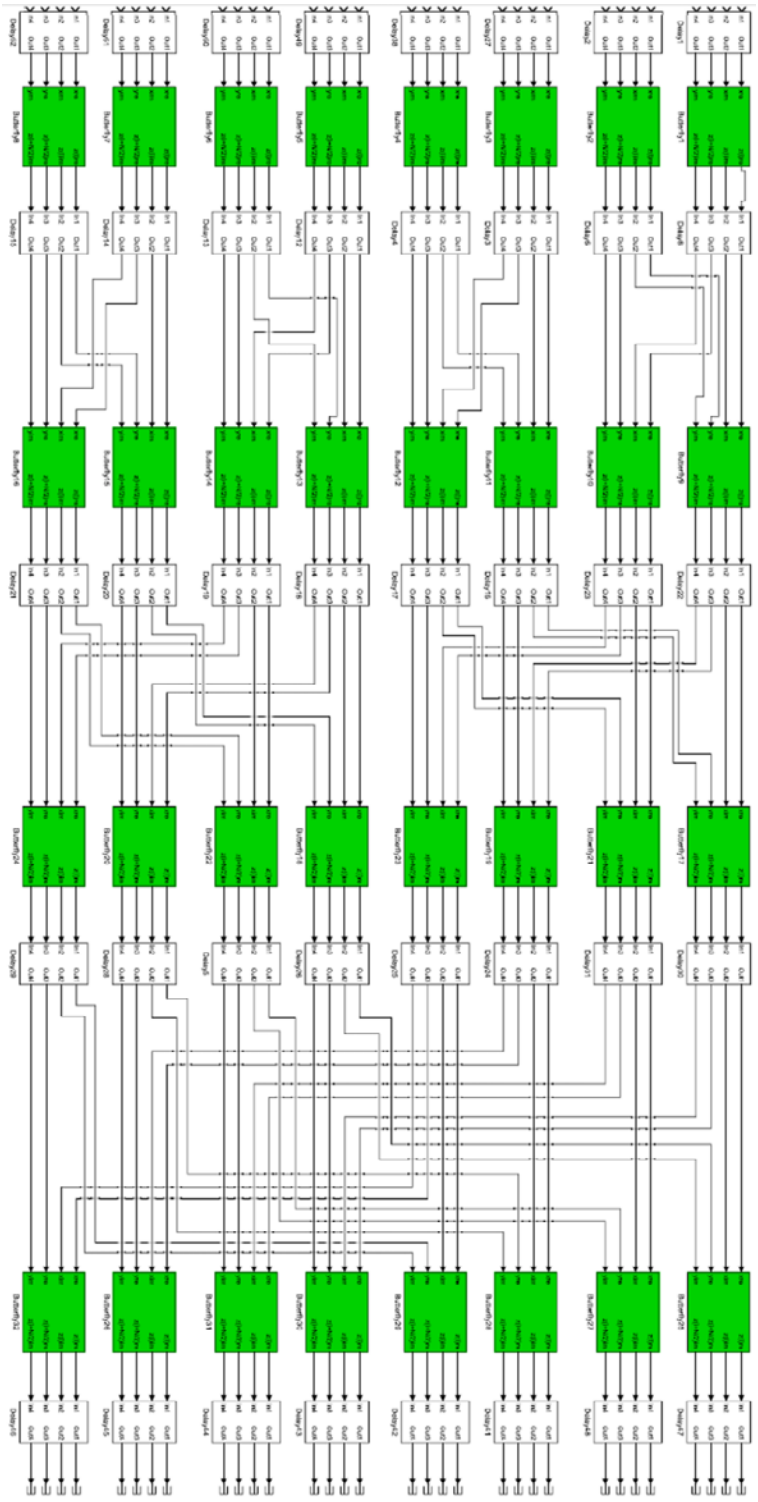

Fig. 8 FFT architecture.

Journal of Theoretical and Applied Information Technology
31st August 2017. Vol.95. No.16

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

In Fig. 9 is shown the FPGA layout.

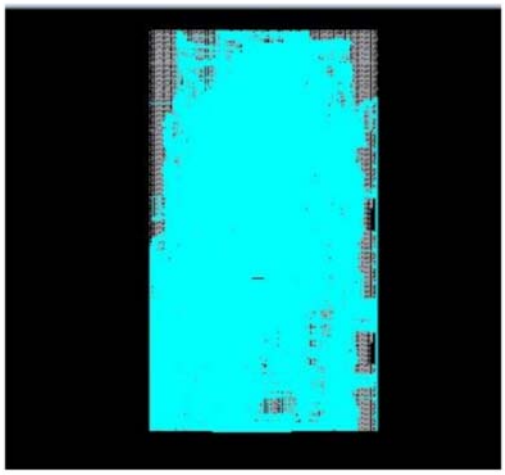

Fig. 9. FPGA layout

Different experiments have been performed in order to verify the performance of the system. Fig. 9 shows the results for one of the experimental scenario. Five different tones are applied at the input of the system according to the frequency allocation shown in the figure. These tones have been generated by using the arbitrary waveform generator AFG3252 by Tektronix. In this experiments we re-aggregate the elementary channels 5 and 6 and the elementary channels 7 and 8 obtaining two channels to process. The spectra of the reconstructed signals are shown in the upper part of Fig. 10. The spectra have been obtained from the output digital signals by the FFT, computed on the PC using the MATLAB program.

4. CONCLUSIONS

In this paper, a new structure for the processing of channels in a wideband spectrum has been presented. The architecture is based on a TI-ADC and cascaded with two blocks implementing the channel decomposition and channel aggregation, based on a perfect reconstruction filter banks. The architecture uses the polyphase approach for exploiting the data structure of time interleaved ADCs. This allows to reduce the clock frequency of the digital system used for the processing. The proposed method has been implemented in hardware and tested in the case of an ADC working with an overall sampling rate of 1.250 GHz coupled with a 16-channel channelizer. With these parameters, the obtained elementary channels have a sampling rate of 156.25 MHz (the frequency is higher for the oversampling by 2 of the 78.125 MHz sampling rate) and the re-aggregated channels have the same rate of 156.25 MHz.

Experiments have been carried out for a scenario of 5 sinusoidal signals. The results show the correctness of the proposed method, while the hardware complexity of the processing system is compatible with the modern FPGA.

The analysis performed demonstrates the feasibility and the usefulness of the proposed approach.

In this paper the validation of the methodology has been performed using single tones. In order to improve the performance evaluation, we planned new tests using modulated signals instead of single tones.

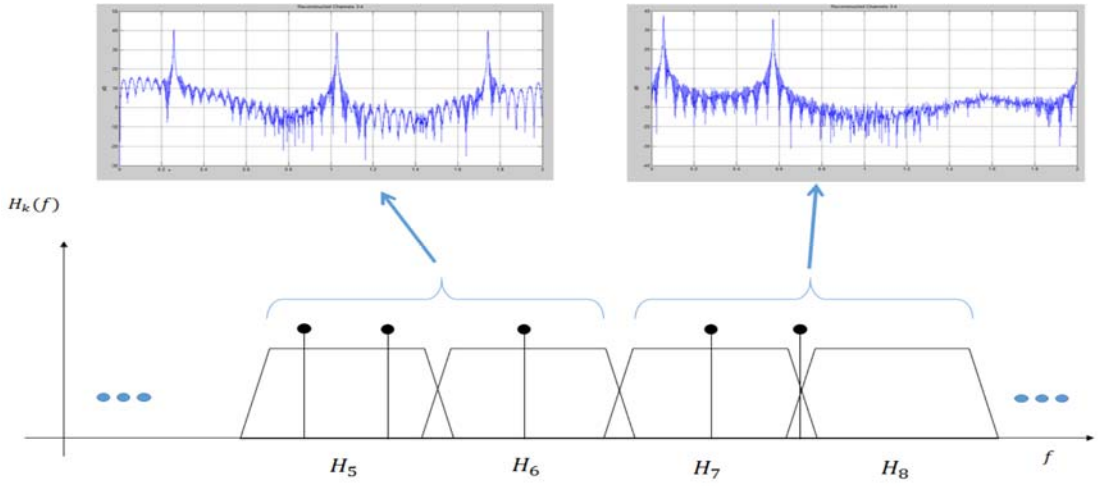

Fig. 10. Experimental results

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

These tests will allow toestimate the errors introduced by the system in terms of BER.

In order to evaluate the potentiality of the methodology, let consider a FPGA able to process data at a processing frequency F. Our method allows to extract and process any channels located anywhere in the available bandwidth of a high speed ADC working at a frequency = N*F/2, where N is the channels number of the channelizer. The factor 2, as explained in previous sections, derives from the interpolation by 2 required for the perfect reconstruction.

Considering the capability of modern FPGAs to process data at frequencies of more than 500 MHz, the proposed technique can be used to analyze and extract channels in a very wide band spectrum.

This property is very useful in SDR and Cognitive radio systems where it is required the capability to extract and process channels located anywhere in the wide band spectrum.

5. ACKNOWLEDGMENT

The authors would like to thank P. Ciambrone e M. Beretta of INFN Laboratori Nazionali di Frascati for the support in experiments and Xilinx Inc, for providing FPGA boards and software tools by Xilinx University Program.

REFERENCES:

[1] Buracchini, E. "Software radio concept" , 3rd ed. *IEEE Communications Magazine Volume 38, Issue 9, September 2000, Pages 138-143*

[2] Jondral, F.K. "Software-defined radio - Basics and evolution to cognitive radio", *3rd ed. Eurasip Journal on Wireless Communications and Networking Volume 2005, Issue 3, 1 August 2005, Pages 275-283*

[3] Haykin, S. "Cognitive radio: Brain-empowered wireless communications",*3rd ed. IEEE Journal on Selected Areas in Communications Volume 23, Issue 2, February 2005, Pages 201-220*

[4] M. Song, C. Xin, Y. Zhao and X. Cheng, "Dynamic spectrum access: from cognitive radio to network radio", *IEEE Wireless Communications, vol. 19, no. 1, pp. 23-29*

[5] Ian F. Akyildiz, Won-Yeol Lee, Mehmet C. Vuran , Shantidev Mohanty: "NeXt generation/dynamic spectrum access/cognitive radio wireless networks:A survey" , *3rd ed. Computer Networks Volume 50, Issue 13, 15 September 2006, Pages 2127-2159*

[6] Zamree Che-aron, Aisha Hassan Abdalla, Khaizuran Abdullah,omer Mahmoud "A comprehensive study of routing protocols for cognitive radio networks" *Journal of Theoretical and Applied Information Technology pp 521 - 536 Vol. 47. No. 2 – 2013*

[7] Amritha R, Anjali T, Aswathylakshmi P, Greeshma V, Dr T Sudha:" Tv White Space Detection Using Usrp", *Journal of Theoretical and Applied Information Technology 31st December 2015 -- Vol. 82. No. 3 – 2015*

[8] Abhishek Ambede, Smitha K. G. and A. P. Vinod "A Low Complexity Uniform and Non-Uniform Digital Filter Bank based on an Improved Coefficient Decimation Method for Multi-Standard Communication Channelizers" *Proceedings - 8th International Symposium on Signal Processing and its Applications, ISSPA 2005, 1, art. no. 1580246, pp. 263-266.*

[9] Hu J1, Zuo Z1, Huang Z1, Dong Z1.:" Dynamic Digital Channelizer Based on Spectrum Sensing." *PLoS One. 2015 Aug 26;10(8):e0136349. doi: 10.1371/journal.pone.0136349.*

[10] David G. Nairn: "Time-interleaved analog-to-digital converters", *3rd ed. Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*

[11] Cummings M. Haruyama S. "FPGA in the Software Radio" *IEEE Communications Magazine Volume 37, Issue 2, February 1999, Pages 108-112*

[12] Vogel, C. and Johansson, H: "Time-interleaved analog-to-digital converters: Status and future directions": *2006 IEEE International Symposium on Circuits and Systems; Kos ISCAS*

[13] *www.ti.com/lit/wp/snaa111/snaa111.pdf*

[14] P. P. Vaidyanathan. "Multirate Digital Filters, Filter Banks, Polyphase Networks, and Applications: A Tutorial" *proceeding of the IEEE, Vol. 78, N. 1, January 1990*

[16]http://www.e2v.com/products/semiconductors/adc/ev8aq160/

[15] *https://www.xilinx.com/products/design-tools/microblaze.html*

[17] Gian Carlo Cardarilli, Luca Di Nunzio, Rocco Fazzolari, Amirhossein Fereidountabar, Filippo Giuliani, Marco Re Lorenzo Simone: "Comparison Of Jamming Excision Methods

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

For Direct Sequence/spread Spectrum (Ds/ss) Modulated Signal"
Journal of Theoretical and Applied Information Technology Vol 95 Issue 13, 15th of July 2017

[18] Re, Marco, Cardarilli, Gian Carlo, Del Re, Andrea, Lojacono, Roberto, Rovigatti, G., Piloni, V. Efficient implementation of a filter bank architecture for demultiplexing in satellites applications
Conference Record of the Asilomar Conference on Signals, Systems and Computers, 1, pp. 569-573

[19] Re, M., Del Re, A., Cardarilli, G.C.
Efficient implementation of a demultiplexer based on a multirate filter bank for the skyplex satellites DVB system
(2002) VLSI Design, 15 (1), pp. 427-440

[20] Cardarilli, G.C., Di Nunzio, L., Fazzolari, R., Re, M., Lee, R.B.
Butterfly and inverse butterfly nets integration on Altera NIOS-II embedded processor
(2010) Conference Record - Asilomar Conference on Signals, Systems and Computers, art. no. 5757737, pp. 1279-1283

[21] Cardarilli, G.C., Di Nunzio, L., Fazzolari, R., Re, M. "Algorithm acceleration on LEON-2 processor using a reconfigurable bit manipulation unit", *(2010) WISES 2010 - 2010 8th IEEE Workshop on Intelligent Solutions in Embedded Systems, art. no. 5548433, pp. 6-11*

[22] Cardarilli, G.C., Di Nunzio, L., Fazzolari, R., Re, M. "Fine-grain reconfigurable functional unit for embedded processors", *(2011) Conference Record - Asilomar Conference on Signals, Systems and Computers*

[23] Cardarilli, G.C., Di Nunzio, L., Re, M.
"Arithmetic/logic blocks for fine-grained reconfigurable units" *2009 IEEE International Symposium on Circuits and Systems, ISCAS 2009.*

[24] Source-Synchronous Serialization and Deserialization
]https://www.xilinx.com/support/documentation/application_notes/xapp1064.pdf

[25] R. E. Crochiere and L. R. Rabiner. "Multirate Digital Signal Processing" *SBN-13: 978-0136051626*

[26] G.v Ganesh, B. Murali Krishna, K. Sravan Kumar T.prathyusha, R.venkatesh, T.vineel Jessy. "Fpga Implementation of Ofdm Transmitter Using Simulink and Xilinx System Generator" *Journal of Theoretical and Applied Information Technology 10th August 2015. Vol.78. No.1*

[14]M. Harteneck, S. Weiss, R.W.Stewart: "Design on near perfect reconstruction oversampled filter bank for subband adaptive filters" IEEE Transactions on Circuits and Systems II: Volume 46, Issue 8, 1999, Pages 1081-1085