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FPGA IMPLEMENTATION OF HIGH SPEED MEDICAL IMAGE SEGMENTATION USING GENETIC ALGORITHM

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ABSTRACT

Nowadays, image analysis plays a key role in processing of the medical images such as retinal image, cardiac image and brain MRI images in bio-medical field. Medical Image Segmentation (MIS) is a process of obtaining the different intensity levels of the image and extracting the features for analysis. Some of the existing algorithms are capable of extracting a section of image but not able to find an optimum threshold for image segmentation. So, a novel image segmentation algorithm with different thresholds is based on Genetic Algorithm (GA) on Field Programmable Gate Array (FPGA) has been introduced in this paper. Here the optimum threshold values are used to segment the same image as well as similar kind of images, which is obtained from same kind of biomedical imaging instruments. The proposed FPGA architecture for image segmentation is time as well as power efficient algorithm.

Keywords: *Segmentation process, Genetic Algorithm, Field Programmable Gate Array.*

1. INTRODUCTION

Now a day, image processing plays a very important role in the Medical Image (MI) analysis. So, to enhance MI there is an algorithm called GA which was proposed by J. Holland in 1975. It has been extensively utilized in several areas, such as image processing combinatorial optimization, automatic control pattern recognition and artificial intelligence, etc. It is an efficient global search algorithm, where the applications required excellent optimization. A new hardware architecture is explicitly designed to achieve the realization of parallelism GA. It has to follow units such as genetic operator, objective function and fitness evaluator. The individual unit is implemented with the help of a FPGA chip. FPGA has special features such as unique flexibility and scalability to handle many engineering applications that help to improve the computation speed [1]. Compact Genetic Algorithm (CGA) has been implemented in Verilog HDL. It is simple and 1000 times faster than software execution and with this, highly deceptive problems can be solved [2].

A novel RTL structure for time efficient GA has been introduced to increase the efficiency of image segmentation. The goal of using GA and CNN is to make fast, simple bit by bit operation and parallel searching. This parallel processing will make an algorithm to speed up the process by utilizing time efficiently [3]. The Gaussian Markov Random Field (GMRF) model with Iterated Conditional Modes (ICM) does not give the best results. So, there is another new algorithm for image segmentation is GAGMRF. This gives the best results compared to the GMRF in terms of accuracy and execution time [4]. An efficient image segmentation with GA by considering four gate levels and it has successfully applied to gray level Medical MRI images. This algorithm requires more number of generations and larger population size with increased noise levels [5]. GA based FCM clustering has introduced for MRI brain image segmentation. MRI brain image was segmented using FCM clustering technique give the best results compared to other clustering techniques. Multilevel thresholding using GA with fuzzy sets is the technique for efficient segmentation process. In this, different type of

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membership functions was used to get optimized parameters for segmentation [7]. Another new quantum GA was presented for image subdivision process. In this parameter like specificity(S), over segmentation (O+), homogeneity (H) and under segmentation (O-) were optimized to get the best segmentation of the image. These parameters improve the image quality and execution time of the algorithm [8].

Some researcher used fusion methods, which is based on GA method that use two types of segmentation technique like Iterative Self Organizing Data (ISODATA) and Self-Organizing Map and Hybrid Dynamic Genetic Algorithm cooperation method (SOM-HGA) to carry out the image segmentation. These two segmentation methods improve the results in separation of the image [9]. Another efficient image segmentation method based on the improved threshold of GA was also been introduced. Here very fine areas of the image were segmented using optimized thresholding technique and calculation time was minimized effectively [10]. An adaptive genetic algorithm (AGA) has been implemented on Field Programmable Gate Array (FPGA) based on modular design. In this comparison has been done on hardware and software running time and conclude that hardware performance is better than software performance for genetic algorithm in the running time and accuracy [11]. The existing methods has limitations such as much execution time, less flexible and high cost. The proposed method with different thresholds by using GA in FPGA with area as well power efficient implementation for image segmentation is presented in this paper. The main aim of proposed work is to obtain best segmented image with less area, power and execution time using CSLA adder for FPGA implementation.

2. RELATED WORK

Vijai Singh et.al [12] has introduced the novel cardiac image segmentation algorithm. As we all know the heart is the most important part of the human body for proper supplying of blood to all parts of the human body. For prior identifications of these problems researchers have developed many algorithms in image processing. Manual cardiac image segmentation methods are very lengthy and difficult process. To overcome the issue, a new algorithm called simulated genetic algorithm was proposed. Firstly, noise was removed from the image, random generation of cut sets. With the assists of these cut sets fitness function for each chromosome was calculated. The fitness of the novel solution was compared with the fitness of the previous solution. If the fitness value is higher, then a new solution has kept otherwise algorithm will make the decision based on the temperature variations. Clustering technique was used in this is only for two dimensional feature vectors.

Songhua Xie et al. [13] has proposed the new algorithm to know the retina condition of the eye with an image segmentation process. Nowadays retinal disease is one of the common problem in the human beings. To identify condition of the retina, an innovative algorithm has been introduced. In this, they used GA and FCM for global optimization. Firstly, image segmentation used GA to obtain approximate solutions, later by keeping genetic approximate solution as initial value for FCM. FCM gave the global optimum solution and experimental results also concluded the effectiveness of the segmentation process in the retinal vascular image segmentation.

Robert Collier et al. [14] has introduced the efficient GA to solve the problem of FPGA placement. The placement problem can be solved by developing recombination operators. Genotype subspace was generated by recombining two parent genotypes and in some cases offspring were produced. An intuitive visualization technique was used to identify the violations and also helped in a development of new operators which exhibit improvement in performance over the standard recombination operators but execution can be increased with the increments in the number of iterations.

Mohammed Alansi et al. [15] has introduced the Adaptive Genetic Algorithm-based instrument for SDMA-OFDM Systems (GASOS) to enhance the computational complexity and performance. In order to minimize execution time of the algorithm, pipelined and parallelization data flow structures was implemented in this paper. A new GASOS based Multi User Detection (MUD) hardware was implemented on a FPGA. In this, resource utilization was optimized and clock cycles required for the algorithm were also reduced. To achieve real time implementation of MUD in SDMA-OFDM systems, GASOS used the parallelization. There was no flexibility of the hardware implementation.

Vishnu P et.al [16] has introduced a new hardware software (HW/SW) co-design for implementation of a reconfigurable Hardware based GA (HGA) accelerator. The hardware implementation of an algorithm was rigid in their architecture and it is difficult to reconfigure for

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different applications. A novel HGA design has been implemented to provide good flexibility as well configurability to design any kind of applications but accuracy and speed of the algorithm is less.

3. PROPOSED SYSTEM

The proposed method has the following operations such as ROM address generation, RAM address generation, Random number generator, cross over and mutation. There are several methods in a segmentation process. Those are time consuming, less flexible and worthless methods. To reach the best segmentation of the image, we have proposed a new method of image segmentation process. The block diagram of the proposed method is shown in the fig.1. In the proposed method, ROM address generator will generate the address for each of the pixel in the image. The image has a size of 128x128 pixels. Takes one pixel for segmentation at a time out of 128x128 pixel. We are applying the GA for image segmentation process to achieve the best segmentation of the image. In GA, there are several sets of chromosomes and each chromosome set is applied individually to the image pixels, to obtain best segmented image. The RAM address generator generates the address for each of the chromosome set. The random number generator will generate the random number for the chromosome set. After generation of the chromosome sets, cross over as well as mutation operation has been performed on the genes. The two register banks have been included in the proposed method for cross over and mutation operations.

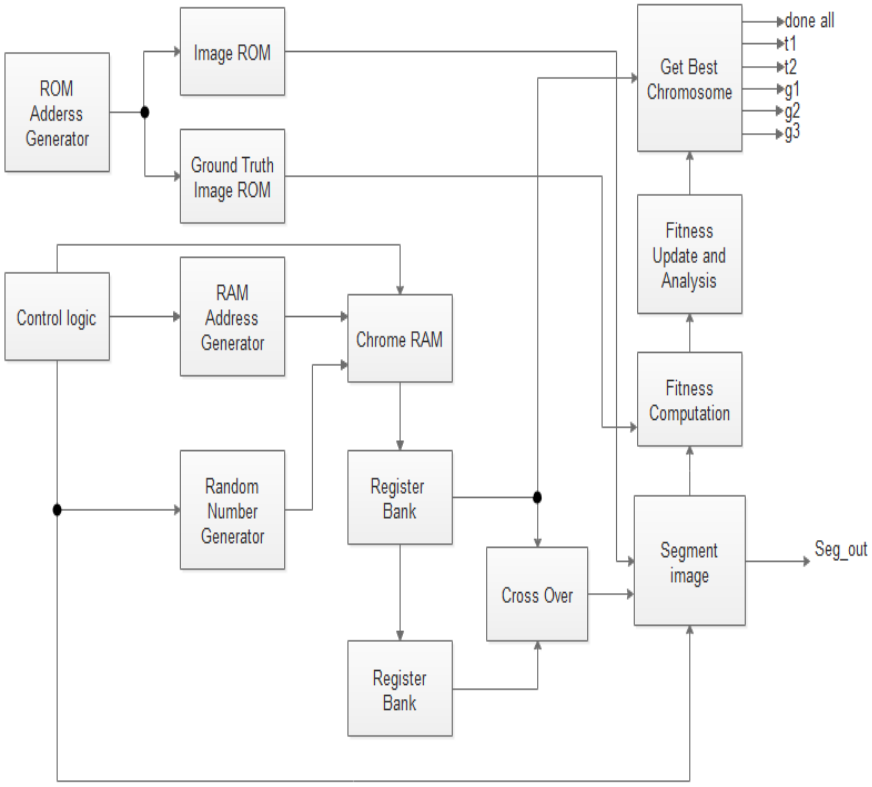

Figure 1: Block Diagram Of A Proposed System

The overall proposed block diagram is shown in fig.1. The address can be generated from the ROM address generator. That address value is connecting to the different kind of ROM such as image ROM and ground truth image ROM. Those addresses can be stored in that ROM. Control logic can be getting from the input from the logical block 1, which holds some multiplication and addition operation. The output of the control logic is connecting to the RAM address generator. The output of the RAM address generator and the random number generator can be connected to the chrome RAM. The read and

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write operation can be done in that chrome RAM. That output of the RAM is connecting to the Register bank, which is stored the values. That register bank value can be connecting to the register bank, which contains the exceeding input values. Output of second register bank can be connected to the cross over operation block as showed in the fig.1. After the cross over and mutation operation on the chromosome set, this chromosome set is applied to the image segmentation process to obtain the best chromosome set of genes such as t1, t2, g1, g2 and g3. Those values can be done after performing the fitness calculation. Finally, segmentation output can be getting from the segmented image block.

Every chromosome set is applied to the image to get the best segmentation. This process will be repeated for all the chromosome sets and obtaining the best chromosome set. Segmentation process has been repeated until the optimized threshold and gain values are achieved. After segmentation process, identifying the noised pixels and applying de-noised algorithm for all noised pixels to get noise free segmented images. With this, we will achieve the noise free segmented images in this proposed system.

- The implementation of segmentation of the image is done on FPGA with GA, the FPGA module design has some set of principles such as:
- The register is used at each timing synchronization sub-module output stage.
- Similar multiplexed logics are located in the same module.
- Different modules are used to place the various optimization objectives.
- Same module is used to place the loose constraint logics.
- The stored logic is placed in a separate module.
- Choosing the appropriate module scale.

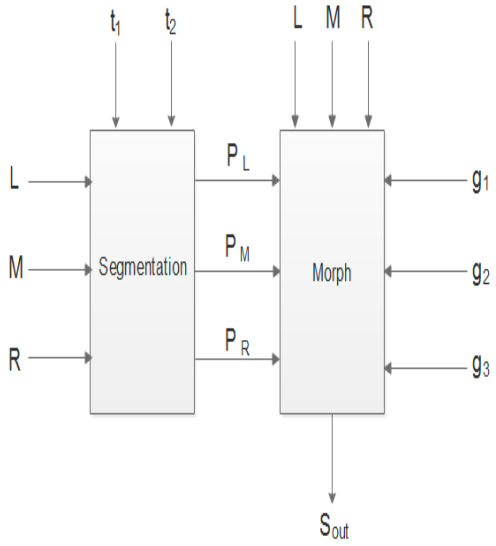

Figure2: Block Diagram Image Segmentation With Morphological Operations

The image segmentation of the architecture is shown in fig.2. The operation structure of morphological filter is shown in fig.2. That architecture contains average, comparator, logical gates, and multiplexer. The input value such as left (L), middle (M) and right (R) pixel can be given to the average section with different gain values (g1, g2, g3). After averaging operation, the Pout value can be given to the input of the comparator. The Cout value can be varied depend on the two thresholds (t1, t2). If the Pout satisfied with the two thresholds the result of Cout should be 1 else, it becomes 0. With the support of logical gates only can able to set the selection line of the MUX. If the PL, PM, PR value of the two AND gates should be input 010, the logical operation can be done as well as an OR gate result connected to the selection line of the MUX. Finally, segmentation output can be getting from the MUX output.

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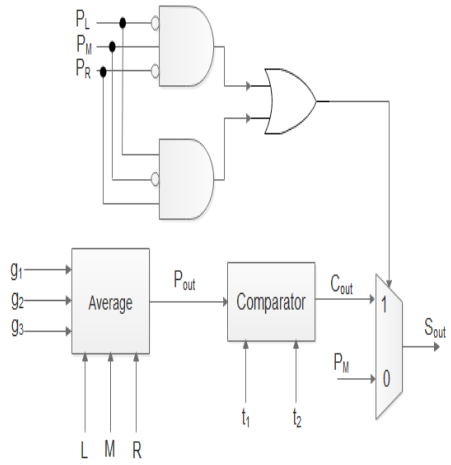

Figure 3: Block Diagram Of Morphological Filter

In the proposed work, we have introduced a new area with efficient CSLA adder instead of the normal adder], which is given in fig.4. This adder can achieve fast arithmetic operation in various data processing techniques. The main aim of using this adder is to minimize the area and power dissipation. CSLA is manipulated in many computational structures to cut the carry propagation delay. The elementary knowledge of this work is to habit BEC (binary to excess-1 convertor) instead of RCA (ripple carry adder) with Cin=1. By using fewer numbers of logic gates, we can derive BEC logic than n-bit FA (Full Adder).

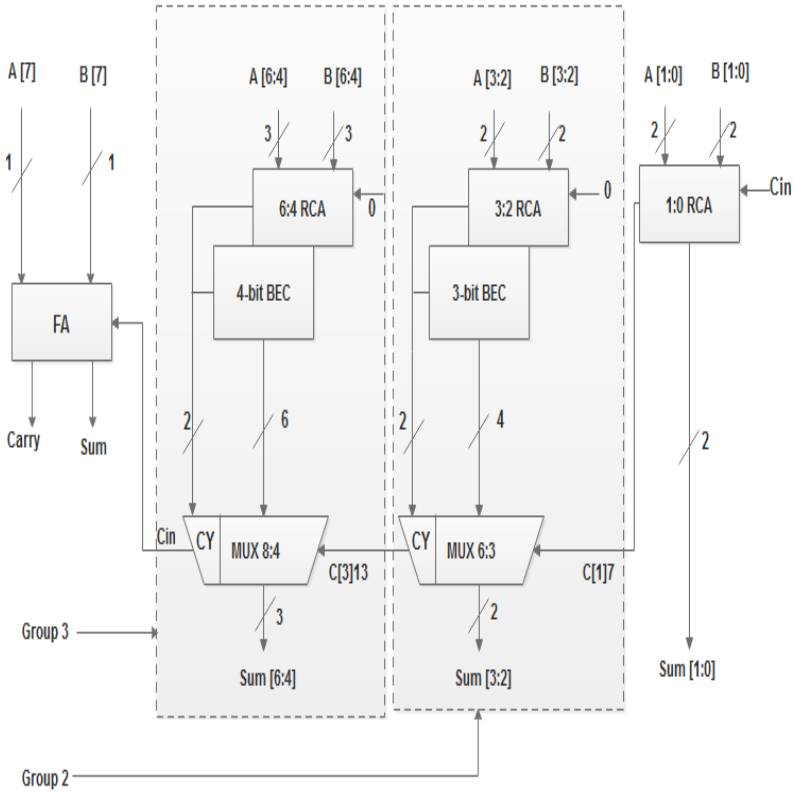

Figure 4: Low Area Carry Select Adder

The assembly of the proposed system using BEC for normal adder or RCA with Cin =1 to hike the power and area. 2-b RCA which has one full adder and one-half adder for Cin =1 where 3-b BEC is utilized which enhances one of the output from 2-b RCA. According to this consideration, the time delay has been reduced. It is the process on feedback values, which are the output of the mux is depended on the input of the mux. The input arrival time is lesser than the multiplexer selection input arrival time. Based on the selection line input Cin, this adder gives either BEC output or multiplexer output. While designing CSLA, the area will be reduced. The multiplexer delay and mux selection

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arrival time derived from the different kind of groups. Overall, power consumption and area will be minimized by the proposed method with the support of CSLA adder.

4. EXPERIMENTAL SETUP

The proposed method is implemented in Verilog language. Verilog code is synthesized by using cadence RTL compiler with 180nm CMOS technology and area, power and delay values are obtained. Similarly, RTL logic verification is done by MATLAB software as well as ModelSim software. MRI image of size 128x128 is converted into binary text formats and it read in Verilog code and verified by using the timing diagram. The complete work is done by using I7 system with 8 GB RAM with Ubuntu virtual machine for cadence. FPGA performance has been done in Xilinx software with different Xilinx device families. By using Xilinx, we obtained LUT, Flip flop, Slice, RAM, Maximum Frequency (MHz).

5. RESULTS AND DISCUSSIONS

Table 1: Comparison of area, power, delay for existing and proposed in 180nm CMOS technology

Relevancy (%)	Area (um2)	Power(nw)	Delay(ps)
Existing method[3]	-	-	185200000
Existing method[11]	720746	1017554593	1762
Proposed method	714307	1014839994.6	1745

The segmentation methods were extracting only portion of the image and also consuming much area, power and execution time as shown in the table.1. But in the proposed method extracting image features at different intensity levels and also area, power and execution time has been reduced as shown in the table.1.

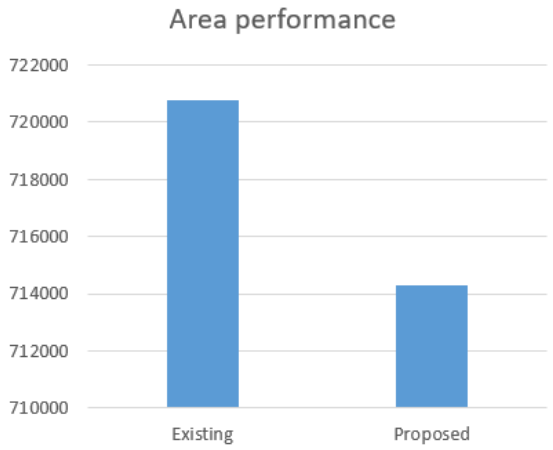

Figure 5: Flow Chart Of Area Performance

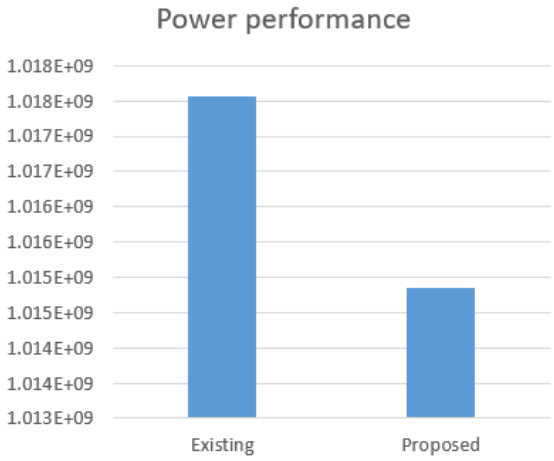

Figure 6: Flow chart of Power performance

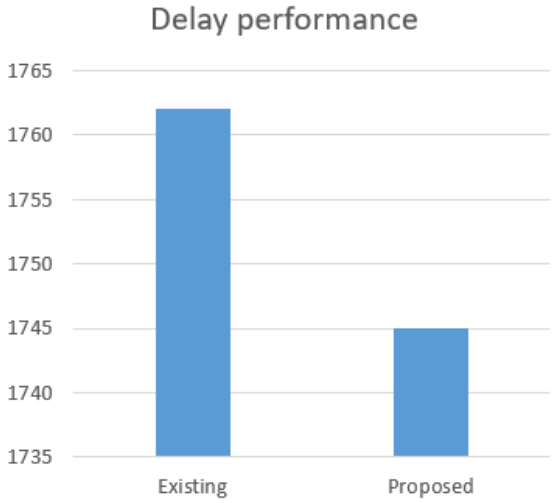

Figure 7: Flow Chart Of Delay Performance

The overall circuit performance such as area, power and delay is shown in fig.5, fig.6, and fig.7. From that flow chart, we can easily understand

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those three parameters are minimized in proposed method compare to the existing method.

As we can observe the tab (1) and tab (2), the proposed method will consume less area, delay and power in the operation then compared to the existing methods. The main aim of this work is to segment medical image very effectively with less number of hardware units with high speed. The input image and ground truth images are shown in fig.8 and fig.9. After applying GA to the input image with optimized segmentation parameters, an efficient segmented image is obtained as showed in fig.10.

Table 2: Comparison Of Slices, LUT, Flip Flop And Frequency For Existing And Proposed

Target FPGA	Circuit	LUT	Flip flop	Slice	RAM	Frequency
Virtex6	Existing	221/46560	150/46560	77/11640	2	170.909
	Proposed	183/46560	150/93120	78/11640	2	173.761
Virtex5	Existing	2629/12480	169/12480	880/3120	2	162.113
	Proposed	2608/12480	169/12480	933/3120	2	176.338
Virtex4	Existing	8623/10944	225/10944	5470/5472	2	92.073
	Proposed	8559/10944	172/10944	5470/5472	2	87.451

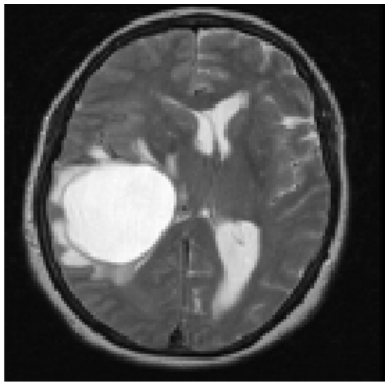

Figure 8: Input Image

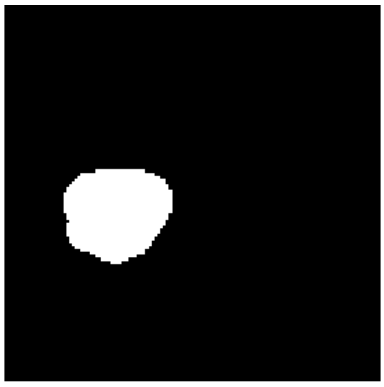

Figure 9: Ground Truth Image

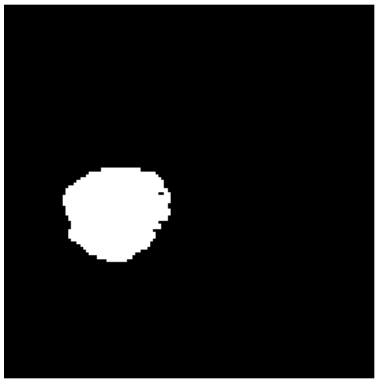

Figure 10: Segmented Output

6. CONCLUSION

In this paper, we have proposed a new algorithm to improve the performance of medical image segmentation with GA on FPGA implementation. Image is segmented with different intensity levels using thresholds and obtained the best segmented image with less hardware cost. The algorithm has been implemented for various devises of Xilinx FPGA. Performance analysis has been done on parameters like power, area and delay consumption of the system. From these results, we can conclude that the proposed system is power, area efficient and also consume less time in their operation compared to the existing algorithm.

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