# IMPLEMENTATION OF LOW POWER SRAM CELL STRUCTURE AT DEEP SUBMICRON TECHNOLOGIES

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## ABSTRACT

SRAM (Static Random Access Memory) is an significant component in memory devices where refresh operation required. To achieve high speed, SRAM has been used in most of the SOC chips. To get high reliability and low power consumptions in various applications a low power Static RAM is needed. This paper concentrates on reducing the dissipation of power during write operation in CMOS Static RAM cell for various frequencies. Here different cell SRAM cell structures like single bit SRAM, Stable SRAM cell respectively implemented and those are compared with the proposed SRAM Cell construction. Generally, power indulgence happens through the write operation because of charging and dis-charging of the SRAM Cell bit line, it is the major problem in the Static RAM cell. In this work, the Static RAM cell proposed which operates at low power compared to existing models. The comparative analysis performed in the DSCH and Microwind tools by applying technology node as 180nm.

**Keywords**: *SRAM, STABLE SRAM Cell, Single bit SRAM Cell, 180nm*

## 1. INTRODUCTION

Prediction of exon regions is a substantial area of research in the field of genomics. Generally, in embedded systems and microprocessor system-on-chip SRAM is used for cache memory. This because the SRAM is faster than Dynamic random access memories (DRAM). They are fabricated on the same silicon chip. But the SRAM occupies more area compared to DRAM as stated by international road map for semi-conductors (ITRS) [1]. SRAM stores the data using MOSFET's in the form of 0's and 1's. In Dynamic Random Access memory (DRAM) the data is stored in capacitor, so it requires refreshing data and SRAM does not require refreshing data. To increasing speed of SRAM, the threshold voltage MOSFET should be reduced. But there is a limitation in reducing the Threshold voltage (Vt). The change in the Vt leads to change in noise margin of the SRAM. The noise margin effects the technology and supply voltage scaling [1]- [3]. The design of low power SRAM results in better performances of the chip. Most of

the energy consumed due to the current leakage in high performance computing processors. An arrangement of SRAM cell structure is one of the foremost source for the leakages currents, because of large number of transistors will present. Because of this there will be a need of design of a low leakage SRAM cell [2]. This can be achieved by reducing the supply voltages (VDD), and the dynamic power will be decreased and the first order low powers will be decreased linearly and it is one of the possibility to achieve the low power SRAM cell [7]- [8].

This paper work planned as follows section 2 defines about existing models like stable SRAM, Single bit SRAM Cells operations are explained. section 3 describes proposed SRAM Model and section 4 describes simulation results of all the existing and proposed models and in section 5 conclusion and future scope discussed.

## 2. EXISTING MODELS:

There are diverse categories of SRAM cell are based on the sort of load used in the simple inverter of the flip flop cell. Here conventional CMOS

SRAM (6T) Cell, stable 8 transistors based SRAM cell and single bit SRAM cell are considered for implementation.

### CMOS SRAM (6T) Cell:

This Static RAM cell is made of 6-transistors, 1-NMOS & 1-PMOS transistor for every invertor,

in addition to two NMOS transistors associated with row line the design of six transistors based Static RAM is as shown in the Figure 1. Static RAM can be functioned in two modes of operations they are Read operation & write operation.

*Read Operation:*

From the Figure.1 initially both BL and BL' is 1 i.e. both bit-line (BL) and complement of bit-line (BL') are pre-charged. Let us assume to Q and Q' are 1 our task is to retrain at the end BL' and Q' to 1. When WL is high BL should be pulled down through N2 and N1 transistors. But at the same time as bit is pulled down node Q tends to raise [3]. Q is held low by N1 but raised by current flowing from N2 specifically the transistors N1 and N2 must be ratioed Such that the node Q remains below the switching threshold of P2 N3 invertor this is called read stability.

*Write Operation:*

For write operation assume Q=0 initially and we wish to hoard logic value '1' into the cell. BL is pre-charged to high and left floating. BL' is pulled low by a write driver on account of read stability constraint BL will be unable force Q to high through N2 and the cell must be written by forcing Q' to 0. When the cell is written by forcing Q'=0 through N4 then P2 opposes this flow. So P2 must be weaker than N4 so that Q' be pulled low enough. This constraint is called write ability [4].

***Stable 8T SRAM Cell:***

Static RAM cells are normally use to execute recollections that require brief conditions to touch the base after some time, little power scattering, and flexibility to basic situations. The scrambling of the transistor assessments to accomplish the higher rate execution has prompted to an advancement in the scattering of the overflow control in profound submicron Static RAM cells [6]. The six transistors based Static RAM (6-T SRAM) utilizes a gigantic unit and it is watched that the composite information is not at the ideal rational level when the cell is settled.
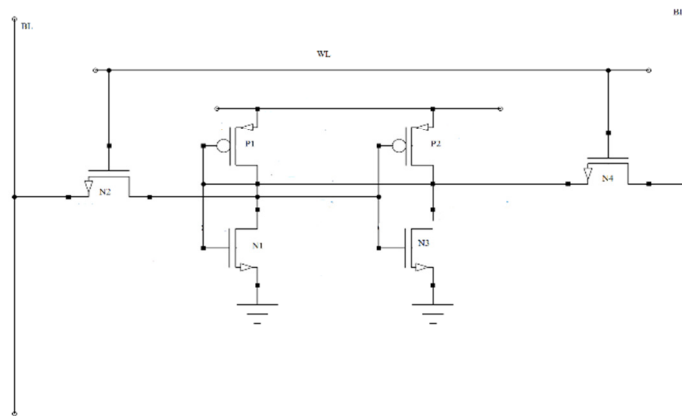


*Figure 1. 6T CMOS SRAM Cell.*

This capacity to keep up the information together with the abatement of the control of the spill and furthermore the dynamic constrain is examined more top to bottom in the present work. The immediate conclusion control SRAM cell is appeared in Fig. In element method, the word line WL = 1, SLP = 1 and SLPN = 0; Along these lines permit the cell to work easily. At the point where the cell does not augment, WL = 0, SLP = 0 and SLPN = 1. This impacts the NMOS and PMOS yield transistors, separating the quick way from the power supply to the ground cell. This outcome diminished the spill because of the pile impact. By the by, the flood through the trading transistor can accommodatingly affect the estimation of the information set away in the telephone in the midst of the standby mode, where (WL = 0) and both piece lines of the SRAM cell are preloaded An estimation of logic1 = 0.5V. Along these lines

Gated - control SRAM cell is less reliable, even with the system and environment arrangements; The social affair of charge in the BN focus point in the standby mode could in like manner realize the phone's state to be annihilated. By the by, the flood through the trading transistor can accommodatingly affect the estimation of the information set away in the telephone in the midst of the standby mode, where (WL = 0) and both piece lines of the SRAM cell are preloaded An estimation of logic 1 = 0.5V. Along these lines Gated - control SRAM cell is less reliable, even with the system and environment arrangements; The social affair of charge in the BN focus point in the standby mode could in like manner realize the phone's state to be annihilated. QAS-SRAM is introduced to conquer the issue of reduced quality [2]. The QPG-SRAM cell shown in Figure 3 uses a semi-electric structure to show the impact of the stack and the control is performed

using WL and an internal sign (B or BN). The semi-electric transistors M9 & M7 have WL as control information at the entryway line and can be completely terminated from the bit lines. The QPG-SRAM cell demonstrates good power hold control in the midst of the dynamic mode, in any case, it reduces the power inversion control in the midst of

the standby mode when it is showed up distinctively in connection to the close SRAM with VDD. In any case, the upkeep of method of reasoning 1 (0) is in a general sense improved when showed up distinctively in connection to both circuits passed.
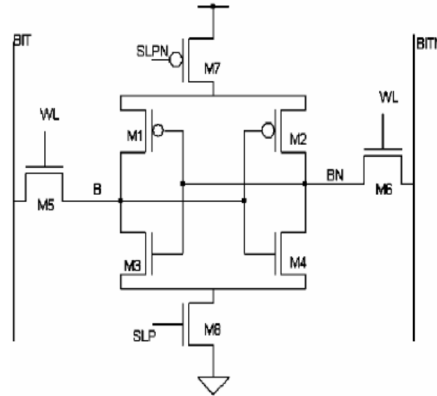


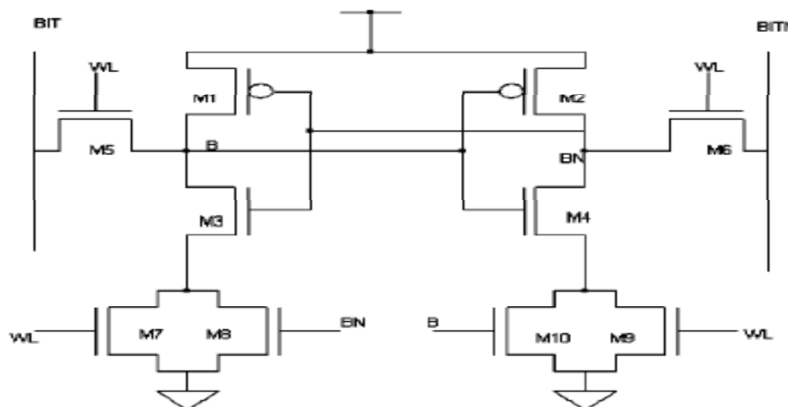*Figure 2. Stable 8T CMOS SRAM Cell.*



*Figure 3. QPG-SRAM cell for power saving*

With a particular true objective to achieve better essentialness save reserves dynamic & standby mode to handle strength issues, another, a stable low power Static RAM cell is planned. It involves two arrangements of transistors (NMOS and PMOS), one in the downstream method for the SRAM cell. The extra transistors (M7, M9) are obsessed by the symbol (BN) and B hubs, exclusively. The SRT 8T cell can be worked in two working methods: Active Method Operation and Standby Method Operation.

*Active Method Operation:*

In the write mode operation1, Word line hail WL = 1, bit line hails BIT = 1 and BITN = 0. The transistors M6 & M5 transmits BIT and BITN qualities to B & BN. Transistors M9 & M4 are ON. As a result of information, two transistors M9 &

M7 in the plunging method for the inverters, don't hamper in the composed operation. BN = 0 and B = 1 make transistor M2 be off, M1 to be on. B is along these lines kept up at 1. The releasing way given by the affiliation transistors M9 & M4 will push the BN hub to the method of reasoning regard 0. It is kept that the rationale esteem 1 enrolled in hub B is emptied in light of the fact that every one of the transistors M8, M3 and M7 are off, withdrawing the ground way. Subsequently the transistors M8, M3 & M7 are turned off; Due to the decrease in spillage streams. Along these lines, while creating reason 0, hub B = 0 and hub BN = 1; Some portion of hub B and BN is pivoted and essentialness dispersal is lessened. Since the WL = 1 hail sanctions its entryway line, the transistors M10 & M8 are incapacitated, in the midst of the

dynamic mode. This decreases the dynamic current through the cell by growing the impedance seen while creating.

*Standby Method Operation*

Out of gear mode, WL is Logic-0 and both get to transistors are debilitated by isolating bit lines in the Static RAM cell. Due to inside response, the status of the SRAM cell is held at a conventional sensible regard Logic-1 (Logic-0). The hub putting away rationale 1 is kept up at that incentive by the PMOS transistor driven by the lucid hub 0 and the hub putting away rationale 0 holds the impetus as a result of the mass discharge route gave by two related NMOS transistors in course of action. As far as possible spillage control in the faltering way is reduced by using the stack affect.

***Single Bit Line CMOS Static RAM Cell:***

The single-piece SRAM cell is constructed including two transistors, i.e. Read-Access-Transistor (MRA) and Read-Driver-Transistor (MRD), work self-sufficiently in the midst of the read operation.
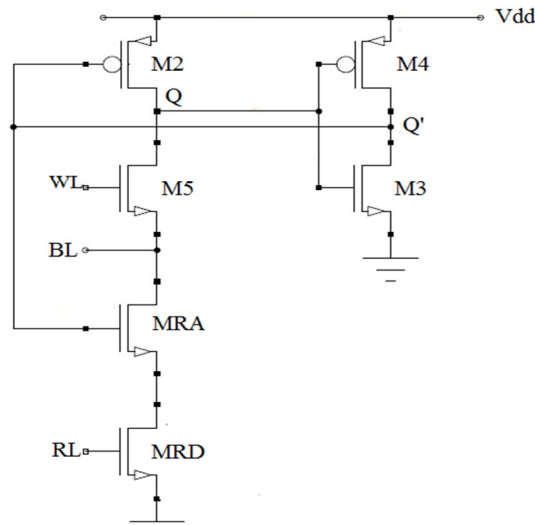


*Figure 4. Single bit Line CMOS SRAM Cell*

In the cell when Q = VDD, Q '= 0, both memory cells will be in their individual voltages. In any case, if Q = 0, Q '= VDD, Q is lessening as showed up in Figure 5, spillage current over M5 must be more noticeable than M2, to ensure that Q remains at 0. Providentially, Then NMOS (M5) is a more grounded stream controller than PMOS (M2), this condition is fulfilled and the single-piece SRAM can be worked in two techniques for operation which are write operation and read operation.

*Write Operation:*

The word line WL is stacked in VDD as in six transistors based Static RAM. Subsequently NMOS is a more grounded controller than PMOS, there is no issue shaping a 0 in the cell. The NMOS nonattendance of balance for the memory concentrator Q Gives you an opportunity to shape a 1 in the cell effortlessly. The formation of a 1 is finished by preloading the bit line (BL) to VDD. While shaping 0, bit line BL is freed and after that word line (WL) is stacked to VDD as in six transistors based Static RAM.

*Read Operation:*

As the situation of the recognition Q = 0; Before taking a gander at a quality from the breaking point focus focuses, the BL bit line is preloaded to VDD. The examining word line (RL) is then confirmed VDD. The point of confinement concentrator Q 'which supplies a logic value '1' is statically related with the MRA gateway, will deplete the loads on the bit line from MRD to GND as the RL is logic-1. This deduces that the line of bit has at present, when Q = 1, Q' will be 0 and MRA will be in expurgated and the bit line (BL) would not have the capacity to release from MRD to Gnd, and would read a logic-1.

## 3. PROPOSED MODEL

In this model, evacuate the power supply that is utilized to peruse and is supplanted by an inverter that is driven by the compose flag. The more prominent power dispersal is because of composing and perusing, with the goal that we pass the bit line to ground amid the read operation, hence diminishing the impact of the bit line on the circuit and in certainty lessening the power supply. The proposed new transistor SRAM cell 6 is manufactured including two read get to transistor (MRA) & MRD (Read Driver Transistor)

transistors that work openly amidst the read operation and will not impact the Cell SNM in any capacitance. The stun prerequisites of the cell coherence and the written work capacity set up the imperviousness to the changeability of a standard 6T cell. The set conditions are utilized for a similar stride input contraptions to peruse and create the cell, and it is unavoidable that the two conditions cannot be in the meantime progressed. Like firmly balanced drive supplies that confine the supplies for perusing and making, a Static RAM cell can likewise accomplish that by evolving itself. A composite procedure to an unselected fragment of a standard six transistors based Static RAM cell can bring about robustness matters when the word line begins while both work piece lines stay high; A tilting ailment as a read operation. These issues brought the blueprint of a few SRAM cell topologies to enhance data security and the utilization of spill power.

*Memory Cell Operation:*

When the put away information of the cell is 1 i.e. Qm=VDD and Qm'=0, then the two memory hubs will fill in as a circle at their separate voltages. In spite of the fact that the put away information of the cell is 0 (Qm=0, Qm'=VDD) ,Qm is above water. Spillage current in M2 transistor must be not as much as spillage current in M5 transistor to assurance Qm is in condition of rationale low. This condition is fulfilled on the grounds that ebb and flow driver of PMOS(M5) is lesser than NMOS(M2). The proposed single bit Static RAM can be functioned in methods of operations they are write operation and read operation.

*Write Operation:*

In instance of composing, the requested information to be composed will be given on bit-line and after that word line (WL) will be worked. For overwhelm the cell Strong pass transistor licenses bit-line. For compose 1 operation, bit-line ought to be in logic high i.e. VDD. For compose 0 operation, bit-line ought to be in the condition of logic "0" and afterward after word line must be charged to VDD.
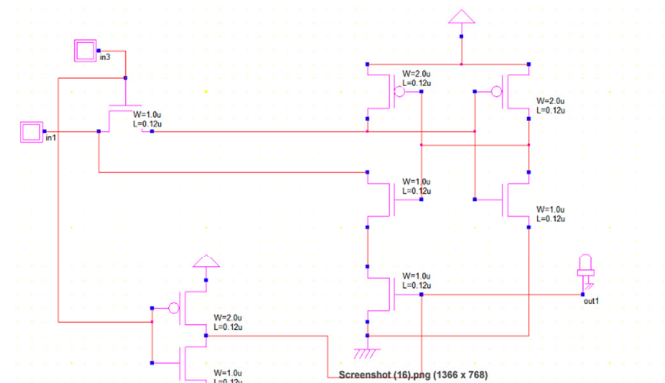


*Figure 5. Proposed Single Bit Line CMOS SRAM Cell*

*Read Operation:*

To perused the put away information from the cell, firstly bit-line ascends to logic '1'. RL is dynamic after the bit-line ascends to VDD. At the point when the bit-line is releasing or holding the put away charge, then we can decide the put away information of one-piece line multi-limit SRAM cell. On the off chance that bit-line goes low after ascents the read-line to VDD, it demonstrates one-piece line multi-edge SRAM cell put away the quality "0" in it. On the off chance that bit-line is holding the put away charge then in one-piece line multi-limit SRAM cell is putting away the value'1'. Consider that one-piece line multi-edge SRAM cell is firstly put away a quality "0" (Qm=0, Qm'=1). At the point when bit-line rises to VDD and RL is declared to VDD, MRA1, M7 and MRD1 transistors are on in light of the fact that RL is at rationale high. Presently bit line has approach to

deplete the charges to ground through MRA1, M7 and MRD1 transistors. So, tumbles down to logic "0" indicating put away information is '0'. Consider that one-piece line multi-edge SRAM cell is firstly put away a quality "1" (Qm=1, Qm'=0) when bit-line is ascending to VDD and RL is declared to VDD, MRA1 and M7 is off and MRD1 is on. MRD1 is on since read line is in VDD. MRA1 and M7 is off on the grounds that Qm'=0. Presently BL has no real way to deplete the charges to ground subsequently it read a '1'.

## 4.   RESULTS AND DISCUSSIONS

To implement these CMOS SRAM cells, DSCH tool can be considered to simulate the CMOS SRAM Cell. DSCH is a product for logic outline. In view of primitives, a progressive circuit can be manufactured and simulated. It moreover incorporates delay and power utilization

assessment. Here, 180nm node is considered for Microwind tool to draw layout for SRAM Cell. Microwind is a device for designing and simulating

circuits at design level. The post layout simulations can be seen as a waveform as shown in Figure 7.
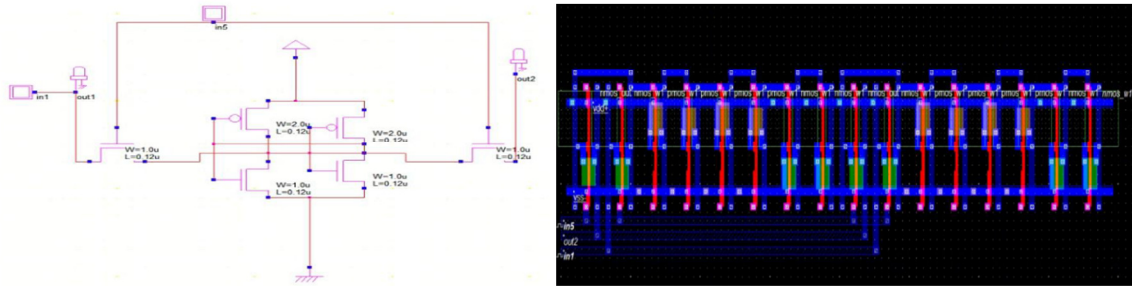


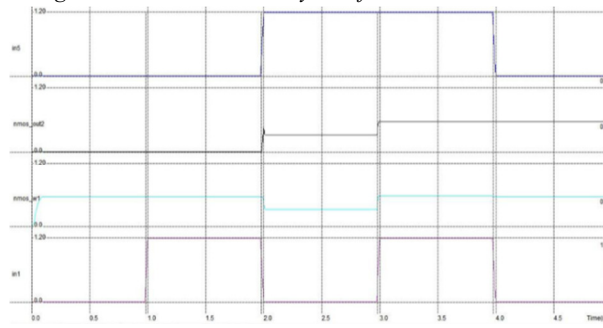*Figure 6. Schematic and Layout of CMOS 6T SRAM Cell*



*Figure 7. Simulation waveform of 6T CMOS Static RAM Cell*

### Stable 8T CMOS Static RAM Cell:

The stable 8T Static RAM Cell schematic is designed using DSCH tool and the layout drawn by using Microwind tool by considering 180nm

technology are shown in Figure 8. The post layout simulations are considered from Microwind tool and shown in Figure 9.
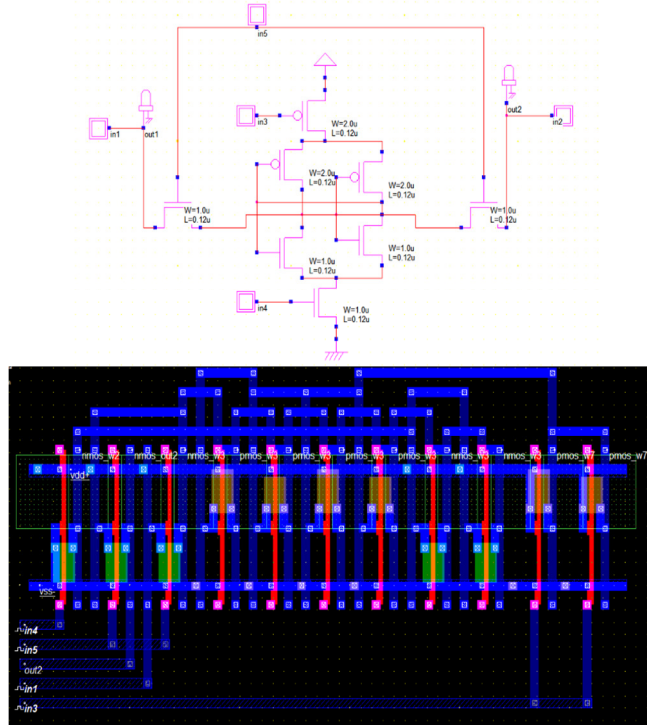


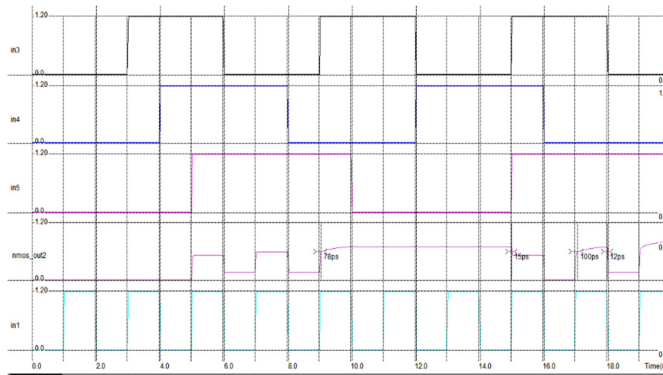*Figure 8. Schematic and Layout for Stable 8T CMOS SRAM Cell*

*Figure 9. Simulation waveforms of Stable 8T CMOS SRAM Cell*

***Single Bit Line CMOS SRAM Cell:***
The Single bit line SRAM Cell schematic is designed using DSCH tool and the layout drawn by using Microwind tool by considering 180nm technology are shown in Figure 10. The post layout simulations are considered from Microwind tool and shown in Figure 11.
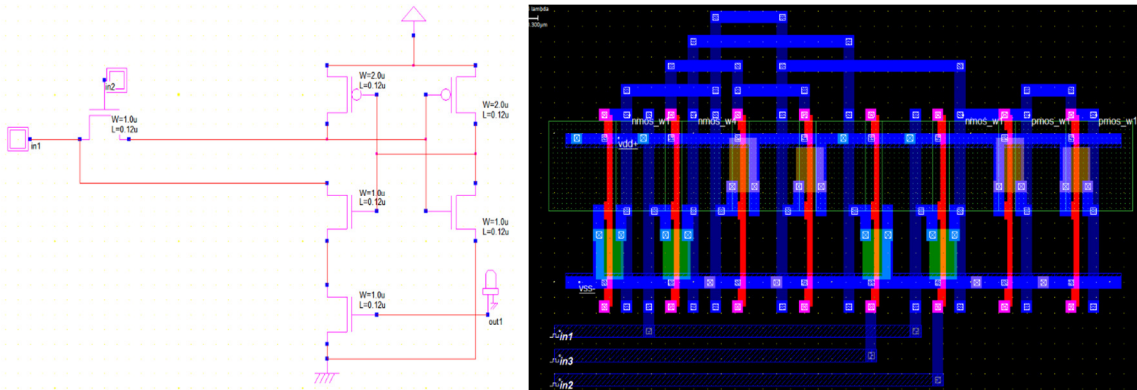


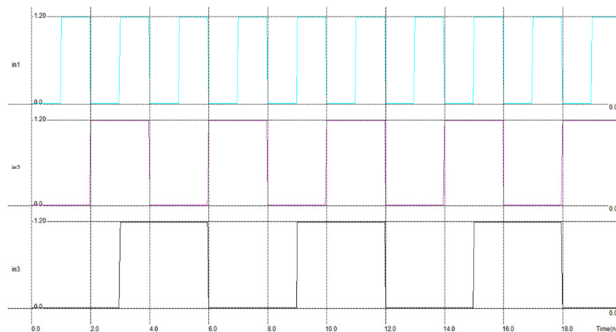*Figure 10. Schematic and Layout for Single Bit Line CMOS SRAM Cell*



*Figure 11. Simulation Waveforms for Single Bit Line CMOS Static RAM Cell*

***Proposed Single Bit Line SRAM Cell:***
The proposed Single bit line Static RAM Cell schematic is designed using DSCH tool and the layout drawn by using Microwind tool by considering 180nm technology are shown in Figure 12. The post layout simulations are considered from Microwind tool and shown in Figure 13. The results are regarding the comparison between the power consumptions of various SRAM cell structures and compare them with the conventional 6T SRAM Cell. There was an 84.6% of power consumption reduced for proposed model associated to CMOS 6T Static RAM cell, 75% power reduced when compared to CMOS 8T SRAM and 49.8% power consumption reduced when compared to 1-bit SRAM cell. All simulations were done using 180nm technology. As shown in the above table 1 the proposed model has less power consumption of 0.147mw. The tradeoff between all the SRAM

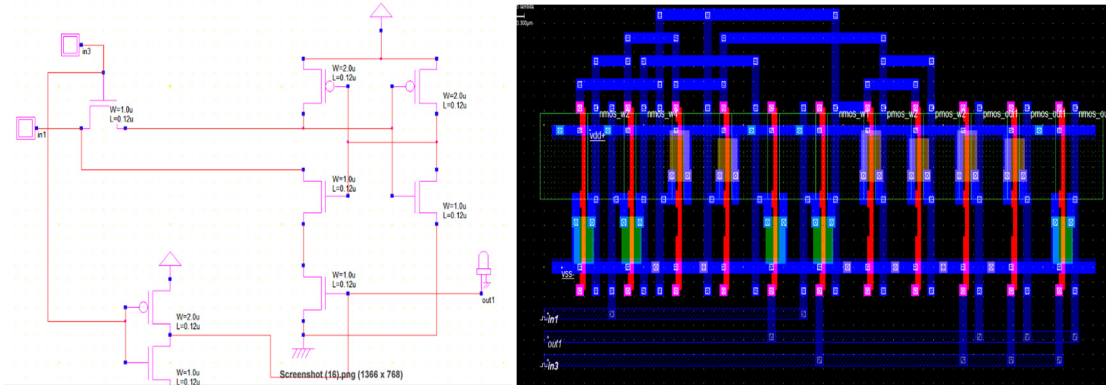Cells are explained by using the graph shown in Figure 14.



*Figure 12. Schematic and Layout for Proposed Single bit line CMOS Static RAM Cell*
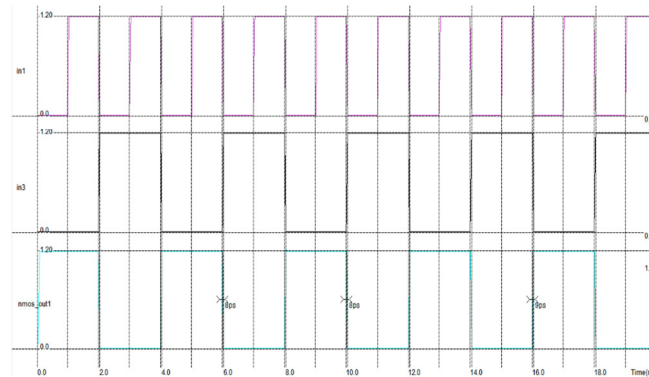


*Figure 13. Simulation waveforms for proposed single bit line CMOS Static RAM Cell*

*Table 1: Power Evaluation for different Static RAM Cells.*

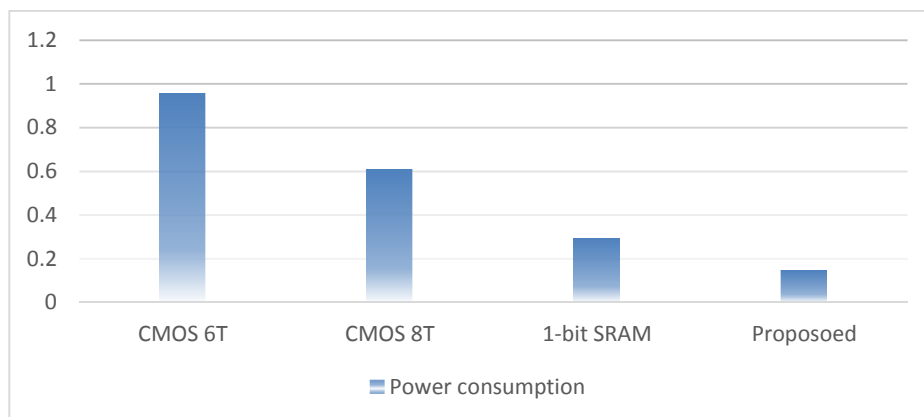| S.No | SRAM CELL | Power Consumption(mW) | Advantage |
|------|-----------|-----------------------|-----------|
| 1 | CMOS 6T SRAM | 0.956 | Conventional |
| 2 | CMOS 8T SRAM | 0.606 | Stable operation |
| 3 | Single bit SRAM | 0.293 | Less power comparatively |
| 4 | Proposed SRAM | 0.147 | Less power |



*Figure 14: Tradeoff graph between all SRAM Cells*

## 5. CONCLUSION

Proceeding with innovation scaling down puts a point of confinement on the amount of voltage supply can be scaled. Consequently, restricting the force utilization with new structures are the configuration prerequisites in late incorporated circuits. On account of SRAM, one apparently illogical methodology is to use just a solitary piece line without imperiling read security, which prompts the improvement of a Single Ended 6T-SRAM. In this work, single bit line SRAM implemented. The new SRAM working plan, proposed single bit line SRAM cell gives a huge force diminishment by lessening the measure of exchanging on bit lines. After comparing with all the Static RAM Cells, the proposed single bit line Static RAM Cell has better in the form of low power dissipation compared to other Cells and have stable operation in it.

## REFERENCES

[1] V.Subhamkari, G. S. Siva Kumar, " Low Power Single Bit line 6T SRAM Cell with High Read Stability", 2011 International Conference on Recent Trends in Information Systems.

[2] Nair P., Eratne S., John, E., "A Quasi Power Gated Low Leakage stable SRAM Cell," Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium.

[3] Jawar Singh, DhirajK.Pradhan et al," A single ended 6T SRAM cell design for ultra-low voltage applications",IEICE Electronic Express,2008,pp-750-755

[4] E. Seevinck et al., "Static-Noise Margin Analysis of MOS SRAM Cells," IEEE J. Solid-State Circuits, vol.SC-22, no.5 pp.748-754, Oct. 1987.

[5] H. Yamauchi, "A Discussion on SRAM Circuit Design Trend in Deeper Nanometer Scale Technologies," IEEE Trans. Very Large Scale Integr. Syst. vol.18, no.5, pp.763 774, May 2010.

[6] Benton H. Calhaun, Anantha P. Chandrakasan "Static Noise Margin Variation for Sub-threshold SRAM in 65 nm CMOS", IEEE Journal of Solid-State Circuits,, pp.1673-1679. vol.41,July 2006.

[7] Arandilla,C.D.C et al."Static Noise Margin of 6T SRAM Cell in 90nm CMOS" IEEE 13th International Conference on computer modeling and Simulation, pp.534-539,March 30,2011.

[8] Aly, R.E. Bayoumi, M.A., "Low-Power Cache Design Using 7T SRAM Cell" Circuits and Systems II: Express Briefs, IEEE Transactions, vol. 54 April 2007, Issue: 4, pp. 318-322

[9] Yen Chen,Gary Chen et al., "A 0.6V dual rail compiler SRAM design on 45nm CMOS technology with Adaptive SRAM power for lower Vdd_minVLSIs,Solid-State Circuits, IEEE Journal,vol. 44 ,April.2009, Issue 4 , pp.1209-1214

[10] L. Chang et al., "Stable SRAM cell design for the 32 nm node and beyond," in Symp. VLSI Technology Dig. Tech. Papers, Jun. 2005, pp. 128–129

[11] Damarla Paradhasaradhi, K. Satya Priya, K. Sabarish, P. Harish and G. V. Narasimharao "tudy and Analysis of CMOS Carry Look Ahead Adder with Leakage Power Reduction Approaches",Indian Journal of Science and Technology, Vol 9(17)

[12] Awais M. Kamboh, Matthew Raetz, Andrew Mason, Karim Oweiss, "Area-Power Efficient Lifting-Based DWT Hardware for Implantable Neuroprosthetics", *Circuits and Systems 2007. ISCAS 2007. IEEE International Symposium on*, pp. 2371-2374, 2007.

[13] W. Dehaene, S. Cosemans, A. Vignon, F. Catthoora, P. Geens, "Embedded SRAM design in deep deep submicron technologies", *Solid State Circuits Conference 2007. ESSCIRC 2007. 33rd European*, pp. 384-391, 2007, ISSN 1930-8833.

[14] Do Anh-Tuan, Kong Zhi-Hui, Yeo Kiat-Seng, "Hybrid-Mode SRAM Sense Amplifiers: New Approach on Transistor Sizing", *Circuits and Systems II: Express Briefs IEEE Transactions on*, vol. 55, pp. 986-990, 2008, ISSN 1549-7747.

[15] Hao-I Yang, Ssu-Yun Lai, Wei Hwang, "Low-power floating bitline 8-T SRAM design with write assistant circuits", *SOC Conference 2008 IEEE International*, pp. 239-242, 2008.

[16] Stefan Cosemans, Wim Dehaene, Francky Catthoor, "A Low-Power Embedded SRAM for Wireless Applications", *Solid-State Circuits IEEE Journal of*, vol. 42, pp. 1607-1617, 2007, ISSN 0018-9200.