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PERFORMANCE ANALYSIS OF THROUGH SILICON VIA'S (TSV's)

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ABSTRACT

At present, the 3-D IC integration utilizes Through Silicon Vias (TSV's) and it increased tremendous energy. The structure of the TSV composed of Cu, isolating liner and the silicon substrate. The isolating liner is encompassed signal TSV to stay away from signal leakage from TSV to the silicon substrate. In the conventional TSV structures, Sio2 is utilized as an isolating liner on account of its material compatibility with thesilicon substrate. To contrast to that several researchers had reported the issues of Sio2. Due to the high dielectric constant to such an extent that it brings about increasing of delay. Subsequently, Sio2 is not appropriate for elite applications. In this paper, we utilized polymer liner as isolating liner in place of Sio2. We simulated the performance analysis for both conventional and proposed TSV structures by varying radius and height of TSV. The proposed TSV structure simulation shows better results compared to conventional TSV structure.

Keywords: *Delay, Height, Power, Radius, Through-Silicon Via (TSV).*

1. INTRODUCTION

According to Moore's prediction, the number of transistors that are to be fabricated on a chip gets doubled for every eighteen months. Due to breakneck increase in thecount of transistors fabricated, the 2D IC integration is getting complicated. Subsequently, it becomes a hard nut to crack for the design engineers. To overwhelm this hectic task engineer's instigated 3D IC integration technology. [2]In the preface of 3D IC integration process wirebonds and flipchips are used for a certain time period and then replaced by TSV's which are considered to be the predominant method for interconnection[8]. In the semiconductor manufacturing sector, these TSV's have been the most expeditious developing technology and are used for multi-chip integration and packaging techniques [13].

TSV is a vertical electrical association [16] going totally through a silicon wafer.TSVs are a superior interconnect methods utilized as a contrasting option to wire-security and flip chips [18] [7] to make 3D bundles and 3D incorporated circuits, contrasted with options. Short pitch in between the signal TSV and ground TSV, crosstalk analysis [3] which causes achange in the delay becomes important. [1] In past, many approaches have been suggested for designing TSV's. TSVmodelinghas been suggested for a3D package of an IC. In the proposed model delay and powerconsumption have been reduced by varying the radius of a signal TSV and the height of TSV that is to be fabricated [21].

In this paper, a comparison of power and delay with the conventional and proposed circuits are being analyzed and the power delay product is obtained for both conventional and proposed circuits. TSVmodelingcontains asingle ground TSV and two signal TSV's. A ground TSV isplaced between two signal TSV's [5]. Ground TSVdoesnot have an oxide layer, it is made of metal which is surrounded by high depletion layerwhereas thesignal TSV also resembles the same as ground TSV but itcontains an oxide layer which is surrounded by high depletion region.The conventional and proposed

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models are simulated using T-Spice [21] [9] and comparison of performance analysis of TSVmodeling is done.

2. DESIGN METHODOLOGY

In 2D IC integration, fabrication is done in a horizontal manner[4] whereas, in 3D IC integration, fabrication is done in avertical manner where the usage of thearea is reduced. In fabricating a 3D IC and 2.5D IC[6] TSV are used. TSV's are the basic structures which act as an electrical connectivity between two dies which are placed on a silicon wafer. The basic conventional circuit which is proposed in [1]. In this circuit,the TSV's have two inductors and two resistors. The circuit is as in Fig 1. As the signal, TSV has an oxide layer so an oxide capacitance ($\mathbf{C_{oxide}}$) and a depletion layer so a depletion capacitance ($\mathbf{C_{depletion}}$) exists between the signal and ground TSV associated witha signalTSV.

There exists a contact resistance ($\mathbf{R_{contact}}$)

$$R_{contact} = \frac{\rho_C(N_a)}{2\pi r_0 h_{TSV}} \quad (1)$$

In the above equation i.e., to calculate contact resistance we should know $\mathbf{h_{TSV}}$(height of TSV). $\rho_C(N_a)$ is concentration of contact resistance which is a constant value [1].

$r_0$is the radius of doping region which is formed around the signal TSV [20].

The resistance for that region($\mathbf{R_{region}}$).To calculate $\mathbf{R_{region,}}\boldsymbol{\rho}$ isthe doping region resistivity constant

Where it can be given as$\boldsymbol{\rho = 1/\sigma_{region}}$and the doping region resistance can be calculated over the thickness of doping region [1].

$$R_{region} = \rho\frac{1}{s}$$

$$= \int_{r_0}^{r_0+t} \frac{\rho dr}{2\pi r h_{TSV}} = \frac{\rho}{2\pi h_{TSV}} \ln\frac{r_0+t}{r_0} \quad (2)$$

These two resistance'sconstitute as a total resistance acting across the ground TSV [1], that is by combining the equations (1) and (2).

$$R_{total} = R_{contact} + R_{region}$$

$$R_{Total} = \frac{1}{2\pi h_{TSV}} \ln\frac{r_0+t}{r_0}\frac{1}{\sigma_{eq}} \quad (3)$$

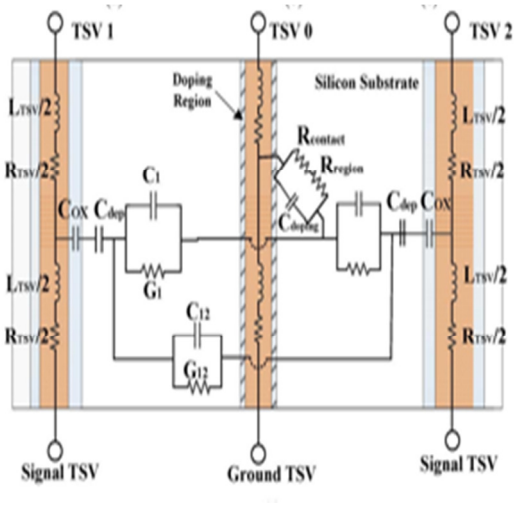

Fig 1: Structure of TSV

By equalizing the total resistance and summation of contact resistance and doping region resistance $\boldsymbol{\sigma_{eq}}$can be obtained as below [1].

$$\sigma_{eq} = \frac{\ln\left(1+\frac{t}{r_0}\right)}{\frac{\rho_C(N_a)}{r_0} + \frac{\ln\left(1+\frac{t}{r_0}\right)}{\sigma_{region}(N_a)}} \quad (4)$$

The conductivity depends on the concentration of doping which creates doping region, so the doping capacitance is required. It can be computed as

$$C_{doping} = \frac{\varepsilon_{Si} h_{TSV}}{\ln\left(1+\frac{t}{r_0}\right)} \quad (5)$$

Using transmission line model the resistance, capacitance and inductance parameters are calculated forTSV'sand silicon substrates.

$$L_{ij} = \begin{cases} \frac{\mu_0}{2\pi}\ln\left(\frac{l^2_{i0}}{R_i R_0}\right), (i=j) \\ \frac{\mu_0}{2\pi}\ln\left(\frac{l_{i0} l_{j0}}{R_0 l_{ij}}\right), (i \neq j) \end{cases} (i, j=1,2) \quad (6)$$

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Where $\mathbf{L_{ij}}$ is the inductance of TSV.$\boldsymbol{\mu_0}$ is the relative permeability of free space.

$\mathbf{l_{ij}}$ is the space between two TSV's. 0,1,2 are the number representations of TSV's. $\mathbf{l_{01}}$ is the distance between the first signal TSV and ground TSV. $\mathbf{l_{12}}$ is the distance between ground TSV and second signal TSV. $\mathbf{l_{02}}$ is the total distance between two signal TSV's.

Parasitic capacitance existsbetween both the signal and ground TSV [15] [14]. Coupling capacitance and resistance are between TSV's can be drawn out as follows.

$$C=\mu_0 \varepsilon_{Si} h_{TSV} L^{-1} \quad (7)$$

$$G=\mu_0 \sigma_{Si} h_{TSV} L^{-1} \quad (8)$$

Where $\boldsymbol{\varepsilon_{si}}$ and$\boldsymbol{\sigma_{Si}}$ are the constant's for dielectric material and conductivity of silicon substrate [1].

As the radius of tsv decreases the value of R_{tsv} that is the resistance of the signal tsv's and ground tsv'sare increased and with a decrease in L_{tsv} which is an inductance value of through silicon via's [17]. The oxide capacitance between signal and ground tsv remains constant. The capacitance of silicon decreases and the inverse of resistance decreases. Now considering the height as varying parameter the values are altered correspondingly as that are to be mentioned below.

The values for a conventional circuit are obtained with the help of mathematical computational software using the formulae which are required for comupting the values. And these values are substituted in the circuit and simulated using T Spice simulator.

The resistance of tsv decreases with adecrease in height and the inductance of tsv's are increased and the oxide layer capacitance, silicon layer capacitance increases. The inverse of resistance values decreases. The total resistance increases and the doping capacitance also increases for thedecrease in radius and height. As a result of the performance parameters delay and power decreases which contributes to the maximum reliability[12] and reduced noise margin which helps for proper transmission of data [19] [11].

3. RESULTS AND SIMULATIONS

In this module, we discuss the simulation results and observe the performance of the proposed model in [1]. The radius and height of the TSV's are varied accordingly and the effect of delay and power in the circuit is analyzed[10].

3.1. Simulation Analysis

Initially, the height of the TSV is kept constant assuming as 100 µm and the radius is varied from 20 µm to 10 µm and the change in delay and power is observed. Next, the radius of TSV is kept constant at 10 µm and the height of the TSV is varied from 100 µm to 50 µm and the variations in performance parameters are also observed.

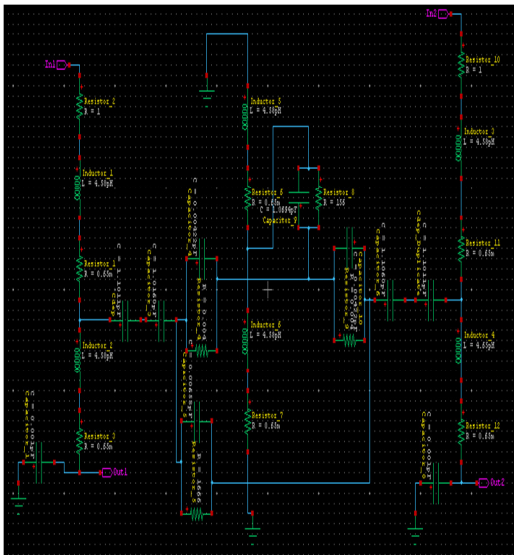

Fig2:Structure of TSV with radius 20 µm and height 100 µm

When the radiusand heightare 20 µm, 100 µm respectively, the values of inductors, capacitors and resistors are obtained and they are connected in the simulationenvironment as shown in Fig 2.

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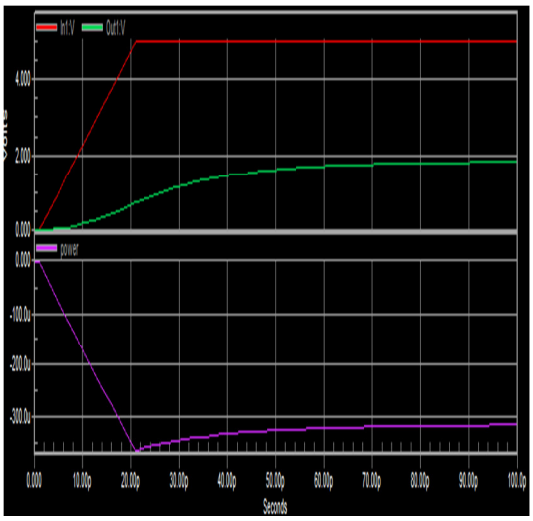

Fig3: Waveforms obtained when radius and height are 20 µm, 100 µm

By observing the waveforms obtained the input and output waves resemble the same with the difference in delay and power waveform is obtained as shown in Fig 3.

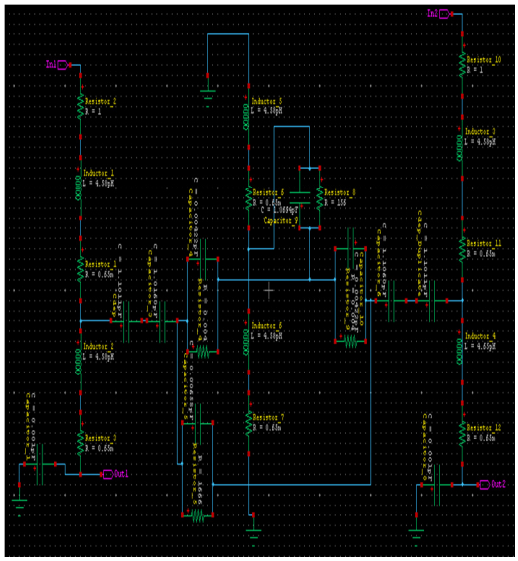

Fig4: Structure of TSV, when radius and height are 10 µm, 100 µm

When the radius is 10µm and heightare 100 µm the respective values of inductors, capacitors and resistance are obtained they are connected in the simulatingenvironment as shown in Fig 4.

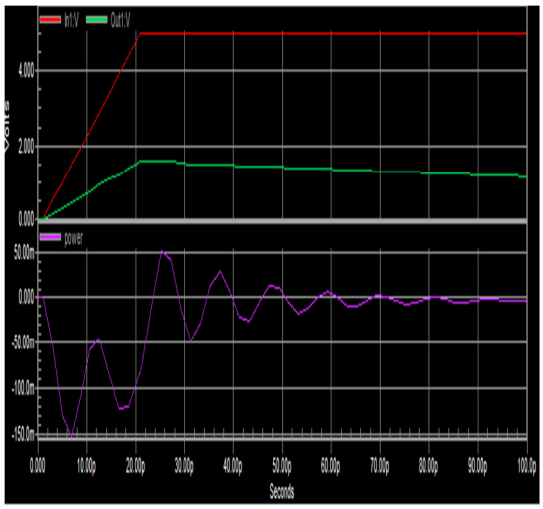

Fig5: Waveforms obtained when radius is 10µm and height100µm

By perceiving the waveforms obtained the input and output waves correspond to bealike with thedifference in delay and power waveform is obtained as shown in Fig5.

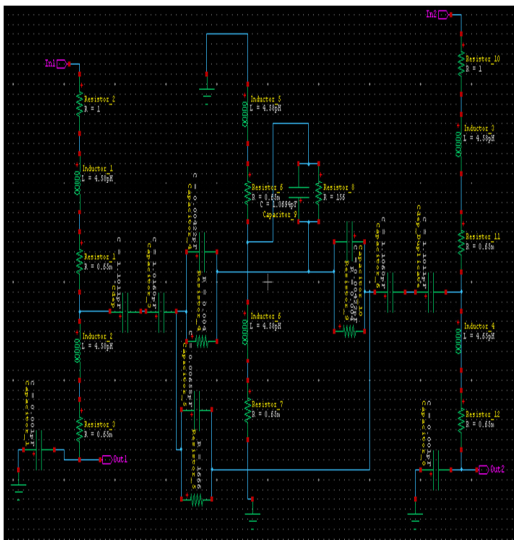

Fig6: Structure of TSV, when radius 10 µm and height 50 µm

When the radius is 10 µm and heightare 50 µm the respective values of inductors, capacitors and resistance are obtained they are connected in the simulatingenvironment as shown in Fig 6.

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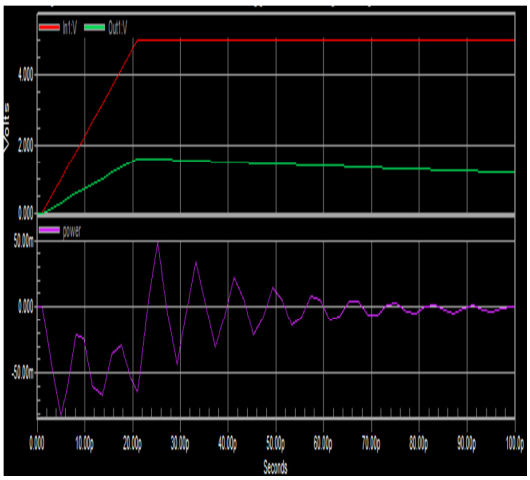

Fig7: Waveforms obtained when radius is 10 µm and height 50 µm

By observing the waveforms obtained the input and output waves bear a resemblance to the alike with thedifference in delay and power waveform is obtained as shown in Fig7.

3.2. Comparison Analysis

Table 1: Delay analysis for TSV Structure by varying radius

Delay when radius is varied		
Radius(m)	Height(m)	Delay(s)
20 µ	100 µ	14.1334p
10 µ	100 µ	04.6700p

Table 2: Power analysis for TSV Structure by varying radius

Power when radius is varied			
Radius(m)	Height(m)	Avg Power(W)	Max power(W)
20 µ	100 µ	1.4229e-4	1.8313e-3
10 µ	100 µ	5.9309e-3	5.3052e-1

Table 3: Power Delay Product analysis for TSV Structure by varying radius

Power Delay Product when radius is varied		
Radius(m)	Height(m)	PDP(Ws)
20 µ	100 µ	2.009e-15
10 µ	100 µ	2.769e-14

Table 4: Delay analysis for TSV Structure by varying height

Delay when height is varied		
Height(m)	Radius(m)	Delay(s)
100 µ	10 µ	04.6700p
50 µ	10 µ	04.2022p

Table 5: Power analysis for TSV Structure by varying radius

Power when Height is varied			
Height(m)	Radius(m)	Avg Power(W)	Max Power(W)
100 µ	10 µ	5.93079e-003	5.3052e-01
50 µ	10 µ	2.981777e-003	3.1865e-001

Table 6: Power Delay Product analysis for TSV Structure by varying radius

Power Delay Product when Height is varied		
Height(m)	Radius(m)	PDP(Ws)
100 µ	10 µ	2.769e-14
50 µ	10 µ	1.21515e-14

The execution parameters are compared and tabulated in tables 1-6. In this muniment, the parameters considered are delay, power and product of those two and these are compared using bar graphs. In the Fig 8, the similitude of two different radii for the parameters like delay, power and power delay product are plotted and represented.

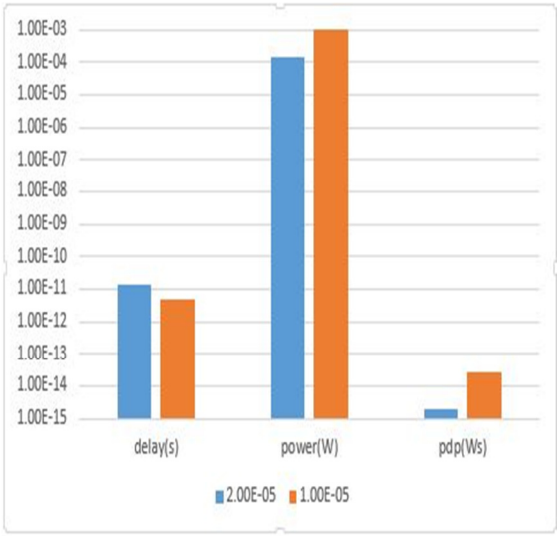

Fig 8: Comparison graph between parameters for different radius

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In the shownfig 8, 9, the similarities between the parameters (delay [11], power and power delay product) are observed for unlike values of heights.

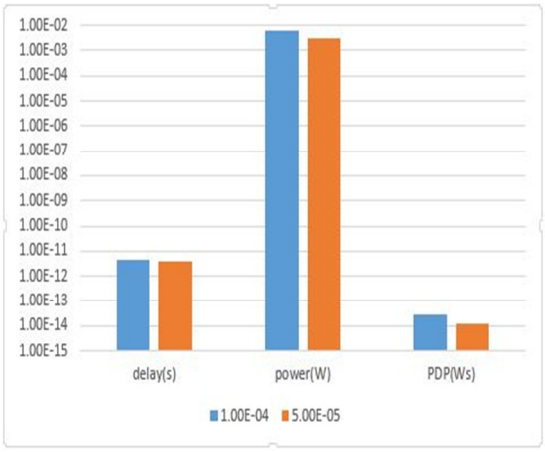

Fig 9: Comparison graph between parameters for different heights

The graphs in fig 8,9depict the information of different parameters for different radius and heights. The three different parameters are Delay, Power and PDP (Power delay Product).The first graph compares the parameters with the two different radii 20µ and 10µ denoted with two different colors blue and orange. The delay for radius 20µ is slightly above 10p in Y-axis and the delay for the radius 10µ is close to 10p which is slightly less to the radius 20µ.The power parameter for radius 20µ is at 100µ and for radius, 10µ reached the top 0.001 and is higher to 20µ and same with PDP, 20µ is lower compared to 10µ.

20µ is minutely above 1.00f radius and 10µ is above 0.01p which is half near to 1.00E-13. In the first graph, the radius 20µ is only higher in delays and less in other parameters. In the second graph, the y-axis has different heights and it also has three parameters same as the first graph and it is also a comparison between two different heights 100µ and 50µ.

The delays for both heights are almost same and a half near to 10p,100µ is negligibly higher to 50µ and power for 100µ height is very near to 0.01 and it is the highest and the other height 50µ is slightly less and a half near to 0.01. The PDP for 100µ is over 0.01p and for 50µ is 0.01p approximately. The height 100µ has the higher values for the given parameters.

3.3 Merits and Demerits

The merits of TSV(through Silicon Via) are it gives better performance in terms of electrical i.e., it consumes less power so the circuit has lower power consumption. Bandwidth is the bit-rate of amount of information consumed. There are types of bandwidth network bandwidth and data bandwidth. Network bandwidth is the rate of information shared on a network which is not necessary in this context. Where as coming to data bandwidth is the amount of data that can transmitted at a time. TSV's provide a wider data bandwidth where a large amount of data can be transmitted in single time. These also provide a very high density. It offers low cost when compared to another electrical connectivities and weighs in very small quantity.

The demerits of TSV's are discussed as follows. As the circuit becomes complex the cost of the circuit increases. TSV aspect ratio is low which reduces the difficulty in processing, have a high yeild rate and leads to short process time. In fabricating a TSV there are via first formation [2], via middle [2] and via-last [2] which reduces the fabrictaion damage. Problems caused with bump-less contact which can be avoided by providing a bump contact.

TSV's are mainly used in memory devices, processors and sensors. These are especially used in RAM (Read Only Memory) like SRAM, DRAM, flash memories and so on. Used in sensors like image sensors, are those sensors that convey information about the presence of image.

4. CONCLUSION

In this paper, the performance analysis of through-silicon via's are determined by diversifying the parameters of TSV. This can be accomplished by considering radius and height as the appreciable parameters of TSV'sand the upshot will be in the form of delay and power. As the radius and height are decreased there is a decrease in delay and power and vice versa. First, the values of delay and power are scrutinized at theradius (20µm and 10µm) with

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constant height (100µm). Subsequently, the values of delay and power are examined at height (100µm and 50µm) withconstant radius(10µm). The power-delay product is evaluated at appropriate values. These results are simulated using T-Spice.

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