Journal of Theoretical and Applied Information Technology
15th January 2017. Vol.95. No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

DESIGN OF LOW-POWER ADDER USING DOUBLE GATE & MTCMOS TECHNOLOGY

[1]K. PRIYANKA, [2] K. NEHRU, [3] S. RAMBABU, [4]NANDEESH KUMAR KUMARAVELU

[1]M.Tech Student, Department of ECE, Institute of Aeronautical Engineering, Hyderabad

[2]Professor, Department of ECE, Institute of Aeronautical Engineering, Hyderabad

[3]Assistant Professor, Department of ECE, Institute of Aeronautical Engineering, Hyderabad

[4]Research Scholar, Industrial Electronics Engineering, University of Rome, Italy

E-mail: [1]priyankakotrike@gmail.com, [2]nnehruk@gmail.com, [3] s.rambabu@iare.ac.in, [4]nandeeshforu@gmail.com

ABSTRACT

Low power, high speed Dynamic adders is widely used in Digital Logic Designs to overcome the leakage power and speed issues in static adders. Hence, by using MTCMOS Technology, low power dynamic MTCMOS 8-Bit full-adder cells have been proposed. Eight bit MTCMOS adder circuit has been designed using 45nm CMOS Technology. The static Adder circuit is modified by adding an NMOS transistor as a footer or tail to the circuit. This tail transistor when operates in sleep mode, it cuts off the path of current flow from Rail to Rail, which results in leakage power reduction. Hence, the proposed double-gate, MTCMOS Technology dynamic adders are significantly faster as compared to static CMOS logic designs in two aspects reduction of delay when tail transistor operates in normal mode and reduction of leakage power when tail transistor operates in sleep mode. Design analyses, and comparison results verify that the proposed circuits operate with high speed, obtains a significant reduction in leakage power due to the tail transistor included in the circuit. It is also observed that the power consumption of proposed dynamic adder is significantly less compared to existing static adders.

Keywords: *Dynamic Adders, MTCMOS, Sleep Transistor, Double Gate MOSFET, Ground Bouncing Noise*

1. INTRODUCTION

In the previous days, the VLSI designers were more bound towards the performance and area of the circuits. The cost and Reliability gained an important part whereas power consumption was a secondary consideration for them. In modern years, however, this has begun to vary rapidly and power has been given equitable importance in contrast to area and speed [1].

The adder is one of the foremost and necessary component of a processor and DSPs as a result of its utilization in ALU [3]. Increasing the demand of portable physical devices such as PDA, Mobile Phones, PC wants the employment of power economical circuits. The potency of ALU is about the efficiency of adder circuit. Many structures are designed to upgrade the performance of adder unit in terms of low power and high-speed and are very essential. As the count of the transistors gets increased on the chip leads to a dramatic increase in the power and area; performance betterment has been accompanied by a increase in power dissipation [2].

More number of transistors are utilized in the CMOS Static Logic circuits which in turn increases the power and also the die area. Except during the switching transients at every point each gate output is connected to Vdd or Vss via a low resistive path. Because of this the static power consumption is increased. This is overcome by using the dynamic logic circuits. Less number of transistors is required in the dynamic logic circuits which results in less die area utilization and also minimizes the delay, but due to the switching activity and clockload increments the dynamic power dissipation becomes high [3].

The major drawback of dynamic logic arises when the circuits are in cascaded form, i.e. cascading one gate to the next. During the stage 1 when the first gate is in precharge '1' state it may cause the second gate to discharge prematurely,

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

before the first gate of the first stage has reached its correct state. So, because of this it uses the "precharge" of the second gate. Until the next clock cycle this cannot be restored, hence there is no recovery for this error occurring. Hence, we can say that the power dissipation is even more for cascaded dynamic logic blocks [4].

To overcome this Domino Logic circuits came into existence. To evaluate any number of transistors these domino logic circuits are used, they are high speed circuits as they use a single clock to precharge the circuit. But these domino logic circuits after every stage require inversion [5]. While cascading NMOS and PMOS blocks they require a two phase clock signal. But because of this clock skew problem is raised.

In order to reduce this problem TSPC (True Single Phase Clock) logic is used which utilizes only single clock throughout the circuit. Hence a low power TSPC Domino logic adder cell has been designed, but this circuit resulted in sub-threshold leakage problem. To eradicate this drawback MTCMOS Domino Logic circuits has been implemented. These MTCMOS transistors reduce the power dissipation by minimizing the sub-threshold leakage current introduced in the domino logic circuits [6]. But this logic was not effective in terms of speed hence double gate technology came into existence, but this logic also resulted in lower speed and power issues hence a proposed method was given in this paper.

CMOS technology is widely used in all the digital circuits due to low power consumption. In a digital CMOS circuit, dynamic power dominates the total power dissipation. Reducing the supply voltage is the most effective approach to minimize the dynamic power dissipation. Hence, the leakage current acts as a major component of power; especially when the circuit is in idle mode. The major source of the leakage current is the sub-threshold leakage current, typically in the deep sub-micron technology. Lowering Vdd is also important in deep sub-micron (DSM) technologies to avoid reliability problems [7]-[8].

The supply voltages are scaled down as the technology is being scaled down to minimize the dynamic power consumption. However, reducing the supply voltage alone causes serious degradation in the circuit performances. One best way to maintain performance is to scale both Vdd (Supply Voltage) and Vth (Threshold Voltage). By reducing the Vdd (supply voltages), the Vth (threshold voltage) also needs to be scaled to keep the delay in acceptable limits. With the reduction in Vth there will be an exponential increase in the sub threshold leakage current, typically when the transistors are turned OFF and when the circuit is in idle mode.

Dynamic power is consumed when transistors are switching, as the technology continue to scale down, short circuits and leakage power becomes analogous to dynamic power dissipation. Due to the reduction of the threshold voltage leakage current is obtained in digital circuits. Hence, the identification and molding of various leakage and switching components is very essential for the estimation and reduction of power consumption especially for high speed low power application [1].

Dynamic logic circuits such as Domino and Domino Differential Cascade Voltage Switch Logic (DDCVS) have significantly worse tolerance to device sub threshold leakage compared to static CMOS. Hence, utilization of low threshold voltage (LVT) devices in order to improve the critical path delay makes the applications risky. A trade-off therefore exists between improving the gates reliability and enhancing its speed. Reducing the Vt increases the power dissipation and noise immunity of the circuits [8]. A new Domino logic style: High Speed Domino (HS-Domino) is therefore devised to resolve the speed-NM trade-off in domino circuits. It extends the domino's operation into the DSM regime, with no degradation to the gate's NM.

The leakage power contributes to the total power of the circuit in recent deep sub-micron technologies. Hence, leakage power minimization is a major issue for VLSI designers. Some devices like Memories and Laptops have a large idle period which has to be reduced. To minimize leakage power several techniques came into existence such as input vector control [9], Dual Vt Techniques, Multi Vt Techniques. The Dual Vt techniques are widely used in dynamic logic circuits. To minimize the leakage power Dual Vt technique includes low Vt transistor in critical path to minimize delay and high Vt transistors in non critical path to reduce the sub threshold leakage current [10].

In this Dual Vt technique the transistors which are ON during pre-charge have high Vt where as low Vt transistor is used in the evaluation block. Sub threshold leakage power is expected to dominate the total power consumption of a CMOS logic circuit. Energy efficient circuit techniques aimed at lowering leakage current are therefore highly desirable.

With the up gradation in technology, static power dominates dynamic power dissipation. In the

Journal of Theoretical and Applied Information Technology
15th January 2017. Vol.95. No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

present CMOS technology sub threshold leakage current is higher than other leakage current components [12]. In low power design, leakage power is considered as a great challenge. Many techniques have been proposed to limit leakage power. The two effective techniques to limit power consumption are Multi-threshold Voltage (MTCMOS) technique and voltage scaling technique [1]. A new Multi-Threshold (MTCMOS) scheme for dynamic logic styles is then presented. It is the most widely used technique in deep sub-micron digital circuits to reduce sub threshold leakage current when the circuit is in idle mode [11], [13] since they are highly effective.

Another way to implement MTCMOS technique is inserting a High Vt (HVT) device; called sleep transistor, in series to the normal Low Vt (LVT) circuitry. In this technique high Vt transistor PMOS or NMOS is inserted as a header or footer between the logical circuit (Low Vt) and the supply or ground rail. The sleep transistor is controlled by controllable signal use for active/standby mode control. When Sleep=1 i.e., when the sleep transistor is ON then the circuit operates in normal mode with high speed. When Sleep=0 i.e., when the sleep transistor is OFF the circuit operates in idle mode. This tends to minimization of leakage power significantly, with a slight delay [13].

MTCMOS has been suggested to reduce the leakage power by inserting high threshold sleep transistors to low-threshold circuitry [14]. It is an come up technology that provides high performance and low power operation by utilizing both high and low Vt transistors. These sleep transistors are enabled triggered using through sleep signals. In standby mode high threshold transistors are used as sleep transistors to reduce power consumption. To increase the performance in active mode low Vth transistors are utilized [12].

However, when the circuit transitions from sleep mode to active mode, large current flows through the sleep transistor, which leads to disturbances. Proper sleep transistor sizing is a key issue that affects the performance as well as the dynamic and leakage power of the entire circuit. The design cycle is usually short, but at the expense of a slight speed loss. The supply voltage can be minimized by using low Vth transistors to reduce switching power dissipation. Hence, MTCMOS logic can provide high speed and low power design without any area overhead [12].

In this paper new low power MTCMOS dynamic adder circuits are proposed which minimize leakage power. The proposed eight-bit adders are high speed circuits and also exhibit low leakage as compared to the conventional CMOS low-V_T static adder circuits. This paper is organized as follows. In section II, the existing conventional dynamic adders are discussed. Section III addresses the proposed dynamic adders in MTCMOS technique. In section IV the simulation results and comparisons are discussed. Section V concludes the paper.

2. EXISTING METHOD

A Full CMOS static logic avails more number of transistors which leads to larger silicon area. These faults are overcome with dynamic logic circuits. Dynamic logic requires few numbers of transistors and it minimizes the delay. Due to the increased clockload and switching activity dynamic logic leads to the increment of dynamic power dissipation.

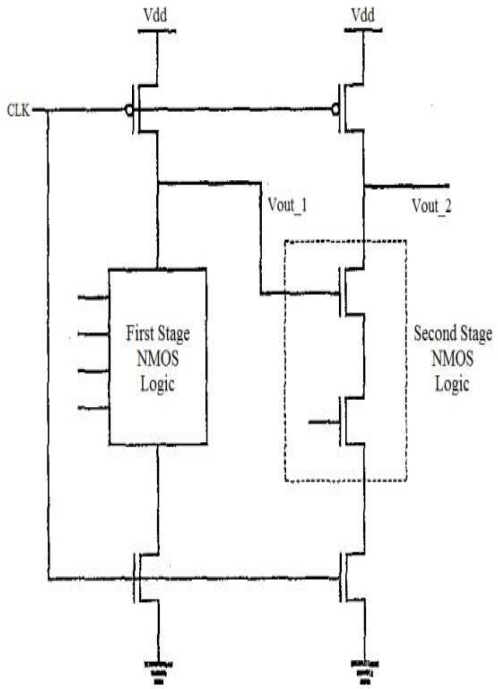

Figure 1: Cascaded Dynamic Logic Block

Dynamic circuits are directed by the clock signal. The output of the logic circuit is pre-charged high when the clock signal is logic 0 i.e. LOW. The logic gets evaluated when clock signal is logic 1 i.e. HIGH. The high speed circuits which can pre-charge and evaluate any number of transistors based on only one single clock are Domino Logic Circuits. But, after every stage the domino logic circuit requires inversion. By cascading PMOS and

Journal of Theoretical and Applied Information Technology
15th January 2017. Vol.95. No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

NMOS logic blocks pipelining operation can be done by using dynamic logic. But, while cascading PMOS and NMOS blocks a two phase clock signal is required for the domino logic. But, clock Skew rate problem is raised when a two phase clock is used. For reducing clock slew rate problem this TSPC logic is used. True Single Phase Clock logic uses a single phase clock signal throughout the circuit. Hence, Conventional Dynamic Adder has been designed whose schematic is shown in Figure 2 below.

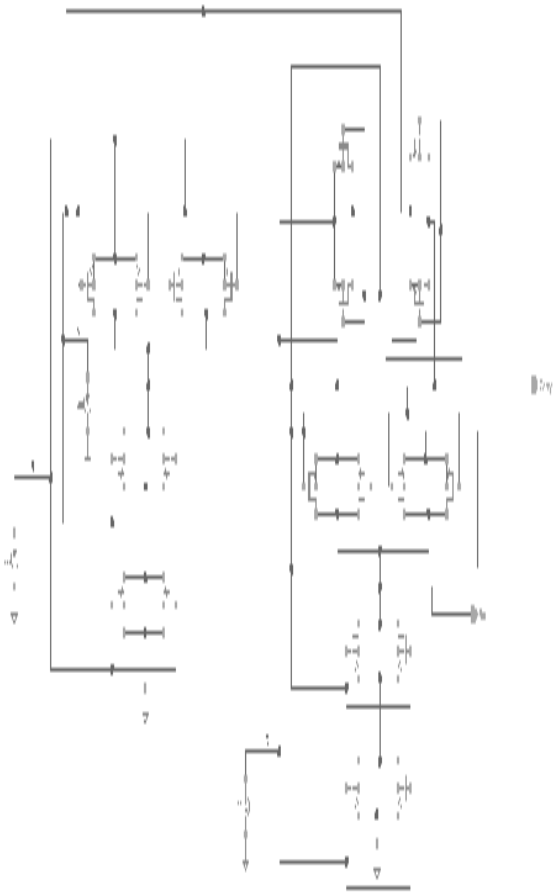

Figure 2: Schematic diagram of Existing Conventional Dynamic Adder

The schematic has been designed using 20 transistors for a single bit which gives reduction in silicon area. This circuit has been implemented in 45nm CMOS technology and the analysis for leakage power; delay and average power consumption are made. Using this single bit adder cell an 8-Bit Conventional Dynamic Adder has been designed; for this circuit also leakage power, delay and average power consumption is evaluated. Simulation results verify that the dynamic adders are efficient than the static adders in terms of delay and PDP reduction. But, the drawbacks in this existing Conventional Dynamic Adder are when the circuit is in idle mode, the static power dissipation is very high. This fault is overcome using the MTCMOS Technology; hence proposed method has been designed with MTCMOS technique included in conventional dynamic adder circuitry.

3. PROPOSED METHOD

The proposed method includes designing part of a single bit full adder circuit by using double gate MOSFET to improve the performance of the adder in terms of power and leakage current using 14 transistors. The double gate 14T Full adder circuit is shown in Figure 3.

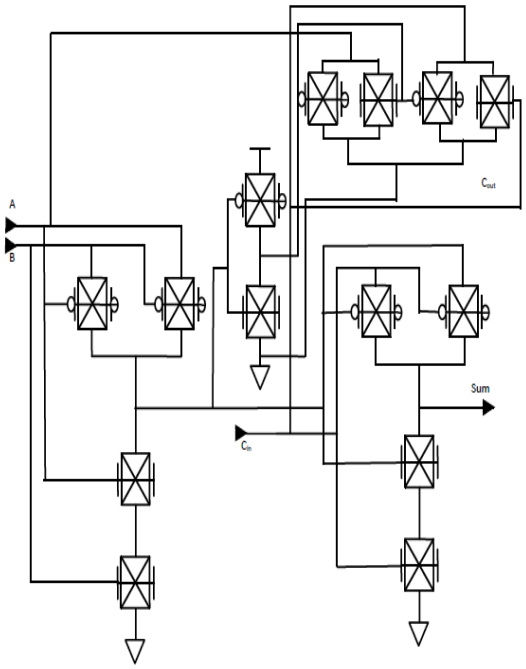

Figure 3: Double Gate 14T Full Adder

Using 4T XOR gate the cell is constructed. This cell is considered as the essential element of full adder cell since it helps in the generation of basic addition operation of adder cell. We used two 4T XOR gates in the 14T full adder circuit. For proper working of the circuit, conventionally XOR gate uses 8 MOSFETS, but at present we have different topologies to go with. To increase the circuit density here we have made use of 4T XOR gate. The main advantage obtained by using XOR gate is reduction in the size of full adder and also reduction in overall leakage current.

The basic advantage of the dynamic circuits is their speed, but at lower technologies

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

they exhibit significant leakage power. Now, for this a new low power MTCMOS dynamic adder has been proposed in this paper in 45nm CMOS technology to minimize leakage power i.e. for this double gate 14T full adder circuit the MTCMOS technique has been included; to limit the leakage power.

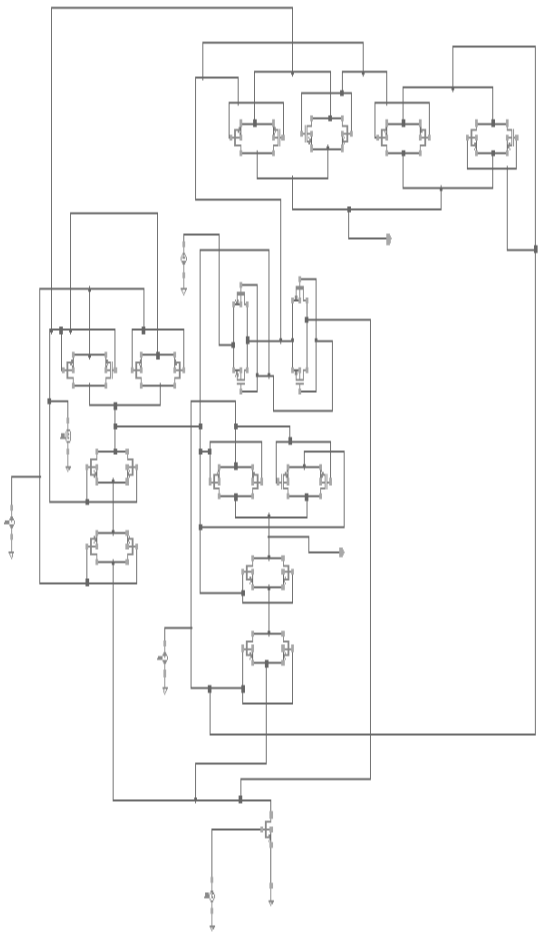

Figure 4: Schematic of Proposed Dynamic Adder using MTCMOS Technique

In this MTCMOS technique a high Vt sleep transistor is added as a header (PMOS) or footer (NMOS) to the circuit. Figure 4 shows the schematic of a proposed MTCMOS dynamic adder circuit with N-Type sleep transistor connected as footer between logic circuit and ground rail. The logic gate ground rails are connected to the virtual ground network; which has a slight high potential compared to real ground. And then, the virtual and real ground networks are linked by the sleep transistors.

Here M_tail signal is connected to sleep transistor depending on this M_Tail signal the circuit operates in two different modes: Normal or active mode, the sleep transistor comes to ON condition i.e. M_Tail sets to logic 1 HIGH, and the circuit functions normally i.e. the virtual ground almost functions as real ground. Due to this in the evaluation block the delay is minimized because of low Vt transistors. In this standby mode the sleep transistor is turned OFF i.e. M-Tail=0 logic LOW due to this the path between the supply and ground rail is cut-off which leads to the reduction of sub-threshold leakage current i.e. the leakage current is low which ultimately leads to the reduction of leakage power.

Hence, our proposed circuit has the dual advantage i.e. low leakage power in sleep mode and low delay in active mode. Using this single bit 8-bit proposed dynamic adder has been designed and their power consumption, delay and PDP calculations are made and compared with the Conventional Dynamic Adder circuit. Results verify that the proposed circuit is efficient than conventional dynamic adder in terms of both power, delay and as well as PDP.

However, when the circuit transitions take place i.e. when the circuit switches from sleep mode to active mode, noise is produced on the real ground line. This is named as ground bouncing noise. This is because, when the sleep transistor is set to logic 1 HIGH then large amount of current flows through it which leads to noise in the circuit. The ground bouncing noise can be limited by gradually increasing the rise delay of the M_Tail signal given to sleep transistor. This, is because if the M_Tail signal rises slowly, the sleep transistor turns ON gradually due to which the current through the sleep transistor passes in a wider time frame. This minimizes the ground bouncing noise to some extent in our proposed circuit.

Figure 5 and Figure 6 shows the schematic of 8-Bit Conventional Dynamic Adder and 8-bit proposed dynamic adder using MTCMOS logic. By using the single bit conventional dynamic adder circuit the 8-Bit conventional dynamic adder circuit has been designed similarly using single bit Proposed dynamic adder using MTCMOS logic circuit 8-bit proposed dynamic adder using MTCMOS logic circuit has been designed and the respective power and delay calculations are made in 45nm technology and they are compared and tabulated.

Journal of Theoretical and Applied Information Technology
15th January 2017. Vol.95. No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

Figure 5: Schematic diagram of Existing Conventional 8-bit Dynamic Adder

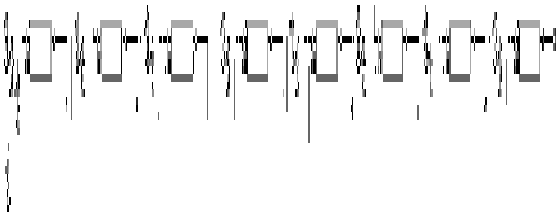

Figure 6: Schematic of Proposed 8-bit Dynamic Adder using MTCMOS Technique

4. TABLES AND FIGURES

Table 1: Performance Comparison

Technology	gpdk-45		
	Power (µW)	Delay (ns)	PDP (pJ)
Existing Single Bit Conventional Adder	166.7	17.89	2.982
Proposed Single Bit MTCMOS Dynamic Adder Using MTCMOS Technique	140.3	1.213	0.170
Existing 8-Bit Conventional Adder	1746	50.0	87.3
Proposed 8-Bit MTCMOS Dynamic Adder Using MTCMOS Technique	966.5	3.849	3.720

The power delay product is also known as energy which is the multiplication result of both power consumed and the delay time. After simulating the schematics using 45nm technology the power and delay values are calculated which is shown in the above Table 1. From the table we can say the power utilization and delay of single bit proposed MTCMOS dynamic adder are 140.3µW and 1.213ns which is 15.8% and 93.2% less than the existing single bit Conventional Adder; whereas the power utilized and delay for 8-Bit proposed MTCMOS Dynamic adder is 1746µW and 50.0ns which is 44.6% and 92.3% less than the existing circuit. Hence our proposed circuit is efficient both in terms of power and delay.

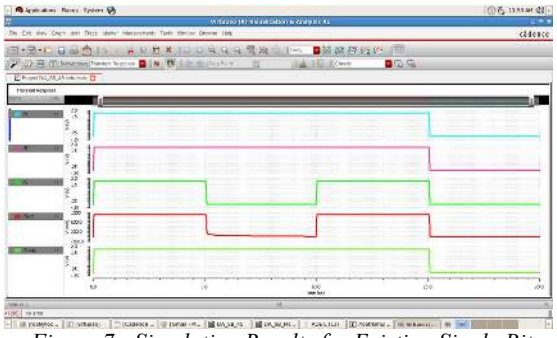

Figure 7: Simulation Results for Existing Single Bit Conventional Adder Schematic

Figure 7 shows the simulation result for existing single bit conventional adder circuit. Since, this is a full adder it has three inputs labeled as A, B, C and has two outputs labeled as Sum and Carry for one single bit. The operation is same as an adder i.e. when A=B=C=1, then the Sum=Carry=1.

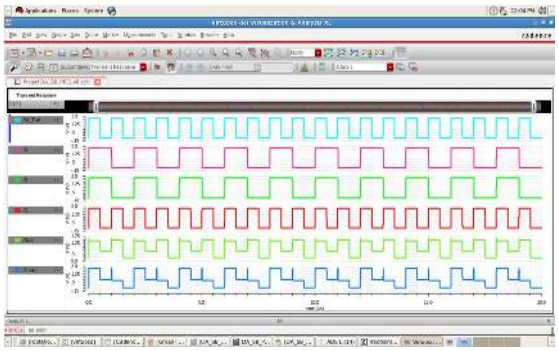

Figure 8: Simulation Results of Proposed Single Bit Dynamic Adder Using MTCMOS Technology Schematic

Figure 8 shows the executed waveforms for the Proposed MTCMOS Dynamic Adder circuit. This circuit is similar to conventional adder but includes one more input. Hence, the inputs for this circuit are M_Tail, A, B, C and the outputs are Sum and Carry for one single bit. The circuit is triggered only when the M_tail is in high condition i.e. when M_Tail is high the circuit acts as an full adder and results the output, when M_Tail is low then the circuit is in OFF condition resulting in almost logic 0 signal for Sum and carry.

Journal of Theoretical and Applied Information Technology
15th January 2017. Vol.95. No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

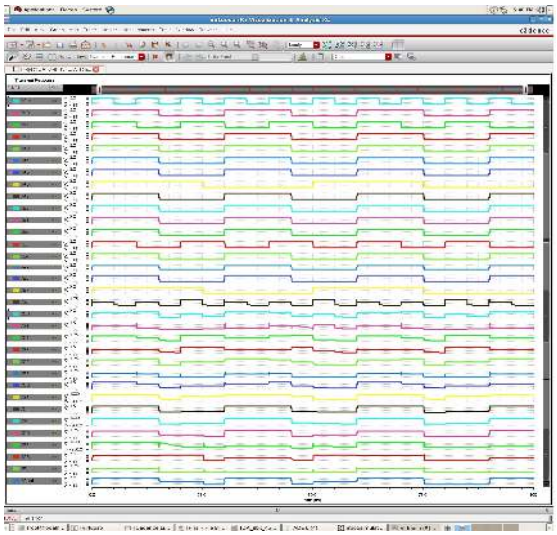

Figure 9: Simulation Results for Existing 8-Bit Dynamic Adder

Fig 9 shows the simulated result for the 8-Bit existing Conventional Adder circuit. Since it is an 8-Bit adder it has inputs labeled as Cin, input A (A0, A1, A2, A3, A4, A5, A6, A7) i.e. A [0:7] and input B (B0, B1, B2, B3, B4, B5, B6, B7) i.e. B [0:7], outputs Sum is labeled as S0,, S1, S2, S3 ,S4, S5, S6, S7 i.e. S [0:7] and Carry C0, C1, C2, C3, C4, C5, C6, Cout. For different combinations of inputs the outputs sum and Carry are obtained.

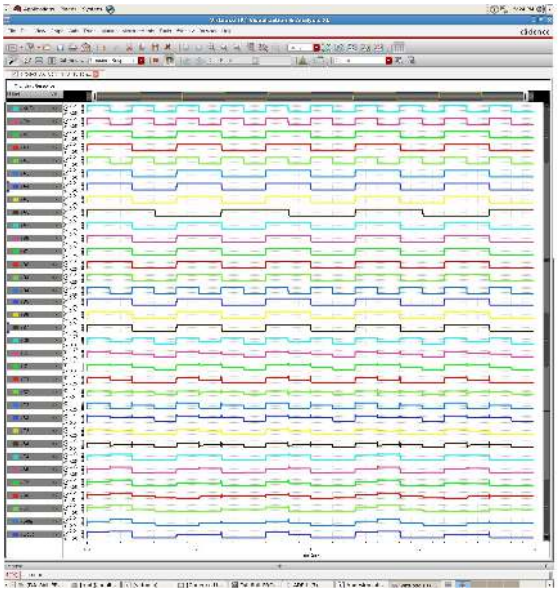

Figure 10: Simulation Results for Proposed 8-Bit Dynamic Adder

Figure 10 shows the simulated waveforms for 8-Bit Proposed MTCMOS Dynamic Adder. It has same inputs as conventional adder with another signal M_Tail included. When M_Tail is in logic 1 condition then the circuit acts as a full adder for different combinations of A [0:7] , B [0:7], Cin inputs and when M-Tail is in logic 0 condition then the circuit remains in OFF condition resulting in almost logic 0 signal for both Sum and Carry irrespective of the inputs.

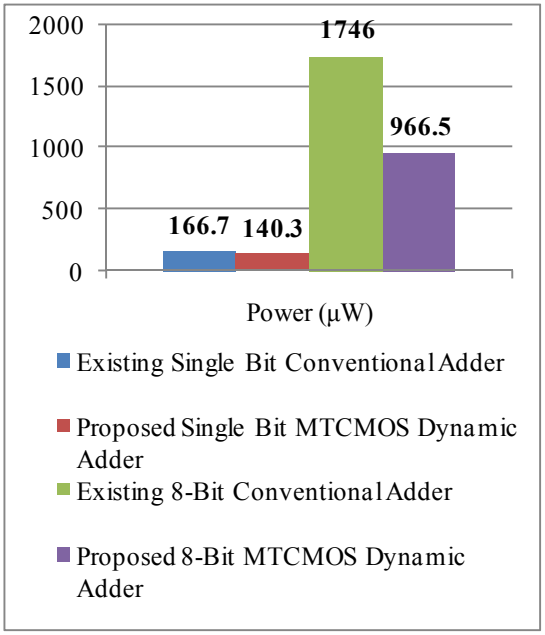

Figure 11: Comparative Analysis for power

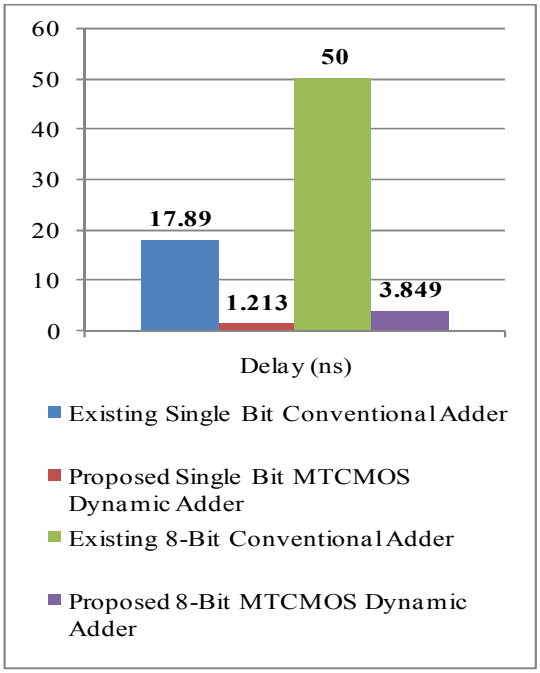

Figure 12: Comparative Analysis for delay

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

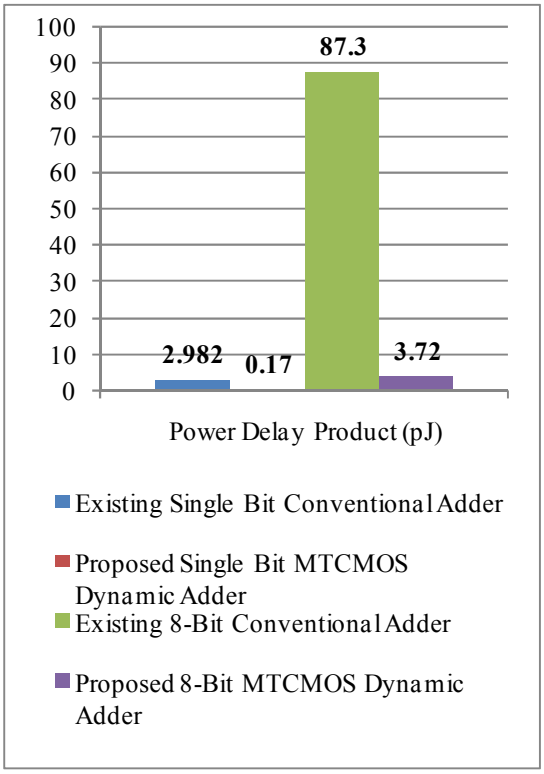

Figure 13: Comparative Analysis for power delay product

Using Cadence Virtuoso tool the proposed MTCMOS schematic has been executed in 45nm CMOS technology in which design analysis part includes Design Rule Checker (DRC) in Analog Design Editor (ADE) tool to find the effective performance of the proposed circuit. From this Power Consumption and delay results are obtained.

The obtained results of power and delay reduction for the existing circuit and the proposed system by using MTCMOS technology are shown in Figure 11 and Figure 12, and their respective PDP is shown in Figure 13. From the figure we can say that the proposed MTCMOS dynamic adder is effective both in terms of power and delay.

5. CONCLUSION

Both the existing system and proposed system are implemented using cadence virtuoso tool using 45nm CMOS technology. The design analysis part includes DRC in Analog Design Editor (ADE) tool. The maximum power and delay timing for single bit and 8-Bit Existing Conventional system are 166.7µW & 17.89ns and 140.3µW & 1.213ns respectively, whereas maximum power and delay timing for single bit and 8-Bit Proposed Dynamic adder using MTCMOS Technique are 1746µW & 50.0ns and 966.5µW & 3.849ns respectively. Hence, proposed system will ensure low static power consumption than conventional system. Hence, the proposed system can be extended for any number of bits depending on designer's requirement because the delay timing is being reduced for any number of bits.

Other than reducing leakage power the MTCMOS technique could be used for a different design goal. In MOS Current Mode Logic (MCML) the operating supply voltages can be reduced by using this MTCMOS technology. We can design a low power standard cell library for the adder circuit using this MTCMOS technology which can be standardized at logic levels; it includes a collection of components. This leads to even reduction in power since MTCMOS technique is used. These cells can be designed by varying the size of the sleep transistor to handle different loads and this can be used for minimum area, high speed applications.

A new approach can be made for sizing the sleep transistor which indeed leads to reduction of total width of the sleep transistor for a MTCMOS circuit by making an assumption of a cell used and also by the placement of the sleep transistor. This may result in minimizing the parasitic resistances of the virtual ground net; and also leads to leakage power reduction. By increasing the efficiency of packing currents into the sleep transistor more accurate results can be obtained. Future work should include the designing and fabrication of larger MTCMOS circuits using the newly designed and developed design flow techniques.

REFRENCES:

[1] Paanshul Dobriyal, Kurna Sharma, Manan Sethi and Geethanjali Sharm, "A High Performance D-Flipflop Design with Low Power Clocking System Using MTCMOS Technique", 3rd IEEE International Advance Computing Conference (IACC), 2013, pp. 1524-1528.

[2] Milind Gauthama, Shyam Akasha, "Reduction of Leakage Current and Power in Full Subtractor Using MTCMOS Technique", International Conference on Computer Communication and Informatics (ICCCI-2013), Jan 04-06, 2013.

[3] Rumi Rastogi, Sujata Pandey, "Implementing Low Power Dynamic Adders in MTCMOS Technology", IEEE Sponsered Second International Conference on Electronics and Communication System (ICECS 2015).

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

[4] Permendra Kr. Verma, S. K. Singh, Amit Kumar, Sanjay Singh, "Design and Analysis of Logic Gates Using Static and Domino Logic Technique", International Journal of Scientific & Technology Research Volume 1, Issue 5, June 2012, ISSN 2277-8616.

[5] MS. Rakhi R. Agarwal, Dr. S. A. Ladhake, "Systematic Design of High-Speed and Low-Power Domino Logic", International Journal of Advanced Research in Computer Science and Software Engineering Volume 2, Issue 3, March 2012 ISSN: 2277 128X.

[6] Senthil Sivakumar M, Arockia Jayadhas S, Arputharaj T, E. Ramkumar, "Design of MTCMOS Domino Logic for Ultra Low Power High Performance Ripple Carry Adder", International Journal of Emerging Trends in Engineering and Development Issue 3, Vol. 1 (January 2013) ISSN 2249-6149.

[7] Gielen, G. ; Dehaene, W. "Analog and Digital Circuit Design in 65 nm CMOS: end of the road?" IEEE Proceedings on Design, Automation and Test in Europe, 2005, Page(s): 37 – 42.

[8] M.W. Alam, M. H. Anis, and M. I. Elmasry, "High-Speed Dynamic Logic Styles for Scaled-Down CMOS and MTCMOS Technologies," Proceedings of third IEEE/ACM International Symposium on Low Power Electronics and Design, July 2000, Page(s): 145 – 160.

[9] V. Kursun and E. G. Friedman, "Node Voltage Dependent Subthreshold Leakage Current Characteristics of Dynamic Circuits," Proceedings of the IEEE/ACM International Symposium of Quality Electronic Design, pp. 104 – 109, March 2004.

[10] Song Yang ; Hong Wang ; Zhi-jia Yang "Low Leakage Dynamic Circuits with Dual Threshold Voltages and Dual Gate Oxide Thickness", Seventh International Conference on ASIC, 2007 ASICON-07, Page(s):70 – 73.

[11] Abdollahi, A. ; Fallah, F. ; Pedram, M. "Leakage Current Reduction in CMOS VLSI circuits by input vector control" IEEE Transactions on Very Large Scale Integration (VLSI) Systems,2004,Volume:12, Issue:2 Page(s): 140 – 154.

[12] V. Leela Rani, Dr. M. Madhavi Latha, "Design of MTCMOS Logic Circuit for Low Power Applications", V. Leela rani et al./ International Journal of Engineering Sciences and Technology (IJEST), ISSN: 0975 – 5462, Vol. 6, No. 7, July 2014.

[13] M. Anis, S. Areibi and M. Elmasry, Dynamic and Leakage Power Reduction in MTCMOS circuits using an automated efficient gate clustering technique", Proceedings of the 39th Design Automation conference, 2002, Page(s): 480 – 485.

[14] Qiang Zhou, Xin Zhao, Yici Cai*, Xi anlog Hong, "An MTCMOS Technology for Low-Power Physical Design", Integration, the VLSI Journal 42, 2009, Page(s):340 – 345.