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THE SPICE DYNAMIC BEHAVIOURAL ELECTROTHERMAL MODEL OF SILICON CARBIDE POWER MOSFET

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ABSTRACT

This paper presents an electro-thermal behavioral model (ETM) Silicon Carbide (SiC) Power MOSFET developed by SPICE. This model is based on the MOS level 1of SPICE model wherein the phenomena characteristic of the static and dynamic behavior which are dependent on self-heating and junction temperature are included and represented by ABM facilities (Analog Behavioral Models) of Spice.

The dynamic behavior of switching device associated with charge / discharge phenomena of the capacitances between its terminals is represented by 4 capacitances and two voltage controlled voltage sources (VCVS). The Cgs, Cgd and Cds capacitances vary according to the voltage to their terminals. And so, a good modeling of these capacitances yields up satisfactory results for the simulation of the switching.

The model parameters are extracted from manufacturers' data (data sheets curves) using polynomial interpolation with simulated annealing (SA) and weighted least squares (WLS) methods. This model takes into account the various important phenomena within the transistor. The effectiveness of the presented model has been proved by Spice simulation results for SiC MOS transistor C2M0025120D CREE (1200V, 90A).

Keywords: *SiC power MOSFET, Dynamic Electro-thermal Model, ABM Spice library, SPICE Behavioural, SiC MOS Model*

1. INTRODUCTION

The Silicon Carbide (SiC) is a wide band gap semiconductor material which has a good potential to replace silicon (Si) in many power switching. The former has several advantages over the latter including: High Speed Switching with Low Capacitances, high-blocking voltage [1], good heat performance in high temperatures [2, 3], high switching frequency (> 500 kHz) [4] and low on-state resistance R-on [5]. This enables it to effectively operate in harsh conditions such as automotive, aerospace and renewable energy domains [6]. However; despite all this, this material is characterized by some drawbacks with regard to the gate driver circuit requirements and availability of models suitable to different simulators, including SPICE.

SPICE simulator [7] (Simulation Program with Integrated Circuit Emphasis) is a well-known and widely used tool for analysing electronic circuits. Unfortunately, the MOSFET models integrated in SPICE (different levels) [8, 9] are formulated for isothermal low power MOS, while self-heating is not included in these models. Besides, these models are characterized by excessive complexity and by a large number of physical parameters which we cannot wholly control and which virtually require obtaining a proper identification for each component [10].

To contribute to the improvement of these models, I have introduced in this paper a flexible behavioural electrothermal model which is based on the Spice model MOS level 1. Indeed, we have already adequately studied the static behaviour [11-12], and this article is rather devoted to chart the dynamic behavioural model.

To help the power electronic circuit designers to realize their simulations under SPICE taking into account the heating effect. I propose this technique allowing to have the models of power SiC-MOSFET transistors.

To demonstrate the performance of this model and hence the significance of our contribution, I have worked on an example of the silicon carbide

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transistor (C2M0025120D CREE (1200V, 90A)) [13].

2. ANALOG BEHAVIORAL MACROMODELING TECHNIQUE

The physical investigation of a power device gives a set of integro-differential equations that describe device's static and dynamic behaviour. The challenge of the modelling ABM SPICE is how to present these equations and thus reduce the problems of convergence. Figure (Fig 1) shows the diagram of the principle of this modelling.

3. SPICE SIC ELECTROTHERMAL BEHAVIOURAL MOS MODEL

The behavioural electrothermal model of SiC MOS transistor is shown in figure (Fig.2); its static characteristics depending on the junction temperature are modelized by Spice ABM facilities, the static part modelling has been described well in LAKRIM works [11-12-14]. The dynamic behaviour is represented by four capacitances C1, C2, C3 and C6, and two voltage controlled voltage sources E1 and E2.

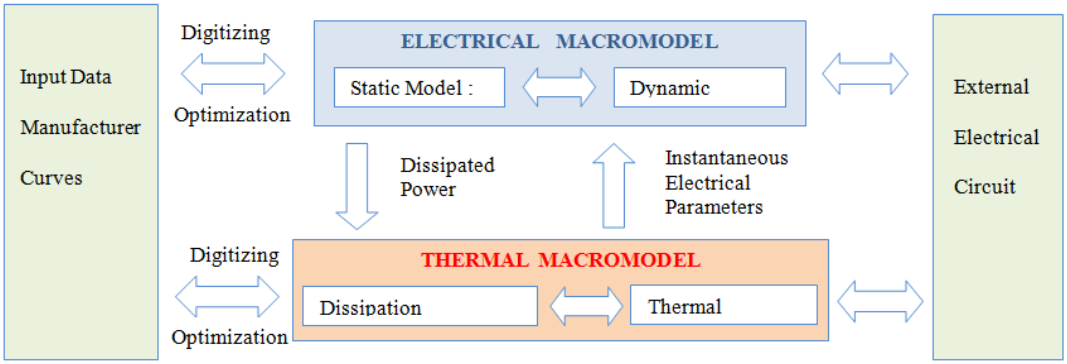

Figure 1: Diagram of an ABM macromodel of Power SiC MOS

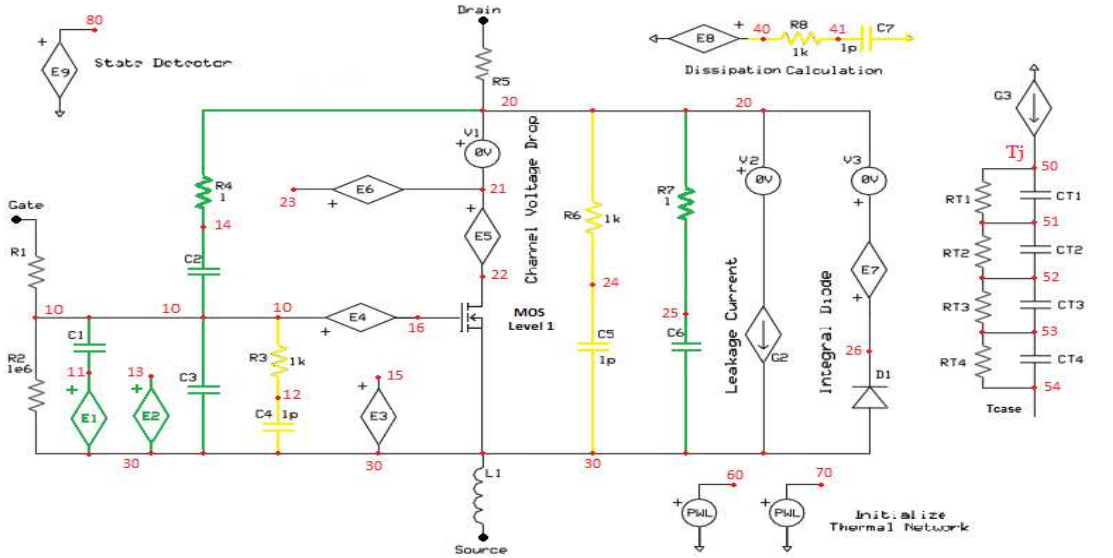

Figure 2: The Behavioural Electrothermal Model of SiC MOS transistor (the DC part Model is in black and the Dynamic part Model is in green)

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In switching the power SiC MOS acts as a power switch and the current I_D is controlled by the voltage V_{GS} (transfer characteristics). Its performance is defined by the time required to establish the voltage variations at the terminals of its physical capacitances within in the transistor which are composed of the gate oxide and the depletion layer as shown (Fig.3) [15].

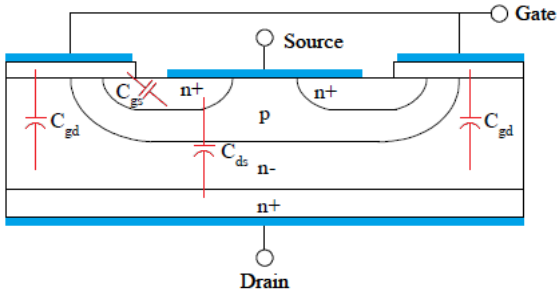

Figure 3 : Power MOSFET Structure Capacitances

These capacitances are independent of temperature [16] which is to say that the switching speed of the MOSFET remains unaffected by the temperature (except for a secondary effect related to the threshold voltage Vth which is bound up with the temperature variations).

3.1 : Input Capacitance – Ciss

Ciss is made up of the gate to drain capacitance CGD in parallel with the gate to source capacitance CGS as follows:

$$Ciss = C_{GD} + C_{GS} \qquad (1)$$

The input capacitance should be charged to the threshold voltage before the device starts switching on, and should be discharged to the plateau voltage before the device switches off. Thus, the impedance of the drive circuitry and Ciss have a direct impact on the switching on/off delays.

3.2 : Output Capacitance – Coss

Coss is made up of the drain to source capacitance Cds in parallel with the gate to drain capacitance Cgd as follows.

$$Coss = C_{DS} + C_{GD} \qquad (2)$$

For soft-switching applications, Coss is important because it can affect the resonance of the circuit.

3.3 : Reverse transfer Capacitance – Crss

The reverse transfer capacitance, also called the Miller capacitance, is one of the main parameters affecting the switching voltage rise and full times. This capacitance is equal to the gate-drain capacitance.

$$Crss = C_{GD} \qquad (3)$$

The figure below figure (Fig 4) shows the variation of these capacitances as V_{DS} for SiC MOS transistor C2M0025120D CREE.

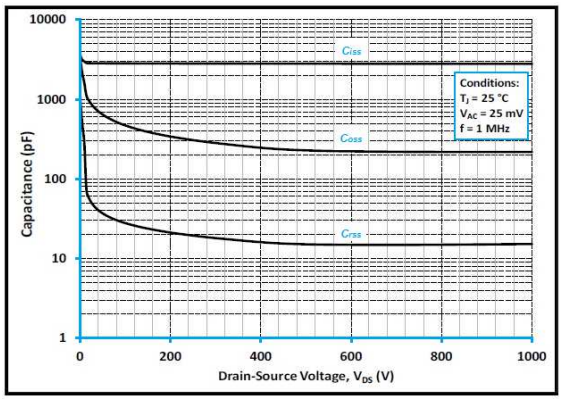

Figure 4 : Typical Capacitances vs V_{DS} (0-1000 V)

3.4 : Q_{GS}, Q_{GD}, and Q_G – Gate Charge

The gate charge values reflect the charge stored in the capacitances as described above. The gate charge is often used for gate driver circuit design because it takes into account the variations in capacitance with voltage variations during switching transient [17-18].

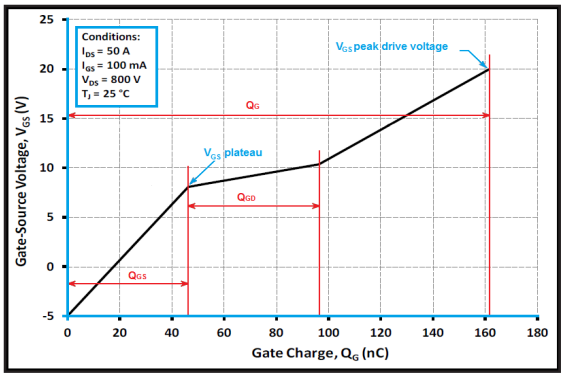

Figure 5. Typical Gate Charge Characteristic at 25°C

Referring to figure (Fig 5):

- Q_{GS} is the charge from the origin to the first inflection in the curve,

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- Q_{GD} is the charge from the first to second inflection in the curve (also known as the "Miller" charge).

- Q_G is the charge from the origin to the point on the curve at which V_{GS} equals a specified gate drive voltage.

- Gate charge values vary slightly with drain current and drain-source voltage but not with temperature. The plateau voltage V_{GS}(pl) shown in figure (Fig 5) is also directly proportional to the threshold voltage, so variation in threshold voltage correlates to variation in the plateau voltage.

3.5 : MOS capacitances turn-on switching Behaviour

For high voltage devices, the gate current is necessary to the charged or discharged the gate-drain capacitance C_{GD} during V_{DS} variations, since it makes the times of the rise and fall of V_{DS} highly dependent on the value of the gate current.

With an inductive load, the transistor current I_D remains essentially constant during switching. The analysis of current-voltage curves at the turning of six phases is presented below (Fig 6) [19] and illustrates the contribution of these capacitances to the switch.

- Phase 1: V_{GS} <0. The input capacitance Ciss is in maximum value.

- Phase 2: 0 <V_{GS} <Vth. The input capacitance Ciss decreases slightly.

- Phase 3: V_{GS}> Vth. Here the main $I_D(V_{GS})$ current increases to I0 switching current value.

- Phase 4: V_{GS}> Vth: In this phase V_{DS} drain voltage decreases rapidly because the reverse capacitance Crss is low. The main current I_D = I0 and the gate voltage VGS no longer changes.

- Phase 5: V_{GS}> Vth. In this phase responsiveness Crss increases, the input capacitance Ciss goes up again and the decrease in V_{DS} slows down while V_{GS} and I_D remain constant.

- Phase 6: V_{GS}> Vth. In this phase V_{DS} remarkably diminishes, and the device continuously progresses in the saturation zone of static characteristics. The V_{GS} voltage progresses again and the input capacitance Ciss reaches its maximum value (same as in Phase 1).

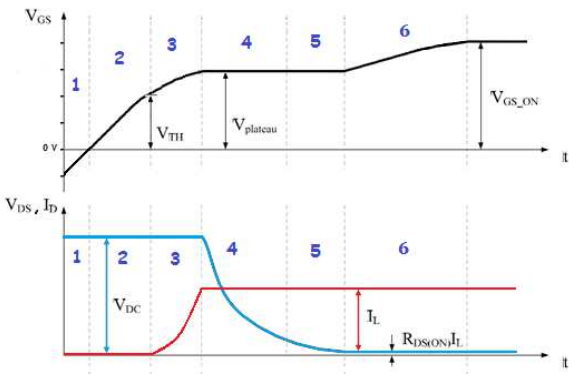

Figure 6. The current and voltage curves MOS turn-on phases

The most notable modification occurs to the C_{DG} capacitance because the V_{DG} voltage at its terminals varies within a greater range as that of across CGS terminals. For approximate calculation switching waveforms, C_{DG} is modelled by two discrete values C_{DG1} and C_{DG2}, as shown in figure (Fig 7) with some variation in value when V_{GS} = V_{DS} (which corresponds to the time when the MOSFET leaves or reaches the ohmic region). We assume that the C_{GS} capacitance is constant because the value of its variations during switching is much lower than that of the variations of the capacitance C_{DG}.

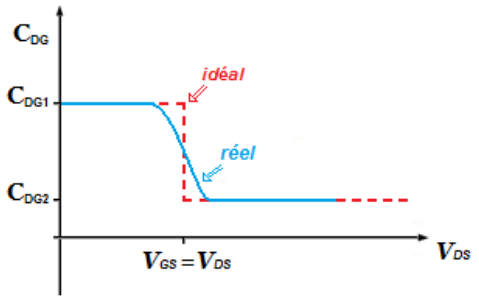

Figure 7. Capacitance C_{DG} variations vs V_{DS} Voltage (0-1000 V)

The proposed MOSFET model characterizing the dynamic capacitances is composed of four capacitors C1, C2, C3 and C6 and two voltage controlled voltage sources (VCVS) E1 and E2 (Fig 2). These components are defined below:

- C2 is the C_{GD} capacitance at the highest voltage V_{DS} value (for SiC MOS CMF20120D V_{DS} = 1000V (Fig 4)). It is the capacitance C_{DG2} in figure (Fig 7).

- C3 is the C_{GS} capacitance at the highest voltage V_{DS} value (for SiC MOS CMF20120D V_{DS} = 1000V. (Fig 4)).

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- C1 is the C_{GD} capacitance at zero V_{DS} voltage value (V_{DS}=0) (Fig 4). It is the capacitance C_{DG1} in figure (Fig 7).

- C6 is the capacitance C_{DS} (C_{DS}= Coss-Crss) at the highest voltage V_{DS} value.

- E2 is a voltage source controlled by the V_{DS} voltage variations (from 0V to V_{DS}max). The E2 output takes a ramp form (0V to 1V), so that when the E2 input equals 0V, its output equals 0V, and when its input equals V_{DS}max its output equals 1V.

- E1 is controlled by E2. It equals VGS where $V_{DS} \geq V_{DS}$max. Hence the C1capacitance has a zero voltage value at its terminals. And when V_{DS} falls below V_{DS}max, E1 value diminishes to zero voltage, so that the C1 capacitance is charged by the discharge of the C2 capacitance current until V_{DS} reaches its limit.

4. RESULTS

4.1 : Validation of the model by Spice simulation

To assess the accuracy of the proposed model described above, we performed simulations of SiC MOS C2M0025120D CREE (1200V, 90A) [13], by using OrCAD Spice 16.6 simulator. First, we start by MOSFET capacitances Ciss, Coss and Crss, because these parameters are of vital importance to the MOSFET as they determine the dynamic behavior of the device during switching transients. And after we present the switching waveforms for a cell switching (MOS-Diode) with a inductive load.

The measurement schematics of capacitance simulation circuits are described in [19], then their equivalent circuit simulations under OrCAD Spice are given by figure (Fig 8). The simulation results compared with manufacturer datasheet are shown in figure (Fig 9). In this figure we notice an almost perfect correspondence between the curves of manufacturer's data and the model data.

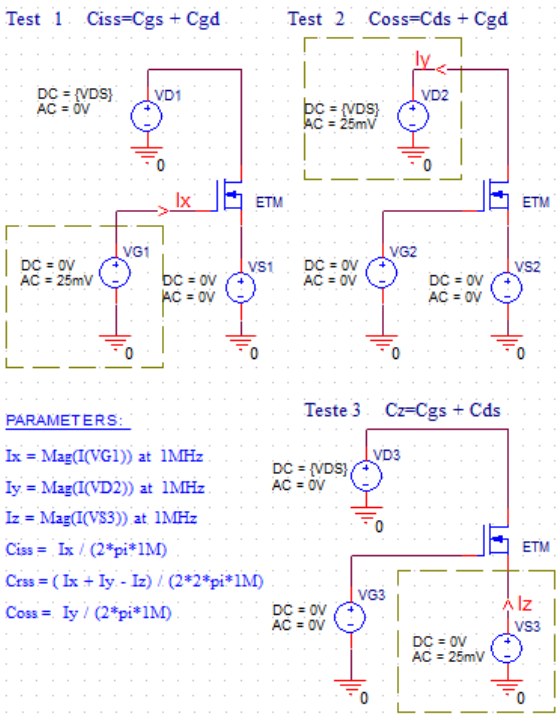

Figure.8: OrCAD Spice simulation circuits for MOSFET dynamic capacitances.

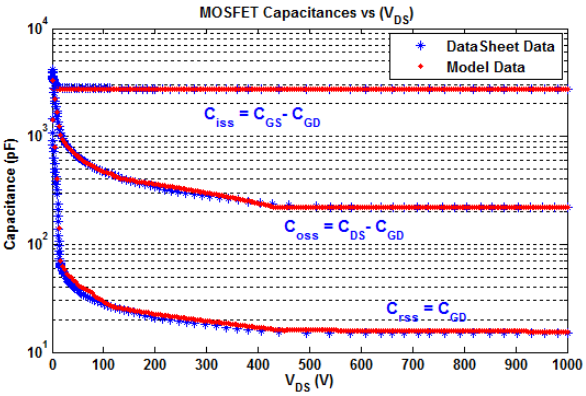

Figure.9: Curves of MOSFET dynamic capacitances Ciss, Coss and Crss, vs V_{DS}.

The simulation schematic with a inductive load is shown in figure (Fig 10):

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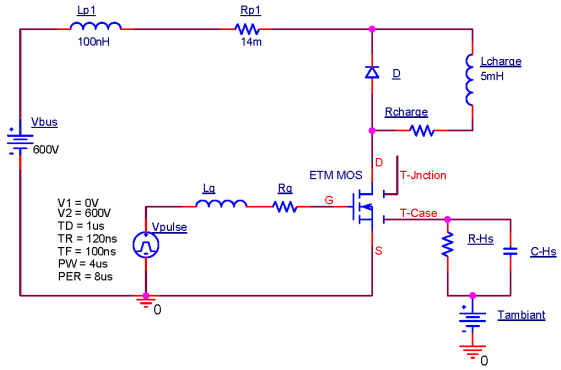

Figure.10: OrCAD Spice simulation schematic

The dynamic behaviour SiC MOS simulation in Turn-off and Turn-on Switching is shown in figure (Fig 11), from this curves we notice the six turn-on phases previously described in section 3, and we remark the I_D current overcoming at the turn-on, which is due to the inductive load behaviour.

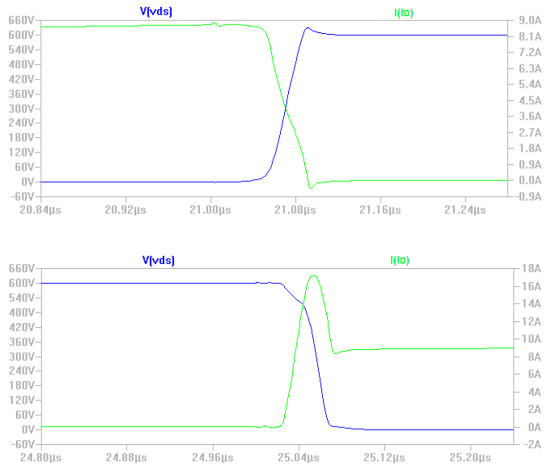

Figure 11. Voltage- Current Turn-off and Turn-on Switching Waveforms

5. CONCLUSION

In this article we dealt with the problem of modelling the MOSFET power. We proposed a behavioural model based on the electrothermal MOS model Level 1 of the SiC MOS transistor, and implemented it using a well-known simulator (SPICE).

The effectiveness of the model was verified by a simulation of SiC MOS C2M0025120D CREE (1200V, 90A) has yielded satisfactory results proved by the good agreement of the MOSFET capacitance curves (model and manufacturer data).

The basic advantage of the proposed model lies in its immanent simplicity and flexibility as to be implemented in modern simulators, adopting Spice programming.

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