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FPGA IMPLEMENTATION OF MIMO METAHEURISTIC MAXIMUM-LIKELIHOOD ALGORITHM HISD-ML

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ABSTRACT

In many wireless communication systems, the detection comes down to solving an optimization problem of a combinatorial system of the form y = Hx + w. In the general case, it's known that ML is "NP-Hard". In this paper, to solve this problem, a new algorithm called HISD suboptimal (hyperplane Intersection and Selection Detector) is proposed. This algorithm is based on a geometric approach. Compared with existing algorithms, the HISD has three very attractive features for implantation into real systems. The first relates to its performance in terms of BER which are close the optimum (ML) limit. Its complexity in terms of calculation is small and its structure is inherently parallel, which makes its hardware implementation easier. The puropose of our research is to develop a near optimal detector that performs a similar performance ML with a polynomial computational complexity. Indeed, we adopt an approach based on the methods of operational research in real time and especially meta-heuristics. Indeed, the developed method is composed of two complementary techniques: the intensification and diversification .In this paper, we propose a hardware implementation of the HISD algorithm in FPGA for MIMO (Multiple Input Multiple Output) systems.

Keywords: *MIMO, HISD, FPGA, ML, BER, SNR…*

1. INTRODUCTION

The increase in spectral efficiency remains one of the major challenges of digital wireless communication. MIMO systems transmissions constitute a solution to improve the transmission quality on difficult channels.

In recent years, an important trend in the metaheuristic field is that of integrating different components resulting in successful hybrid methods that attempt to better exploit the specific problem structure [1]. As a direct consequence of this, sometimes it is not clear how to name a specific heuristic as it uses ideas from several methods. In this regard, the first objective of our research is to develop a quasi-optimal detector near ML performance with polynomial computational complexity. It is important to know that in practice many modern meta-heuristic techniques provide high quality solutions, especially for ML detection problems as shown in [2].

The maximum likelihood ML detector has better performance in terms of bit error rate compared to other existing detectors but unfortunately it has exponential computational complexity [3]. Indeed, we adopt an approach based on the methods of operational research in real time and especially meta-heuristics. Indeed, the developed method is composed of two complementary techniques: the intensification and diversification. Intensification is a neighborhood search method. It is used to find the right solution to the detection problem, this technique has a weakness: it can be trapped in a very small local optimum. To overcome this weakness, effective diversification technique was required. Diversification is used to create a sub starting set which includes the right solutions to reduce the risk that the intensifying stage gives local minimum for all starting solutions. When transmitting with a MIMO system (Multiple Input Multiple Output) maximum speed

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transmitted is reached if emits each time a different symbol on each antenna. The number of symbols transmitted simultaneously is equal to the number N of transmitting antenna; it will be represented in the rest of the article by the vector of the baseband signal $\hat{x}$. Our studies present a new meta-heuristic method with quasi-optimal performance, limited complexity and affluent properties for hardware implementation (highly parallel structure). This paper describes the detection algorithm based on the meta-heuristic approach to detect the transmitted signal $x \in \xi = \{-1, 1\}^n$ of $y = Hx + W$, knowing the received vector y when $y \in R^m$ and the channel matrix $H \in R^{mxn}$. The algorithm has been specifically tailored to run on platforms (FPGA) with minimal computational hardware [4].

We start by describe the HISD approach, we explain in the second time the diversisification and intensisification phases. Thirdly, we present a compariasion between fifferents detectors studied: ML; ZF; MMSE and our HISD detector algorithm. In second step, we studied the complexity of each detector.

In this paper, a pipelined architecture for hardware HISD implementation is presented. Benchmark functions solved by FPGA hardware HISD implementations are compared with ML, ZF and MMSE detectors implementation. We start presenting the symbol detection in MIMO system using HISD method, in second time a FPGA implementation of HISD detectors for MIMO systems description will be detailed. Thirdly, a comparison of different detectors FPGA implementation must be elaborate. Finally, we discuss the performance results of FPGA based HISD implementation

2. HISD DESCRIPTION ALGORITHM

New techniques that advertise a more efficient use of spectrum have been proposed. Among these techniques we find transmissions Ultra Wide Band (UWB) transmissions or millimeter frequencies. Alongside these approaches, wireless telecommunication systems called MIMO (Multiple Input Multiple Output), are also contemplated. These systems are considered as a solution for improving the transmission quality on difficult channels. The MIMO transmission system with multiple antennas for transmission and reception is considered a very good candidate in many standards organizations. MIMO technology effectively meets the needs of future wireless communication networks as it allows increasing throughput while allowing a longer range

The HISD algorithm is one of sub-optimal methods like ML (Maximum Likelihood) which are developed to reduce the size ξ set of solutions selecting a ξ_{start} subset of points.

The HISD algorithm is a new ξ_{start} selection method.

It is about finding solutions near to the optimal solution using a geometric approach taken particularly original works of H. Artes, D. and F. Seethaler Hawatsch [5].

The HISD use an improvement of this approach associated with a process of optimization methodology that contains two complementary strategies [6]. The methodological approach HISD is to see the resolution of the decoding problem as a problem of Operational Research. Therefore, this algorithm consists of two phases, namely "intensification" and "diversification". Improved geometric approach concerns the possibility of calculating with real elements rather than complex, which greatly facilitated implementation of the algorithm. The diversification phase is to seek ξ_{start} all likely reach points in the intensification phase at the point corresponding to the optimum solution. The HIS algorithm uses two parameters that are managed in the diversification phase. The first D is the number of singular vectors obtained from the decomposition of the channel matrix H and the second C is the number of elements of ξ_{start} candidate's intensification phase [7].

3. DIVERSIFICATION PHASE

The diversification phase should allow around the optimal point to find ξ_{start} candidate's points. Those must be the least redundant as possible to cover a sufficient area containing the optimal point and the intensification phase eliminates the trap of local minima.

Let's suppose that the subset $\pi_1 \subset \zeta$ contains all starting points leading to the solution ML: $x \in \Pi_1 \Leftrightarrow x_{ML}$=greedy (x).T he function greedy () is the iterative function of intensification and Π is the set of points which converge to the optimal solution in the intensification phase.

The stage of diversification must give a subset therefore ζ_{start} who verifies $\zeta_{start} \cap \pi_1 \neq \varnothing$.

A geometric approach leads us to an efficient method to find ζ_{start}. In first time, we try to find best solution sub-optimal ρ_{ZF} like ZF or

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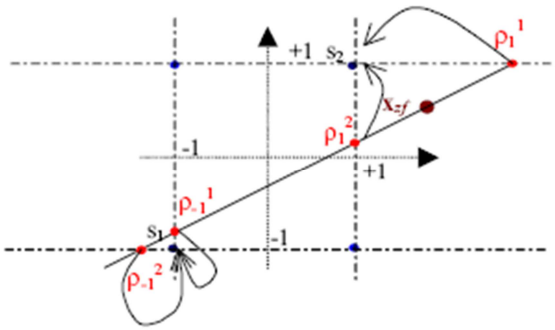
MMSE. Thereafter, the decomposition in singular value of the channel matrix H = UQVT is used knowing that the matrix diagonal Q contains the singular values $\{\lambda_k\}_{k=1...n}$ and the matrixes unit U and V contain, respectively, the singular vectors $\{u_k\}_{k=1...m}$ $\{v_k\}_{k=1...n}$.

We suppose that λ_k are classified in the increasing order ($\lambda_1 \leq \lambda_2 \leq .. \leq \lambda_n$). Let's note$\rho_{ZF} = H^+ y$ the solution under optimal generated by the ZF detector. For each point $x \in \xi$, $x - \rho_{ZF}$ is a vector from R^n expressed in the V basis like $x - \rho_{ZF} = \sum_{k=1}^{n} \alpha_k v_k$ where α_k are real coefficients. We can express the value of the function cost (objective function) to a feasible point:

$$f(x) = \|y - Hx\|^2 = \|H(x - \rho_{ZF}\|^2$$

(1)

We define $\Delta_k = \{z \in R^n / z = \rho_{ZF} + \gamma v_k , \gamma \in R\}$ like a straight in Rn passing by the point ρ_{ZF} and having like direction the vector singular v_k. The idea of the diversification phase is to choose the feasible points close to the straight Δ_1 ,.. , Δ_D to create a subset ζ_{start} containing the good starting points. We define $\xi = \{-3,+3\}^n$ Geometrically, this subset includes the apex of the hypercube unit of n dimension. The essential idea of this method is to find the points of intersection between Δ_k and the faces of the hypercube unit. For a straight Δ_k there are more 4n feasible points I_k c $\{-3,+3\}^n$ who represent the projection on $\{-3,+3\}^n$ of all intersection points between Δ_k define the following manner: P(i,s) = $\{z \in R^n / z(i) = s\}$, shown in figure1.



I. :

Figure .1: The first stages of diversification

Let's examine the intersection between Δ_k and the hyperplan P(i,s) = $\{z \in R^n / z(i) = s\}$.We obtain:

$\rho_{ZF}(i) + \gamma_k^{s,i} v_k(i) = s$

This intersection includes two cases:

If $v_k(i) \neq 0$ ➔ $\gamma_k^{s,i} = \frac{s - \rho_{ZF}(i)}{v_k(i)}$ then the generated point is $\beta_k^{s,i} = \gamma_k^{s,i} v_k + \rho_{ZF,}$ The returned point is $\beta_k^{-s,i}$, If vk(i) = 0 ➔ le point retourné $\beta_k^{-s,i} = \hat{x}_{ZF}$. So $I_k = \{\beta_k^{-s,i}\}_{i=1....n}^{s=-1,1}$ contains to the more 4n distinct feasible points. The subset of beginning of the intensification stage is defined by $\xi_{start} = \cup_{k=1}^{D} \xi_k$ where $\xi k \subset I_k$ contains the best C dawned of I_k. We contend that repair diversification is useful in various practical situations [8].

4. INTENSIFICATION PHASE

For each step K the best solution x^{k+1} is chosen in the neighborhood $N_Q(x^k)$ of the solution x^k. The neighborhood of x^k is a subset of ψ and can be defined of the following manner: The Q neighborhood of a point $x^0 \in \psi$ is the subset $N_Q(x^0) = \{x, d_H(x, x^0) \leq Q\}$ where $d_H(.)$ is the hamming distance. For each $x \in N_Q(x^0)$, x^0 and x defer themselves by in the more Q composing. . The total number of vectors in $N_Q(x^0)$ est $|N_Q(x^0)| = \sum_{i=1}^{Q} \binom{n}{i}$. The greedy methods give a solution to $f(x^k) \leq f(x)$ $\forall x \in N_Q(x^k)$. As shown in the fig 2, Q = 1 defines the points bound to x^0 by a side of a cube of n dimension, while for Q = 2 it defines the points that spread on the same face of the cube like x^0 [9].

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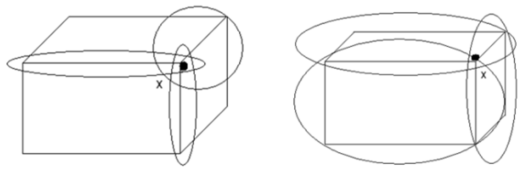
We intend to achieve an appropriate trade-off between intensification and diversification with the aim of being able to effectively sample the solution space, which is a basic principle for designing efficient metaheuristics [10].



Q=1

Q=2

Figure. 2: Representation of the neighborhood of the x point for Q = 1 and 2

5. DESCRIPTION OF HISD ALGORITHM

The HISD algorithm depends on two parameters that D are the number of clean vectors and C that represent the number of the best candidates. A hardware component is defined by its inputs, outputs, parameters and actual treatment. We cut into 2 parts the processing operation: pre-treatment (which is linked to the evolution of the channel) and the various process steps to be included on a FPGA hardware component.

Input:

The vector y of the received signal and the channel matrix.

Output:

A near optimal solution x_{HISD}

The treatment:

Pretreatment: search the D singular vectors associated with singular values of the channel matrix H (singular value decomposition SVD).

Phase 1: calculation of $\rho_{ZF} = Fy$ and $y^T H$

Phase 2: for each direction $k \in \{1 \ldots D\}$, generate I_k.

Note that it is possible at this level to remove redundant points.

Phase 3: for each direction $k \in \{1 \ldots D\}$, extraction of C candidate's points of I_k. With a minimum distance.

Phase 4: Creation of the overall ξ_{start}, then from every point of ξ_{start} use the iterative gradient method.

Phase 5: Saving the best solution found x_{HISD}

6. EQUALIZER PERFORMANCES IN MIMO SYSTEM

In this section we make some simulations to show the approach of the proposed detection. All experiments are described for a system of actual channel matrix of dimension m × n. The constellation is used on M-QAM modulation. According to the simulation model defined in before, the signal received in a given interval symbol can be written as follows:

$$y = Hx + W \quad (2)$$

Where the entries of the matrix H ∈ R^{mn} channel with unit variance and W ∈R^{mx1} are independent real random Gaussian variables and identically distributed with variance σ^2. The vector data takes values in the set $\{\pm 1\}^n$.

We present the results of simulation showing the performance of the algorithm HISD according to the number of candidate points C and the specific vectors D.

For 16-QAM modulation, the symbols x belongs to the set $\{\pm 1, \pm 3\}^n$. The optimum detector that minimizes the average error probability of the detection is given by the detector to maximum likelihood ML which solves the problem of following combinatorial optimization:

$$\hat{x} = \arg\min \|y - Hx\|^2_{x \in \{\pm 1, \pm 3\}^n} \quad (3)$$

This problem can be solved by searching all 4n possibilities. Clearly, as n increases, this option becomes impractical. So to improve the search for sub-optimal solution in the case of 16-QAM modulation, the HISD detector based on an intensification strategy (applied research in a localized region) and a diversification strategy (direct research the unknown regions) can be used as follows:

The idea of diversification step is to determine the achievable points near straight $\Delta_1, \ldots, \Delta_D$ to build a sub ξ_{start} set that contains a good starting points , A first diversity step is then obtained by

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the use of independent lines D. Thereafter, for each straight Δ_k , k = 1, …, D, the second phase is obtained by the intersection between Δ_k and right sides of the hypercube.

The bit error rate of 16-QAM modulation is presented in figure 3 and four receive antenna. Thus, we compare the performance in terms of BER for D = 2 and C = 4 of the proposed detector HISD, the optimal ML detector and linear sensors ZF and MMSE.

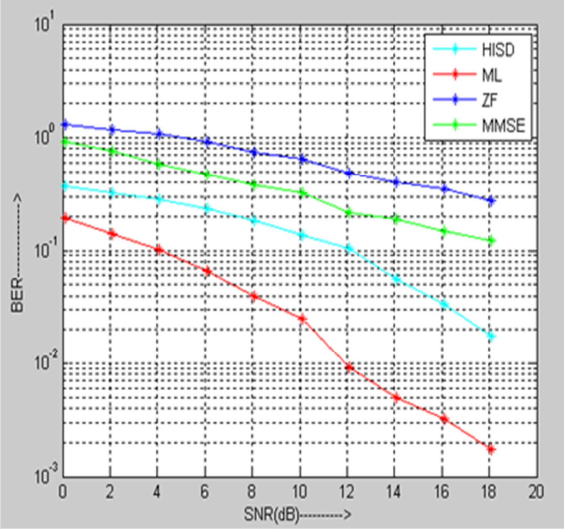

Figure. 3: BER as a function of SNR for a 4 × 4 MIMO system with 16-QAM modulation, comparing the performance of detectors HISD, ML, ZF and MMSE with D= 2 and C = 4

Note that HISD performance is clearly near to those of ML detectors. HISD performance is better than ZF and MMSE equalizers. We present in the next section a complexity comparison between the 4 equalizers studied.

According to [8] and [9] , we proof that by increasing the number of transmitting antenna and one receiving antenna, the bit error rate decreases. This confirms that the plurality of antennas reduces the likelihood of losing information.

Provide a statement that what is expected, as stated in the "Introduction" chapter can ultimately result in "Results and Discussion" chapter, so there is compatibility. Moreover, it can also be added the prospect of the development of research results and application prospects of further studies into the next (based on result and discussion).

7. HISD COMPLEXITY

This section determines the computational complexity of the proposed detection algorithm. We first calculate the number of multiplication and addition / subtraction in the required diversification step. Assume for simplicity that m = n. In a case of worst scenario, the complexity budget for diversification is shown in Table 1.

The computational complexity of HISD expense of two parameters C and D where D is the number of estimated directions and C represents the number of selected candidate points of x_{start}.

The algorithm can be divided into two parts. The first is the calculation of the inverse channel nickname of Moore-Penrose matrix defined by par $H^{+}= (H^{T}H)^{-1}H^{T}$ and the second is the use of the singular value decomposition for the D eigenvectors. Thus, the predominant complexity preparatory steps are O (n^3) per data block shown in Table 2.

Table 1: Complexity of calculating the diversification step for HISD detector

	Addition/Subtraction	Multiplication
HISD	$2n^3 + \frac{9}{2}n^2 - \frac{5}{2}n$	$2n^3 + 3n^2$

Table 2: Complexity Calculation for HISD detector

	Addition/Soustraction	Multiplication
HISD	$2Dn^3 + [\frac{9}{2} + C(3\theta+1)]Dn^2 - (2\theta - \frac{5}{2})n$	$2Dn^3 + [3 + C(2\theta+1)]Dn^2 + \theta n$

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The second part of the algorithm is to be executed for each received vector. The number of additions and multiplications of the second part in the worst case is expressed in Table 2.4. Note that the greedy search method is repeated using $\theta = 2$ times. In the most painful case, the total number of points attainable visited by the HISD algorithm is DCn θ + 2DN.

The complexity of the ML method is exponential. The performance of the proposed detector HISD is near ML performance, while the order of complexity in the worst case is lower than ML (against polynomial exponential).

The algorithm HISD being substantially parallel, the average cycle number is equal to two. The HISD is well suited for high-speed hardware architecture. For example, one can use the greedy search method in a parallel manner on C independent start. Furthermore, each direction of the eigenvector can be studied separately.

8. FPGA IMPLEMENTATION

An FPGA is an integrated circuit composed of a large number of programmable logic elements connected to each other through a routing matrix, it is also programmable.

The FPGA device enables the programmability of the target platform, similar to microprocessors. A circuit structure is controlled by a configuration stream that can be compared to a program stored in a memory [11]. This structure allows the FPGA to emulate any circuit, only on condition that it is not too big to not exhaust the logical resources and routing the FPGA. However, this flexibility of programmability is paid at the circuit performance. Although FPGAs are engraved with the same technology that generalist processors clocked at a few gigahertz, the FPGAs of clock frequency does not exceed a few hundred megahertz for newer models. Nevertheless, the great architectural freedom can make the most of fine-grained parallelism of the implemented circuits, which largely compensates for the low frequencies achievable. The language used is VHDL.

The VHDL language has been often used for implementing digital applications, hence its use in our work. The VHDL is a hardware description language for describing digital designs. The VHDL simplifies the development of complex systems such as Metaheuristic algorithm because it is possible to model and simulate a digital system from a high level of abstraction and with important facilities for modular design [12] , By using the VHDL, the circuit design shows some advantages: i) the implementation technology independence facilitates the migration to a newer technology, ii) it increases modular reusability, iii) it facilitates the automatic circuit generation, iv) it makes easy understanding of the high level code [13].

The finite state machines are used to describe sequential behavior related to the control of operative parts. This makes sequential appearance in the notion of internal state circuits implemented in the form of records.

We use parallel architecture in our HISD algorithm shown in figure 4. The parallelism is exploited to have a good performance and best solution using Finite State Machine (FSM). The HISD algorithm depends on two parameters that D is the number eigenvectors and C representing the number of the best candidates.

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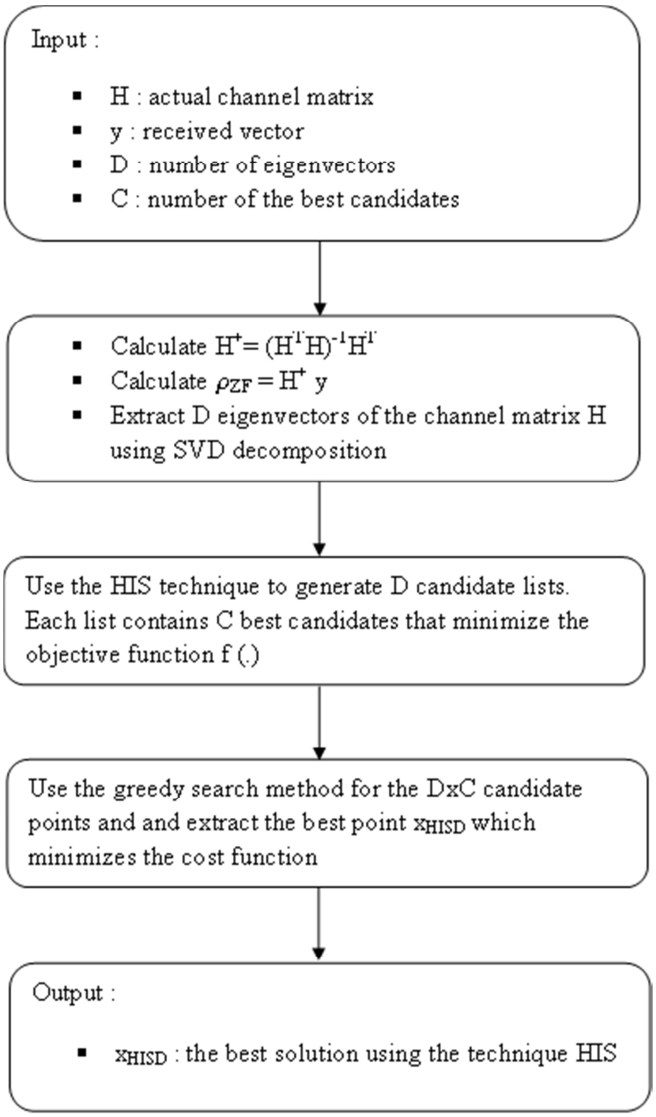

Fig.4: Flowchart of the proposed detection algorithm HISD

The control unit of the HISD algorithm generates suitable control signals to control the operation of different blocks of the logic process. This control unit is broken down into a hierarchy of Finite State Machines (FSM) [14]. An FSM is a sequential circuit with a finite number of states shown in figure 5.

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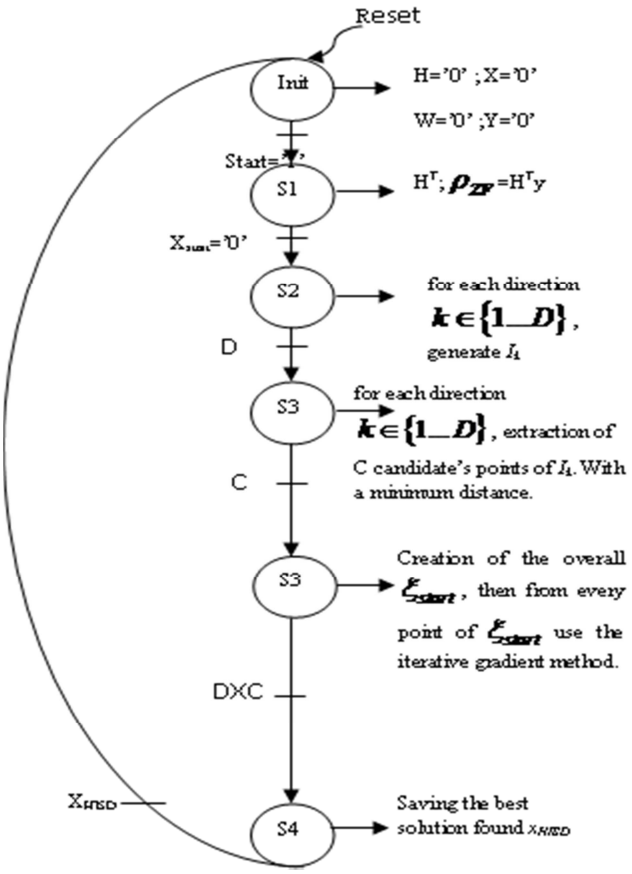

Fig. 5 : HISD logic FSM

In this paper, the FSM shown in figure 5 is defined by five states. At each clock front, one state is activated permitting the generation of the control signals and thus activating a new block of the design.

We present a design method of different detectors studied before when they are implemented in FPGA. We develop the result of HISD equalization algorithm implementation.

The software tools used are MATLAB, Xilinx ISE, and ModelSim.. The measurements have been simulated from the pose given in the database and corrupted with noises consistent with the ones encountered in the real test bench [15]. Figure 6 show the general model design of equalizer used in Simulink and XSG.

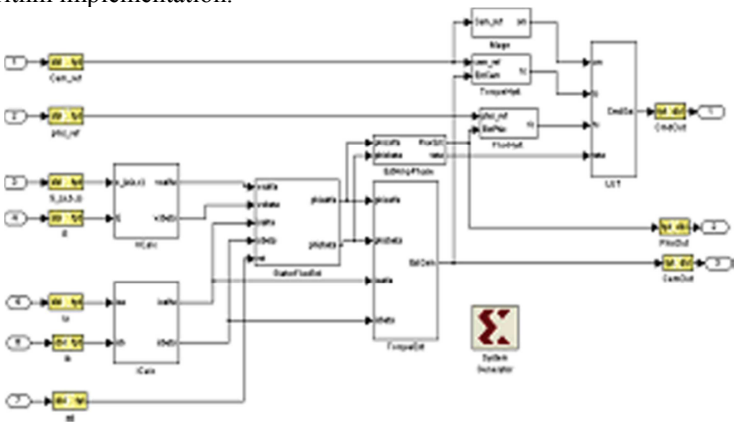

Fig. 6: General model design of HISD algorithm

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The yellow blocks represent the Gateway-in and the Gateway-out blocks. The other blocks are elementary blocks from the Xilinx block set which are essentially multipliers and adders and also some sub-systems doing complex addition and complex multiplication.

After designing the time domain model, we proceed to the FPGA implementation which is automatically done by the System Generator for DSP tool. It uses the Xilinx ISE 11.1 version to do all the flow.

We implement hardware architecture of MIMO equalizers systems based on Modified HSID. Once the algorithm was uploaded from the compact flash to be processed by the FPGA processor, start interruption was activated [16].

The design Of HISD equalizer will be implemented in FPGA board with one million gates. The Table 3 gives and clear idea about the FPGA logic blocks consumption by the design. The Table 4 gives the results of equalizers implementation using Virtex6 (XC6VLX75tl) FPGA.

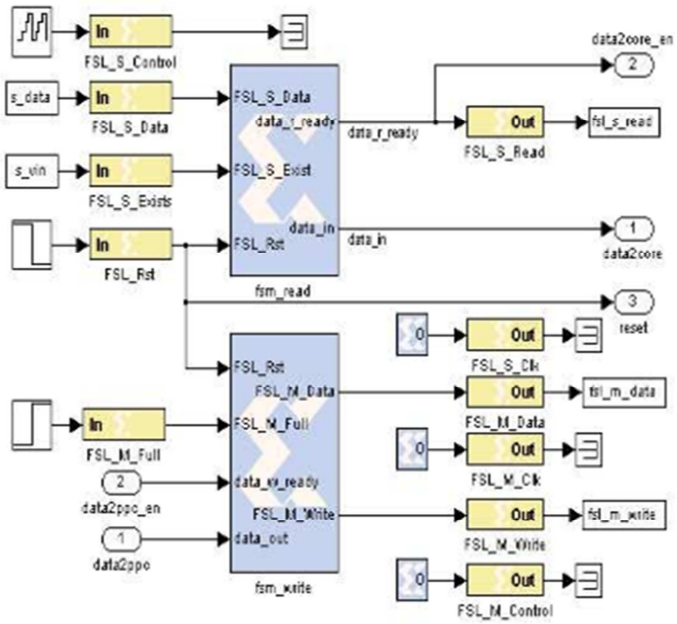

Figure 13: A system Generator description of the design of equalizers

Table 3: Utilization Hardware Resource Of HISD Implementation

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	144	15,360	1%	
Number of 4 input LUTs	12,230	15,360	79%	
Number of occupied Slices	6,278	7,680	81%	
Number of Slices containing only related logic	6,278	6,278	100%	
Number of Slices containing unrelated logic	0	6,278	0%	
Total Number of 4 input LUTs	12,240	15,360	79%	
Number used as logic	12,086			
Number used as a route-thru	10			
Number used as Shift registers	144			
Number of bonded IOBs	233	391	59%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	2.39			

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Table 4: Comparison Of Hardware Resources For Equalizers

Virtex6 XC6VLX75tl	ML	ZF	MMSE	HISD
Slice (93120)	12%(11174)	16% (14899)	20% (18624)	10% (9312)
LUTs (11640)	12% (1396)	14%(1629)	19%(2211)	11% (1280)
IOBs (240)	50% (120)	57% (136)	57% (136)	45% (108)
GCLKs (32)	3% (1)	3% (1)	3% (1)	3% (1)
Numbers of BRAM (156)	3% (5)	2.5 % (4)	2.5 % (4)	1.9 % (3)

Table 4 shows that the HISD approach has the better material performances than the others detectors.
The implementation results have the following execution time for MIMO system using modulation QAM 16 (n=5; m=6, C=4, D=2), Clock frequency is 50 MHz, and 80,000 data is sent continuously.

Table 6: ML And HISD Execution Time Results

Clock period (ns)	20	30	40	60
ML	120	210	260	275
HISD	110	180	240	260

The execution time increases, however, increases the clock period, so it is preferably to work with the smallest clock period to save runtime. The FPGA implementation shows in table 6 that the HISD approach has the better execution time than ML detector.

Simulation with ModelSim gives a curve which represents the performance of the ML detector and rated BER as a function of SNR practically identical to that obtained with Matlab, with a notable advantage: insurance real time while reducing execution time since we have found that the execution time given by the simulation in ModelSim (worth 240 ns) is much lower than that given by Matlab (worth 13.198 s).

9. CONCLUSION

In this paper, we focused on developing a new sub optimal detection method capable of giving a good approximation to the optimal solution and reduce the complexity of the ML detection problem. We proposed a sub-optimal method for maximum likelihood detection problem. This method is based on two complementary research techniques including: diversification and intensification. The diversification phase is defined by the search all feasible points near D straight through the ρ_{ZF} solution and direction D singular vectors of the matrix H. The scale-up is a simple local search, the method named greedy search. The presented method is able to produce a performance near to ML performance with constant computational complexity in polynomial time.
Our work is oriented subsequently to the implementation of FPGA detectors where one was interested mainly in the most optimum ML compared to HISD method.
The results of implementation show a better execution time and small hardware resources.
HISD is well suited for hardware implementation due to its near-optimal performance, reduced complexity and its highly parallel structure, future work will treat the implementation of this algorithm
It's important to develop perspective on FPGA design is to propose a prototyping development system of a fully integrated controller from VLSI technology and SoC design that can include digital control and its analog interface (sensors, ADC, power drivers, etc.) .

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