

IMPLEMENTATION AND RECONFIGURATION OF BASIC DIGITAL MODULATION DESIGN MODELS

B.K.V. PRASAD^{#1}, R. SAI PRIYA^{*2}

[#]ECE Department, KL University, Vijayawada, Vaddeswaram, Green Fields-522502, A.P, India

E-mail: ¹baditakali@gmail.com, ²rentachintalasaipriya@gamil.com

ABSTRACT

In modern communication systems the independent modulation and demodulation techniques is done using proper signal detection schemes and prominent receiver structure. The implementation of BPSK, FSK, ASK modulation and demodulation techniques are design using Simulink in system generator module which is transferred into Xilinx core and undergoes changes using system generator module. The modulated signals obtained from these simulations are analogized with the obtained signals after interfacing and programmed using an FPGA. The FPGA was programmed with the help of ARM processor to compile the bit files to select the required modulation based on our requirement that has best channel support. The interface is done between the controller and spartran-3e FPGA using JTAG. The XSVF format and synopsis programmed files are stored in the SD-card of the microcontroller. The HyperTerminal displays the output corresponding to the selected modulation. The optimum modulation is selected based on available bandwidth, bit-error-rate and signal to noise ratio. Hence, Among available tools for FPGA design, System Generator is a system-level modeling tool that provides, system complexity, power efficiency, better quality of service, bandwidth efficiency and, more secure, cost effectiveness, reliable and efficient compared to the analog communication.

Keywords: *Xilinx, BPSK (Binary phase shift keying), ASK(Amplitude Shift Keying), FSK(Frequency Shift Keying), Simulink, System Generator, FPGA (Field Programmable Gate Array).*

1. INTRODUCTION

1.1 Digital Communication Signals

It is the process of varying the properties of a periodic waveform known as carrier signal with a modulating signal that typically contains information to be transmitted[1]. It is the process of super imposing the information contents of a modulating signal on a carrier signal by altering its characteristics according to the given modulating signal. Digital modulation is the process by which symbols are transmitted into wave forms that are compatible with channel characteristics[1]. A Base band signal is converted in to band pass signal by modulation. To recognize the signal at the end demodulation process is used. This paper utilizes MATLAB simulink and system generator for simulation and implementation on spartran-3e FPGA board which involves flexibility for designing and testing that makes development very easy. It also provides flexibility of increasing the design and testing speed with in limited given time.

1.2 Types of Digital Modulation

BPSK:-

In Binary Phase Shift Keying (BPSK) only one sinusoidal wave is taken as the basis function. Modulation is obtained by changing the phase of this basis function depending on the given message bits. If 1 was transmitted the modulated signal remained unchanged i.e, the same as carrier i.e, with 0° initial phase. If 0 was transmitted the modulated signal changed 180° phase. This modulation is the most robust of all the PSKs since it takes the highest level of noise or distortion to make the demodulation reach a wrong or invalid decision. Thus it, however, can modulate only at 1 bit/symbol and so is

unsuitable for high data-rate applications.

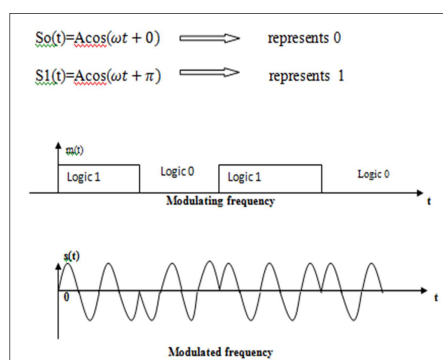


Fig. 1. BPSK modulation.

ASK:-

Amplitude-shift keying (ASK) is a type of amplitude modulation that involves representation of digital data as the changes in the amplitude of a carrier wave. In an Amplitude Shift Keying modulator, the binary symbol 1 is represented by transmitting a fixed-amplitude carrier wave and fixed frequency for a bit duration of N seconds. Here the strength of carrier signal is varied to represent binary 1 or 0. Both frequency & phase remain constant while amplitude changes, commonly, the amplitude decreases when zero transmits.

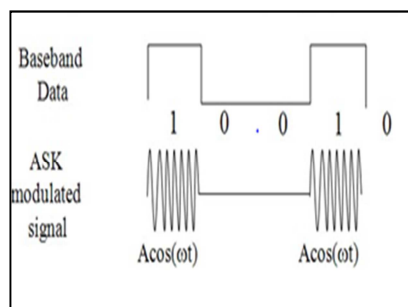


fig. 2. ASK Modulation.

FSK:-

It is a type of frequency modulation that involves representation of digital data as the changes of frequency of a carrier wave. To transmit a message signal for a certain long distance its frequency is modulated using carrier wave. Here both the phase and amplitude of the modulated wave remain unchanged and the respective frequencies for different logic values

gets changed. In case of positive ASK for logic 1 of message signal modulated wave gets more frequency and for logic 0 its frequency decreases.

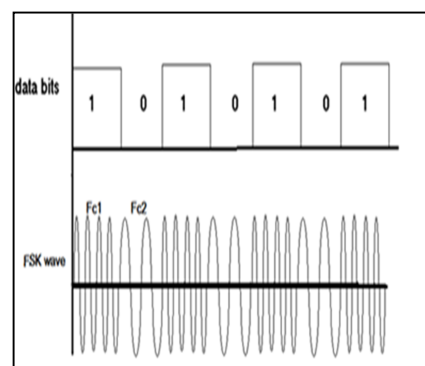


fig. 3. FSK Modulation

2. PREVIOUS WORKS

Previous work presents the implementation of Modulation techniques are created in Matlab/Simulink environment and System Generator. These modulation techniques has been implemented on FPGA [1][2][3][4][5].

Present work shows the Demodulation is the process used to recognize the signal at the receiving end.

This paper presents the simulation of modulation and demodulation techniques utilizes MATLAB simulink and system generator for simulation and implementation on spartan-3e FPGA board which involves flexibility for designing and testing that makes development very easy. It also provides flexibility of increasing the design and testing speed with in limited given time. The modulated signals obtained from these simulations are compared with the obtained signals after implementation. The FPGA was reconfigured and programmed with the help of ARM processor to compile the bit files to select the required modulation based on our requirement and application that has best channel support.

3. SOFTWARE METHODOLOGY

System Generator is a DSP tool from Xilinx based on the Matlab/Simulink environment and is used for FPGA design. System Generator is actually a library in Simulink which translates a Simulink model into a hardware realization of the same model. It also maps the system parameters defined in Simulink into entities and architectures, signals and ports in the hardware realization. Only the subsystems and blocks from the Xilinx Block set are translated by System Generator into hardware realization.

In order to program the FPGA, two distinct software packages are used: Matlab and Xilinx ISE. Matlab/Simulink is the software where the system functionality is verified and where the programming takes place and ISE is where the program will be configured to run on the FPGA. The connection that is involved between the two packages is System Generator, a part of Matlab, which converts the Simulink math code into VHDL code that is recognized by the ISE software.

3.1 Simulink Blockset

Pulse Generator: It involves a train of pulses.

Sine Wave: It generates sine functions.

Scope: Oscilloscope used to compare and see the results.

3.2 System Generator Blockset

Mcode: It calls a Matlab .m file and executes it.

Gateway In: It makes an approach to the representation of a signal behavior in hardware.

Gateway Out: it returns an approach of the signal behavior in hardware to that of simulation mode.

Mult: It performs the multiplication of its two inputs. System Generator: It provides control of the system and simulation parameters. It is used to call and execute the generated code.

FDATool: Filter Design and Analysis tool.

Resource Estimator: in the simulation of circuit the resources used are represented.

3.3 System Generator

It is a software tool that allows the creation and verification of hardware designs for Xilinx FPGA. It works along with Matlab and Simulink. It also allows the addition of DSP tools to design with FPGAs, automatic generation of HDL code starting from a Simulink model and allows the user to create its own libraries.

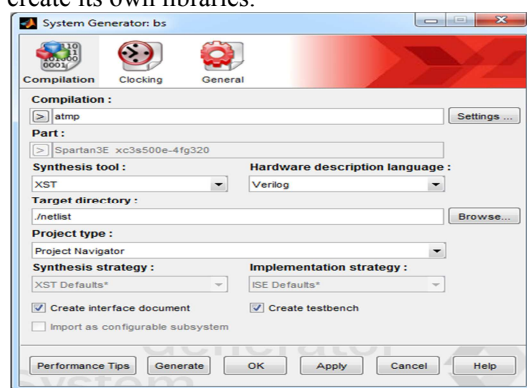


Fig. 4. System generator.

3.4 Modules of System generator

DDS Compiler:-

This block is used for generating the carrier waveform multiplexing in order to modulate the given message signal. Depending on the type of modulation there properties varies; like in case of BPSK 2 DDS compilers each with a phase difference of 180 degrees are generated. Multiplex depending on the input supplied to the selection line it selects whether a positive or negative sine should be supplied as a carrier.

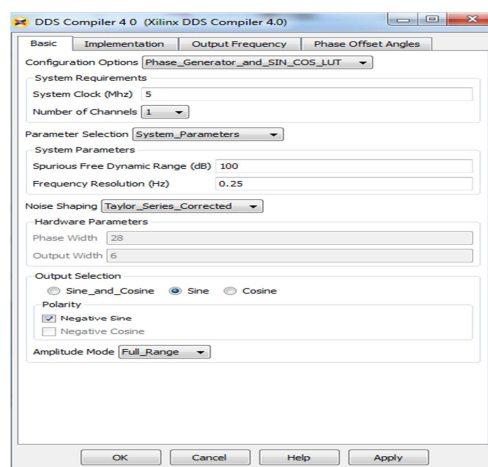


Fig. 5. DDS Compiler

FPGA getting hardware block with verilog code i.e JTAG block to view hard ware result on BPSK demodulation Scope. Both results should be same . Gateway In block makes an approach to the representation of a signal behavior in hardware. Gateway Out returns an approach of the signal behavior in hardware to that of simulation mode.

4.3 ASK Modulation Implementation

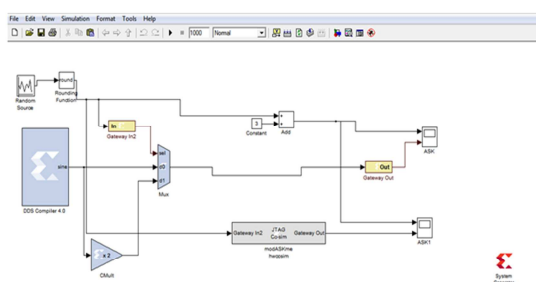


Fig. 8. ASK modulation

Multiplex depending on the input supplied to the selection line it selects the signals to display ASK modulated software output can be viewed on scope ,interfacing with sysgen on FPGA getting hardware block Both results should be same

4.4 ASK Demodulation Implementation

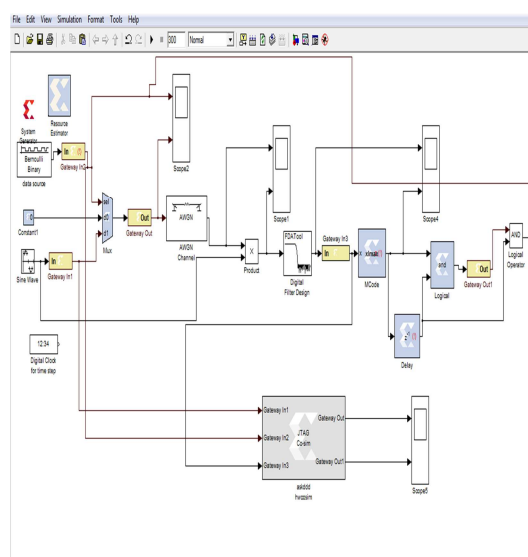


Fig. 9. ASK demodulation

The above fig.9. shows Bernoulli Binary source for producing discrete message signal and ASK modulated signal block and AWGN channel and Digital filter design blocks to make noise free channels given to scope inputs for demodulation process and Mcode block calls a Matlab .m file and executes it and which is used for the purpose of converting the transmitted analog in to digital signal and demodulated software signal can be viewed on scope and interfacing with sysgen on FPGA getting hardware block with verilog code i.e JTAG block to view hard ware result on ASK demodulation Scope. Both results should be same . Gateway In block makes an approach to the representation of a signal behavior in hardware. Gateway Out returns an approach of the signal behavior in hardware to that of simulation mode.

4.5 FSK Modulation Implementation

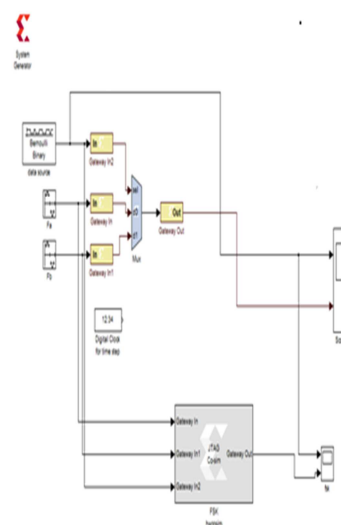


Fig. 10. FSK modulation

Multiplex depending on the input supplied to the selection line it selects the signals to display FSK modulated software output can be viewed on scope ,interfacing with sysgen on FPGA getting hardware block Both results should be same

4.6 FSK Demodulation Implementation

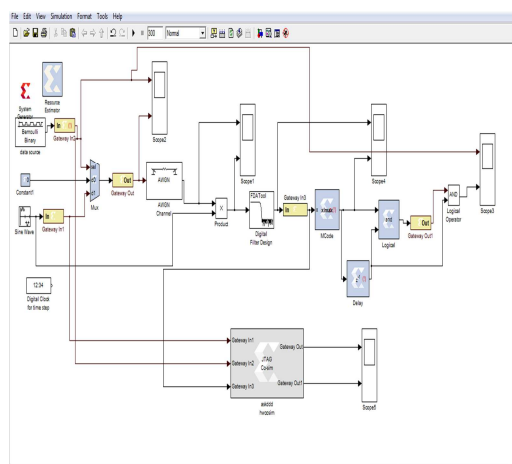


Fig. 11. FSK demodulation

4.7 Hardware Co simulation

After connecting all the required blocks for modulation in system generator vhdl is automatically generated for the designed block diagram. Using JTAG the generated blocks can be implemented on the Spartan 3e kit and the inputs to this are the same inputs supplied in the block design. Using this hardware block is generated for the software block design made. Both the results can be cross checked and will be same and can be viewed using the scope connected as outputs for the JTAG block.

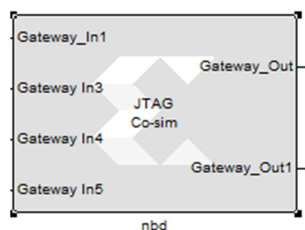


Fig. 12. JTAG Hardware block

4.8 Flow Graph

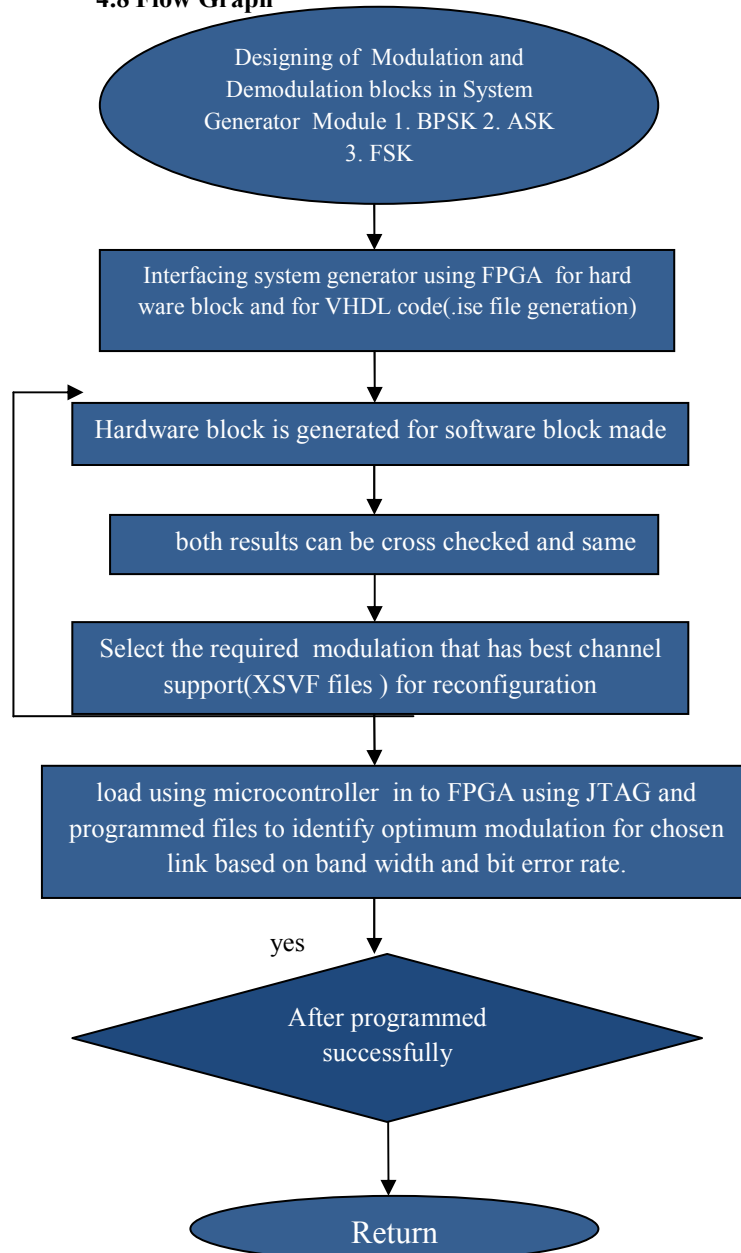


Fig. 13. Flow graph of Implementations of Modulations and Reconfiguration process

5. SOFTWARE AND HARDWARE RESULTS OF MODULATION AND DEMODULATION MODELS

5.1 BPSK Modulation Results

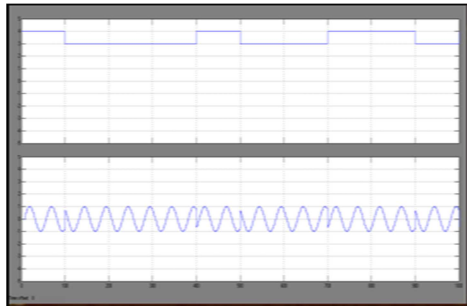


fig. 14. Software output waveform

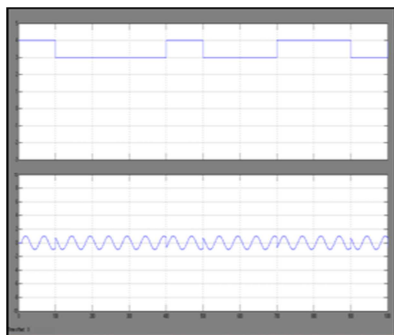


fig. 15. Hardware output waveform

5.2 BPSK Demodulation Results



fig. 16. Software output waveform

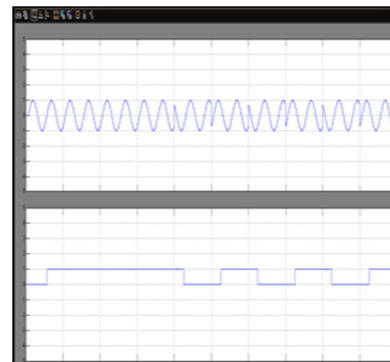


fig. 17. Hardware output waveform

5.3 ASK Modulation Results

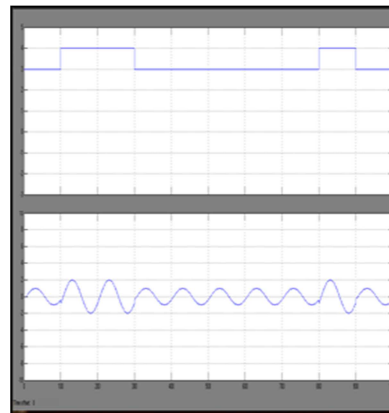


fig. 18. Software output waveform

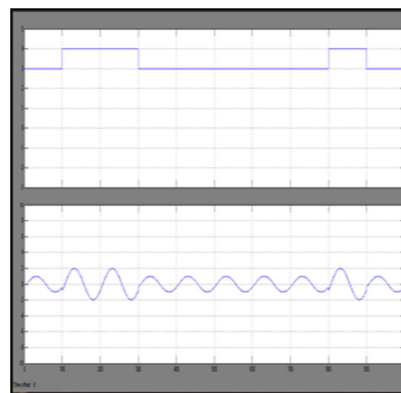


fig. 19. Hardware output waveform

5.4 ASK Demodulation Results

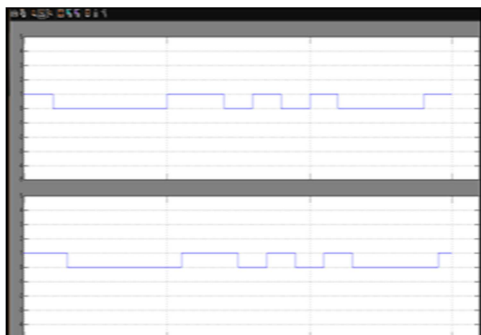


fig.20. Software output waveform

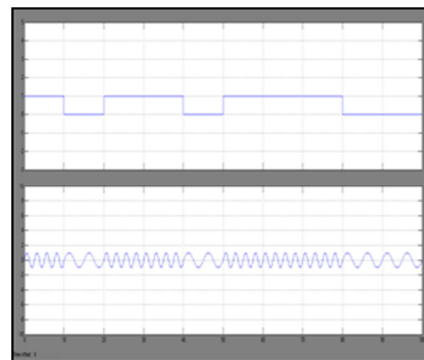


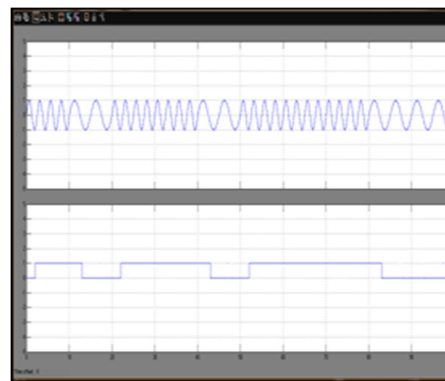
fig. 23. Hardware output waveform

5.6 FSK Demodulation Results

fig. 24. Software output waveform



fig. 21. Hardware output waveform



5.5 FSK Modulation Results

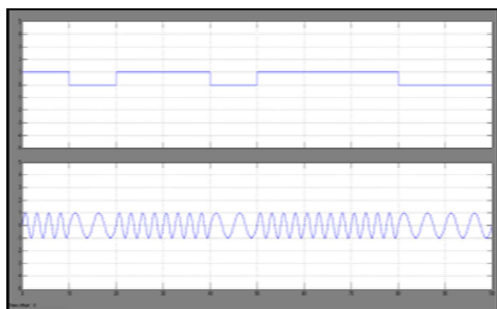


fig.22. Software output waveform

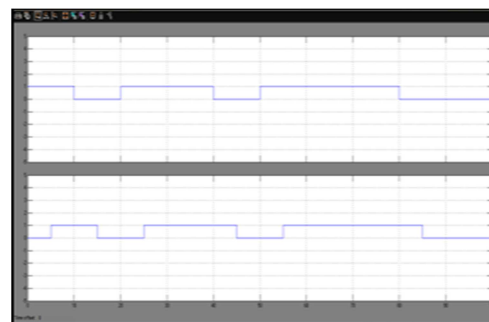


fig. 25. Hardware output waveform

6. RECONFIGURATION PROCESS

The FPGA was programmed with the help of ARM processor to compile the bit files to select the required modulation based on our requirement that has best channel support. The interfacing is done with System Generator between the controller and spartran-3e FPGA using JTAG. The XSVF format and synopsis programmed files are stored in the SD-card of the microcontroller. The HyperTerminal displays the output corresponding to the selected modulation. The optimum modulation is selected based on available bandwidth, bit-error-rate and signal to noise ratio. Hence, Among available tools for FPGA design, System Generator is a system-level modeling tool that provides better quality of service, system complexity, power efficiency, bandwidth efficiency and cost effectiveness, more secure, reliable and efficient compared to the analog communication.

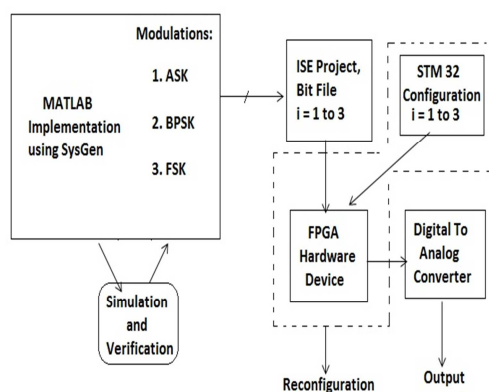


Fig. 26. Block diagram of the Experimental system using Reconfiguration process

```

1. ASK modulation
2. BPSK modulation
3. FSK modulation
4. Exit

Enter your choice

ASK modulation detected
File "0:/ASK/ASK.XSV" opened successfully

SUCCESS - Completed XSVF execution.

Successfully configured FPGA with ask.xsv Modules
File opened successfully to write
Blocks used are:
Xilinx Adder/Subtractor Block
Xilinx Bus Multiplexer Block
Xilinx Constant Block Block
Xilinx Constant Multiplier Block
Xilinx DDS Compiler 4.0 Block
dcu_input_clock_period' => 100
deprecated_control' => 'off'
design' => 'ask'
designFile' => 'ask.v'
device' => 'xc3s250e-4tq144'
device_speed' => -4

```

fig. 27. ASK Modulation Reconfigured output

```

File "0:/FSK/FSK.XSV" opened successfully
SUCCESS - Completed XSVF execution.

Successfully configured FPGA with fsk.xsv Modules
File opened successfully to write
Blocks used are:
Xilinx Adder/Subtractor Block
Xilinx Bus Multiplexer Block
Xilinx Constant Block Block
Xilinx DDS Compiler 4.0 Block
dcu_input_clock_period' => 100
deprecated_control' => 'off'
design' => 'fsk'
designFile' => 'fsk.v'
device' => 'xc3s250e-4tq144'
device_speed' => -4

```

fig. 28. FSK Modulation Reconfigured output

```

SUCCESS - Completed XSVF execution.

Successfully configured FPGA with bpsk.xsv Modules
File opened successfully to write
Blocks used are:
Xilinx Adder/Subtractor Block
Xilinx Bus Multiplexer Block
Xilinx Constant Block Block
Xilinx DDS Compiler 4.0 Block
dcu_input_clock_period' => 10
deprecated_control' => 'off'
deprecated_control_sgadvanced' => ''
design' => 'bpsk2'
designFile' => 'bpsk2.v'
device' => 'xc3s250e-4tq144'
device_speed' => -4

```

fig. 29. BPSK Modulation Reconfigured output

Above figure.27&28&29 describes the XSVF format and synopsis programmed files are stored in the SD-card of the microcontroller. The HyperTerminal displays the output corresponding to the selected modulation for a chosen link based on signal position.

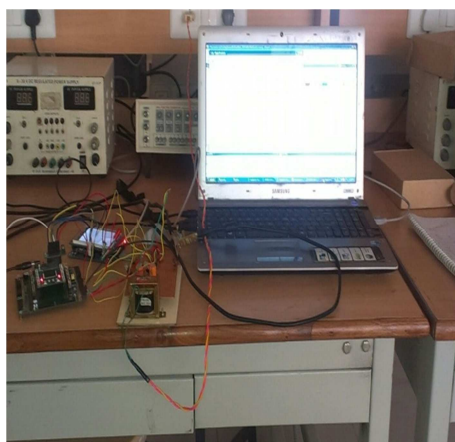


Fig. 30: Reconfiguration set up for different modulations.

7. CONCLUSION

Digital modulation is less complex, more efficient and most secure in very long distance transmission. The noise detection and correction is more efficient in digital modulation than analog. Because of the usage of FPGAs, the design can have low power consumption, small size and involves less cost.

In this project, BPSK and ASK,FSK systems with modulators has been designed and tested. While testing the detector, the delay in the recovered data at the output of the detector is observed, and it is found that the delay is due to the computational delay of multiplier block(mux). The results given by the development board (hardware) exactly matches with the results obtained from simulation setup(software)and also done the reconfiguration process which is used to select the required modulation for optimization which we cant do by using single FPGA. In Reconfiguration process The optimum modulation is selected based on available bandwidth, bit-error-rate and signal to noise ratio. Hence, Among available tools for FPGA design, System Generator is a system-level modeling tool that provides better quality of service, system complexity, power efficiency, bandwidth efficiency and cost effectiveness, more secure, reliable and efficient compared to the analog communication.

REFERENCES

- [1] A.H. Bastami, and A. Olfat, "Selection Relaying Schemes for Cooperative Wireless Networks With Adaptive Modulation", IEEE Transactions on Vehicular Technology, Volume: 60, Issue: 4 May 2011. Page(s):1539 - 1558.
- [2] Popescu, S. O.; Gontean, A.S.; Budura, G., "Simulation and implementation of a BPSK modulator on FPGA," Applied Computational Intelligence and Informatics (SACI), 2011 6th IEEE International Symposium on, vol., no., pp.459, 463, 19-21 May 2011.
- [3] Kikkert, C.J.; Blackburn, C., "Demodulating binary phase shift keyed signals using programmable logic devices," Signal Processing and Its Applications, 1999. ISSPA '99. Proceedings of the Fifth International Symposium on, vol.2, no., pp.689, 692, vol.2, 1999.
- [4] Y.H.Chye, M.F.Ain, N.M.Zawawi, "Design of BPSK Transmitter Using FPGA with DAC", in Proceedings of the 2009 IEEE 9th Malaysia Conference on Communications, Malaysia, 2009.
- [5] F.Xiong, "Digital Modulation Techniques", Artech House, UK, 2010.
- [6] .Linn, Y., "An Ultra Low Cost Wireless Communications Laboratory for Education and Research," Education, IEEE Transactions on, vol.55, no.2, pp.169, 179, May 2012.
- [7] .Xilinx System Generator for DSP User Guide, r10.1.1, April 2008.
- [8] http://www.mathworks.com/products/demos/simulink/Simulink_Key_Features/videos/building.html.
- [9] Vivado Design Suite User Guide: Getting Started (UG910), System Generator for DSP User Guide (UG640).
- [10] Lia-hua jiang, Chaun Huang, "Design and Realization of Multiplexer based on Schematic and VHDL Optics photonics and Engineering(OPEE), 2010 International Conference on 2010, volume 1.

- [11] Spartan-3 Generation Configuration User Guide...xilinx.(http://www.xilinx.com/support/documentation/user_guides/).
- [12] Karris S.T. (2008). "Introduction to Simulink: With Engineering Applications", Orchard Publications.
- [13] Linfei-yu; Qiao wei-ming; Wang Yan-Yu; Liu Tai-lian; zhang jian Chuan, "Efficient WCDMA digital down convertor design using System Generator" on Space Science, year: 2009 IEEE transactions on communications pages 89-92, DOI: 10.1109/ICON SPACE 2009.5352664.
- [14] Mohamed-Slim Alouini, and Anlei Rao, "Multiuser Diversity with Adaptive Modulation in Non-Identically Distributed Nakagami Fading Environments", IEEE transactions on vehicular technology, volume 61, no. 3, march 2012.
- [15] Wei Xing Zheng, and Jinhui Zhang, "Design of Adaptive Sliding Mode Controllers for Linear Systems via Output Feedback", IEEE Transaction on Industrial Electronics, Volume: 6, Issue: 7 Publication Year: 2014, Page(s): 3553-3562.