Journal of Theoretical and Applied Information Technology
15th August 2016. Vol.90. No.1

ISSN: **1992-8645** www.jatit.org E-ISSN: **1817-3195**

TAGUCHI MODELING WITH THE INTERACTION TEST FOR HIGHER DRIVE CURRENT IN WSI_X/TIO_2 CHANNEL VERTICAL DOUBLE GATE NMOS DEVICE

[1]K.E. KAHARUDIN, [2]F. SALEHUDDIN, [3]A.S.M. ZAIN, [4]M.N.I.A. AZIZ
[1]Postgraduate Student, [2]Senior Lecturer, [3]Senior Lecturer, [4]Postgraduate Student at Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Hang Tuah Jaya, Durian Tunggal, 76100 Melaka
E-mail: [1]khairilezwan@yahoo.com.my, [2]fauziyah@utem.edu.my, [3]anissuhaila@utem.edu.my, [4]naazirullifwatt@hotmail.com

ABSTRACT

This paper presents a study in which Taguchi method has been utilized to increase the drive current (I_{ON}) in the WSi_x/TiO_2 Vertical Double Gate NMOS Device. The performance of the device is evaluated in term of its highest drive current (I_{ON}) value. Initially, the Vertical Double Gate NMOS device is virtually fabricated and characterized by using both ATHENA and ATLAS modules of SILVACO TCAD tools. The L_{12} orthogonal array, main effects, signal-to noise ratio (SNR) and analysis of variance (ANOVA) are utilized in order to analyze the effect of process parameter variations on the drive current (I_{ON}). The interaction between the process parameters are also investigated by using L_8 orthogonal array of Taguchi method. Based on the results of the analysis, source/drain (S/D) implant energy has been identified as the most dominant process parameter in which it has contributed 90% of factor effects on SNR. The highest possible value of drive current (I_{ON}) after the optimization and the interaction test is 2859.7 µA/µm.

Keywords: *ANOVA, Drive Current, NMOS, SNR, Taguchi method*

1. INTRODUCTION

The vertical double-gate layout of Metal-oxide-semiconductor Field Effect Transistor (MOSFET) device offers a number of advantages over the planar MOSFET layout. The vertical double-gate MOSFET device does not require an advanced lithography process to obtain a short channel length (L_c) because it is defined by retarded etching of the silicon pillar [1]. The layout of vertical double-gate MOSFET device allows the channel width per device area to be doubled, thus increasing the packing density and the drive current (I_{ON}) [2]. Besides that, the vertical double-gate MOSFET provides an almost ideal subthreshold swing (SS) and low off-state leakage current (I_{OFF}). Other advantages of vertical double-gate MOSFET is an easy integration with planar MOSFET since the drain region is located at the top and the source is located at the bottom [3].

However, the vertical double-gate MOSFET with traditional poly-Si/SiO_2 technology is not capable of producing higher drive current (I_{ON}) that meets the requirement of high performance (HP) multi gate (MG) technology predicted by International Technology Roadmap Semiconductor (ITRS) 2013. For the year 2020, the drive current (I_{ON}) for high performance (HP) multi gate (MG) technology must be equal or higher than 1480 µA/µm [4]. It is hard for poly-Si/SiO2 technology to generate a high drive current (I_{ON}) due to the equivalent oxide thickness (EOT) limitation [5]. Therefore, metal-gate/high-k stack technology are implemented in vertical double-gate MOSFET to overcome EOT limitation since the thickness of high-*k* dielectric does not contribute to the degradation of device performance [6]. In the current research, titanium dioxide (TiO_2) is used as the gate dielectric in which the tungsten silicide (WSi_x) is used as the gate electrode of the vertical double gate NMOS device [7].

This paper attempts to describe the optimization of multiple process parameters for the highest value of drive current (I_{ON}) in WSi_x/TiO_2 vertical double-gate NMOS device. Taguchi method have been widely employed by researchers to obtain the robust design of MOSFET device. Salehuddin *et al.* have utilized Taguchi method for optimization of process parameter variations in 45nm MOSFET device [8]-[10]. These studies have proved that Taguchi method was able to identify the most significant process parameters that affect the threshold voltage (V_{TH}), sheet resistance (Rs), off-state leakage current (I_{OFF}) and drain induced barrier lowering (DIBL). Afifah Maheran *et al.* have utilized Taguchi method in designing and optimizing the 22nm gate length WSi_x/TiO_2 NMOS device [11]-[13]. The study reported that Taguchi method has successfully predicted the robust recipe in obtaining the nominal threshold voltage (V_{TH}) and the lowest leakage current (I_{OFF}) value.

The optimization study presented in this paper was divided into two stages. The first stage emphasizes on the optimization of 11 process parameters towards the I_{ON} by using the L_{12} Taguchi method. The analysis was further enhanced by adding the interaction test analysis using the L_8 Taguchi method in order to investigate the presence of the interaction effect among the process parameters. The optimal combination level of process parameters was then determined from the highest I_{ON} value.

2. PROCESS SIMULATION

The process simulation was executed by utilizing ATHENA module of Silvaco software. The sample used in the process simulation was <100> orientation of p-type (boron doped) silicon substrate with concentration of 1 x 10^{14} atom/cm^3. The silicon pillar was formed by the etching process in order to separate the two vertical metal gates (WSi_x). The silicon substrate was oxidized for about 0.1 ms to ensure a thin oxide layer of 1 nm was grown. The silicon substrate was then doped with 1.81 x 10^{12} atoms/cm^3 of boron at 20 Kev and tilted at 7°. Next, the oxide layer was etched in order to substitute it with titanium dioxide (TiO_2). The metal-gate which was tungsten silicide (WSi_x) was deposited at the top of thin TiO_2 layer. The halo implantation process was then employed by injecting 1.86 x 10^{13} atoms/cm^3 of indium at 170 kev and tilted at 25° into the channel region.

The process was then followed by depositing sidewall spacer. The source/drain implantation was implemented by implanting arsenic with the dose of 1.22 x 10^{18} atoms/cm^3 at 3 kev and tilted at 80°. Finally, compensation implantation was utilized by implanting phosphor dosage of 2.51x10^{12} atom/cm^3 at 60 kev and tilted at 7°. The aluminum layer was deposited on the top structure's surface and any unwanted aluminum was etched to develop the contacts [14], [15]. The completed structure of WSi_x/TiO_2 channel vertical double-gate NMOS device is illustrated as in Figure 1.

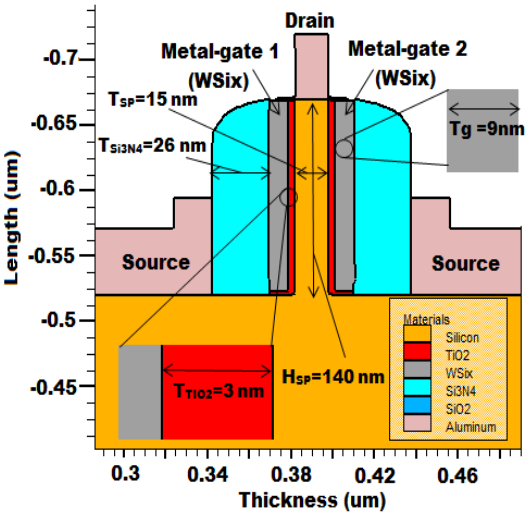

Figure 1: Final Structure of WSix/TiO_2 Vertical Double Gate NMOS Device

3. DEVICE CHARACTERIZATION

The device characteristics of the WSi_x/TiO_2 vertical double-gate NMOS devices were extracted by utilizing ATLAS module of Silvaco software. Figure 2 depicts the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05 V and V_D = 1.0 V for vertical double gate NMOS device. The value of I_{ON}, I_{OFF} and SS was extracted from the graph.

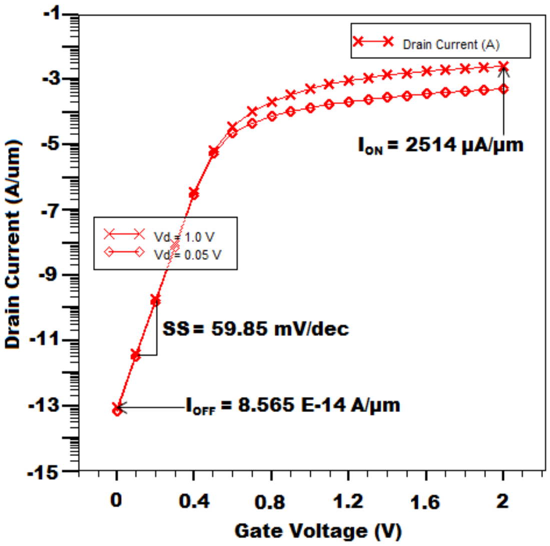

Figure 2: Graph of subthreshold drain current (I_D)-gate voltage (V_G)

Based on the graph, the initial value of I_{ON} was 2514 µA/µm. Meanwhile, the leakage current I_{OFF}

was observed to be 8.565 E-14 A/µm. The SS value was then extracted from the inverse slope of $\log_{10} I_D$ vs. V_{GS} characteristic. It shows how much change in the gate voltage is required to change the drain current by one decade as shown in (1) [14]:

$$SS = \left[\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right]^{-1} \quad (1)$$

The value of SS was observed to be 59.85 mV/dec. The SS is one of the important characteristics of the MOSFET's device that indicates the speed of switching transition from "ON" to "OFF" state or vice versa.

4. OPTIMIZATION OF PROCESS PARAMETERS WITHOUT THE INTERACTION TEST USING L_{12} OA OF TAGUCHI METHOD

4.1 *Selection of the Process Parameters and the OA*

The process parameters that were investigated were: substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, V_{TH} implant tilt, halo implant dose, halo implant energy, halo implant tilt, S/D implant dose, S/D implant energy, S/D implant tilt and compensation implant dose. Each of them were represented by symbols: A, B, C, D, E, F, G, H, J, K and L. Meanwhile, compensation implant energy and compensation implant tilt were regarded as the noise factors as they have a little influence on I_{ON} value. The values of the process parameters (control factors) and noise factors at different levels are listed in Table 1 and Table 2.

The selection of an appropriate orthogonal array (OA) depends on the total degrees of freedom (DF) of the process parameters. The degree of freedom (DF) is defined as the number of comparisons between process parameters that are required to be made in order to determine the best level [16]. In general, the number of degrees of freedom associated with a factor is equal to one less than the number of levels for that factor. In the current study, since each process parameter has two levels, the total DF for the process parameters are equal to 11. Basically, the DF for the OA should be greater than or at least equal to those for process parameters. Therefore, the L_{12} (2^{11}) orthogonal array with eleven columns and twelve rows has been selected for this study. The experimental layout for the process parameters using the $L_{12}(2^{11})$ orthogonal array is shown in Table 3.

Table 1: Process Parameters and Their Levels

Process Parameter	Units	Level 1	Level 2
A-Substrate Implant Dose	atom/cm^3	$1\text{x}10^{14}$	$1.03\text{x}10^{14}$
B-V_{TH} Implant Dose	atom/cm^3	$1.81\text{x}10^{12}$	$1.84\text{x}10^{12}$
C-V_{TH} Implant Energy	kev	20	22
D-V_{TH} Implant Tilt	degree	7	10
E-Halo Implant Dose	atom/cm^3	$1.86\text{x}10^{13}$	$1.89\text{x}10^{13}$
F-Halo Implant Energy	kev	170	172
G-Halo Implant Tilt	degree	25	28
H-S/D Implant Dose	atom/cm^3	$1.22\text{x}10^{18}$	$1.25\text{x}10^{18}$
J-S/D Implant Energy	kev	3	5
K-S/D Implant Tilt	degree	80	83
L-Compensation Implant Dose	atom/cm^3	$2.51\text{x}10^{12}$	$2.54\text{x}10^{12}$

Table 2: Noise Factors and Their Levels

Noise factor	Units	Level 1	Level 2
U-Compensation Implant Energy	kev	60	62
V-Compensation Implant Tilt	degree	7	10

Table 3: L_{12} OA of Taguchi Method

Exp. No	Process Parameter (Control Factors) Level										
	A	B	C	D	E	F	G	H	J	K	L
1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	2	2	2	2	2	2
3	1	1	2	2	2	1	1	1	2	2	2
4	1	2	1	2	2	1	2	2	1	1	2
5	1	2	2	1	2	2	1	2	1	2	1
6	1	2	2	2	1	2	2	1	2	1	1
7	2	1	2	2	1	1	2	2	1	2	1
8	2	1	2	1	2	2	2	1	1	1	2
9	2	1	1	2	2	2	1	2	2	1	1
10	2	2	2	1	1	1	1	2	2	1	2
11	2	2	1	2	1	2	1	1	1	2	2
12	2	2	1	1	2	1	2	1	2	2	1

4.2 *Signal-to-noise ratio (SNR) Analysis*

The signal-to-noise ratio (SNR) was utilized to measure the sensitivity of the process parameters towards the I_{ON} in a controlled manner. In Taguchi method, the term 'signal' represents the desirable effect (mean) for the I_{ON}. Meanwhile, the term 'noise' represents the undesirable effect (signal disturbance) for the I_{ON}. The objective of SNR analysis is to determine the highest SNR of the results. A higher value of SNR of certain factor implies that the signal of the factor is higher than the random effects of the noise factors. To obtain the highest possible I_{ON} value, the-higher-the-better quality characteristics has to be employed. The SNR (Higher-the-better), η can be expressed as [17]:

$$\eta = -10Log_{10}\left[\frac{1}{n}\sum_{i=1}^{n}\frac{1}{y_i^2}\right] \qquad (2)$$

where n is number of tests and yi is the experimental values of the I_{ON}.

Table 4 depicts the experimental results for drive current (I_{ON}) and the corresponding SNR by using (2). Since the experimental design is orthogonal, the effect of each process parameter is possible to be separated out. For instance, the mean SNR for factor B (V_{TH} Implant Dose) at level 1 can be calculated by averaging the SNR for experiment row (1-3) and (7-9) by referring to Table 3. The mean SNR for each level of the other process parameters can be calculated in the similar procedure. The SNR (Higher-the-better) for each level of process parameters with an overall mean of SNR were summarized in Table 5.

Table 4: L_{12} OA of Taguchi Method

Exp no.	Drive Current , I_{ON} (mA/µm)					
	I_{ON1} (U_1V_1)	I_{ON2} (U_1V_2)	I_{ON3} (U_2V_1)	I_{ON4} (U_2V_2)	Mean (10^{-7})	SNR (dB)
1	2514	2518.1	2512	2511.1	1.58	68.01
2	2780.1	2784.3	2777.9	2776.9	1.29	68.88
3	2738.7	2743	2736.7	2735.8	1.33	68.75
4	2520	2524.2	2518	2517	1.57	68.03
5	2393.8	2397.6	2391.5	2390.6	1.75	67.58
6	2848	2850.2	2843.8	2842.8	1.23	69.09
7	2384.8	2388.7	2382.7	2381.7	1.76	67.55
8	2527.3	2531.4	2525.2	2524.2	1.57	68.05
9	2843.2	2847.2	2840.9	2839.9	1.24	69.07
10	2826.9	2831.1	2824.8	2823.8	1.25	69.03
11	2398	2401.9	2395.7	2394.7	1.74	67.60
12	2760.9	2765.1	2758.9	2757.9	1.31	68.82

Table 5: SNR of Process Parameters

Symbol	Process Parameter	SNR (Higher-the-better) in dB		Overall mean SNR (dB)
		Level 1	Level 2	
A	Substrate Implant Dose	68.39	68.35	68.37
B	V_{TH} Implant Dose	68.39	68.36	
C	V_{TH} Implant Energy	68.40	68.34	
D	V_{TH} Implant Tilt	68.39	68.35	
E	Halo Implant Dose	68.36	68.38	
F	Halo Implant Energy	68.36	68.38	
G	Halo Implant Tilt	68.34	68.40	
H	S/D Implant Dose	68.39	68.36	
J	S/D Implant Energy	67.80	68.94	
K	S/D Implant Tilt	68.55	68.20	
L	Compensation Implant Dose	68.35	68.39	

Figure 3 shows the SNR response graph for the I_{ON}. The higher the SNR of a process parameter is, the lower variance will be around the desired value. However, the relative importance among the process parameters for the I_{ON} are still needed to be known so that the most significant process parameters can be determined accurately. This will be discussed in the next section using the analysis of variance (ANOVA).

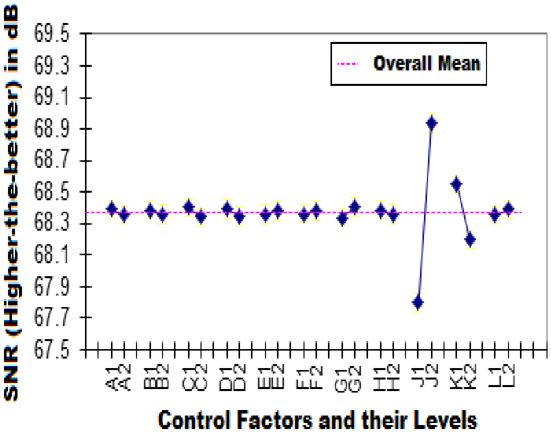

Figure 3: Factor Effects graph for SNR (higher-the-better)

4.3 *Analysis of Variance (ANOVA)*

The primary goal of the analysis of variance (ANOVA) was to identify which process parameters significantly affect the value of the I_{ON}. Table 6 displays the results of pooled ANOVA for higher I_{ON}. The F-ratio is computed for 95% level of confidence. Based on the results, factor J (S/D implant energy) and factor K (S/D implant tilt) were identified as the most significant process parameters that influence the I_{ON} value where each of them have contributed 90% and 9% of factor effect on SNR respectively.

Table 6: Results of ANOVA

Factor	DF	SSQ	MS	F-value	Factor effect on SNR (%)	Dominant/ Significant/ Neutral
A	1	0	0	9	0	Neutral
B	1	0	0	6	0	Neutral
C	1	0	0	26	0	Neutral
D	1	0	0	16	0	Neutral
E	1	0	0	5	0	Neutral
F	1	0	0	2	0	Neutral
G	1	0	0	28	0	Neutral
H	1	0	0	6	0	Neutral
J	1	4	4	9041	90	Dominant
K	1	0	0	853	9	Significant
L	1	0	0	9	0.09	Neutral

4.4 *Verification Test*

Based on the SNR analysis and the ANOVA, the optimal combination level of process parameters for higher I_{ON} is $A_1B_2C_1D_2E_2F_2G_2H_2J_2K_1L_1$. Table 7 shows the best level setting of the process parameters for higher I_{ON} in vertical double-gate NMOS device suggested by L_{12} OA of Taguchi method.

Table 7: Best Combinational Levels of Process Parameters

Sym.	Process Parameter	Units	Best Value
A	Substrate Implant Dose	atom/cm^3	$1x10^{14}$
B	V_{TH} Implant Dose	atom/cm^3	$1.81x10^{12}$
C	V_{TH} Implant Energy	kev	20
D	V_{TH} Implant Tilt	degree	7
E	Halo Implant Dose	atom/cm^3	$1.89x10^{13}$
F	Halo Implant Energy	kev	172
G	Halo Implant Tilt	degree	28
H	S/D Implant Dose	atom/cm^3	$1.22x10^{18}$
J	S/D Implant Energy	kev	5
K	S/D Implant Tilt	degree	80
L	Compensation Implant Dose	atom/cm^3	$2.54x10^{12}$

The vertical double-gate NMOS device was re-simulated by using the optimized level of process parameters predicted by Taguchi method. The simulation results are listed in Table 8. It was observed that the highest value of I_{ON} was 2849.2 µA/µm with SNR of 69.11 dB. However, the I_{ON} value was not the highest among all the I_{ON} values in Table 4. Therefore, the interaction effects among the process parameters were anticipated to be presented on the device. After some observation of the results, factor C (V_{TH} implant energy), factor E (halo implant dose) and factor G (halo implant tilt) were suspected to have interaction effects with each others.

Table 8: Verification Results for I_{ON} using L_{12} OA

I_{ON} (mA/µm)				SNR (Higher-the-better) in dB
I_{ON1} (U_1V_1)	I_{ON2} (U_1V_2)	I_{ON3} (U_2V_1)	I_{ON4} (U_2V_2)	
2845	2849.2	2842.8	2841.8	69.11

In the next section, the three suspected process parameters were re-analyzed for the interaction test by using L_8 OA of Taguchi method. Since, the interaction test using the L_8 OA of Taguchi method required the involvement of five factors, factor J (S/D implant energy) and factor K (S/D implant tilt) were added to the interaction test analysis. Meanwhile, the level of the remaining process parameters that were not involved in the interaction test were fixed as listed in Table 7.

5. OPTIMIZATION OF PROCESS PARAMETERS WITH THE INTERACTION TEST USING L_8 OA OF TAGUCHI METHOD

5.1 *Selection of the Process Parameters and the OA*

Five process parameters which were factor C (V_{TH} implant energy), factor E (halo implant dose), factor G (halo implant tilt), factor J (S/D implant energy) and factor K (S/D implant tilt) were selected in the design of experiment (DoE) with the interaction test. Among these process parameters, halo implant tilt was suspected to interact with substrate implant dose and V_{TH} implant dose. The L_8 orthogonal array of Taguchi method was utilized for the interaction test where each of the factors was varied into two levels as displayed in Table 9. Factor C (V_{TH} implant energy), factor E (halo implant dose), factor G (halo implant tilt), factor J (S/D implant energy) and factor K (S/D implant tilt) were re-assigned as factor A, B, C, D and E respectively. The noise factors were kept at the same level as in Table 2. Eight sets of experiment were run as outlined in Table 10.

Table 9: Process Parameters and Their Levels

Sym.	Process Parameter	Units	Level 1	Level 2
A	V_{TH} Implant Energy	kev	20	22
B	Halo Implant Dose	atom/cm^3	$1.86x10^{13}$	$1.89x10^{13}$
C	Halo Implant Tilt	degree	25	28
D	S/D Implant Energy	kev	3	5
E	S/D Implant Tilt	degree	80	83

Table 10: L_8 OA of Taguchi Method with Interaction

Exp no.	Process Parameter						
	A	B	N(AxB)	C	D	M(BxC)	E
1	1	1	1	1	1	1	1
2	1	1	1	2	2	2	2
3	1	2	2	1	1	2	2
4	1	2	2	2	2	1	1
5	2	1	2	1	2	1	2
6	2	1	2	2	1	2	1
7	2	2	1	1	2	2	1
8	2	2	1	2	1	1	2

Table 11 shows the experimental results for I_{ON} value and their corresponding SNR by using Eqn. (2). Meanwhile, the mean of SNR for each level of process parameters is computed and listed in Table 12.

Table 11: Experimental Results for I_{ON} and SNR

Exp no.	Drive Current , I_{ON} (mA/µm)					
	I_{ON1} (U_1V_1)	I_{ON2} (U_1V_2)	I_{ON3} (U_2V_1)	I_{ON4} (U_2V_2)	Mean (10^{-7})	SNR (dB)
1	2549.4	2553.4	2547.1	2546.2	1.54E-07	68.13
2	2777.9	2782.2	2775.7	2774.7	1.30E-07	68.87
3	2396.1	2400	2393.8	2392.9	1.74E-07	67.59
4	2845	2849.2	2842.8	2841.8	1.24E-07	69.08
5	2784.3	2788.5	2782.1	2781.1	1.29E-07	68.89
6	2536.1	2540.3	2534	2533	1.56E-07	68.08
7	2844.3	2848.4	2842	2841	1.24E-07	69.08
8	2382.4	2386.4	2380.3	2379.3	1.76E-07	67.54

Table 12: SNR of Process Parameters

Symbol	Process Parameter	SNR (Higher-the-better) in dB		Overall mean SNR (dB)
		Level 1	Level 2	
A	V_{TH} Implant Energy	68.42	68.40	68.41
B	Halo Implant Dose	68.49	68.32	
N(AxB)	AxB	68.40	68.41	
C	Halo Implant Tilt	68.42	68.39	
D	S/D Implant Energy	67.83	68.98	
M(BxC)	BxC	68.41	68.41	
E	S/D Implant Tilt	68.59	68.22	

Based on the data in Table 12, the factor effects graph for SNR (Higher-the-better) is plotted as illustrated in Figure 4. The dashed horizontal lines in the graph represent the overall mean of SNR (Higher-the-better) which is 68.41 dB. From the graph, it can be observed that factor $A_1B_1C_1D_2E_1$ have been selected as the optimum value due to their higher SNR.

In order to determine whether the interaction is present or not, a proper interpretation of results is required. In general, the method is to separate the influence of an interacting process parameter from the influence of the others. Factor: AxB and BxC are the interactions that have been investigated in this study.

In the interaction test analysis, column 3 and column 6 in Table 10 is not used. However, the columns that represent the individual factors are used in the analysis. It can be observed that the column 1 of Table 10 indicates A_1 is contained in experiment row 1, 2, 3 and 4, while B_1 is in experiment row 1, 2, 5 and 6. However, the rows that contain both A_1 and B_1 are in experiment row 1 and 2. Therefore, the average SNR for A_1B_1 is computed from the results of experiment row 1 and 2.

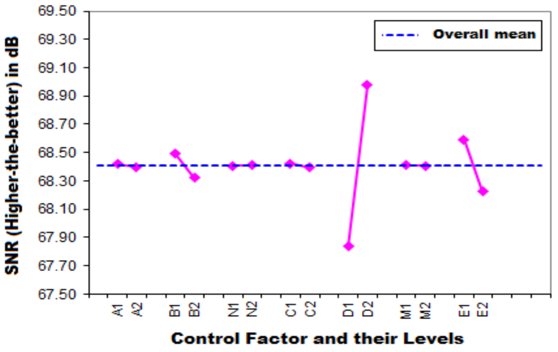

Figure 4: Factor Effects graph for SNR (higher-the-better)

The average effect of $\overline{A_1B_1}$ = (68.13+68.87) / 2 = 68.50. The two corresponding experiment rows for A_1B_2 are row 3 and 4, hence the average effect of $\overline{A_1B_2}$ = (67.59+69.08) / 2 = 68.33. In the computations for $\overline{A_1B_1}$ and $\overline{A_1B_2}$, factor level A_1 is fixed. The difference between the result for $\overline{A_1B_1}$ = 68.50 and $\overline{A_1B_2}$ = 68.33 is due only to factor B. By using similar method, $\overline{A_2B_1}$, $\overline{A_2B_2}$, $\overline{B_1C_1}$, $\overline{B_1C_2}$, $\overline{B_2C_1}$ and $\overline{B_2C_2}$ can be computed as well. The test of interaction for AxB and BxC is illustrated in Figure 5 and Figure 6 correspondingly. The intersection line in Figure 5 indicates that there is the interaction effect between A and B. Since, there is no intersection line Figure 6, it is assumed that there is no interaction effects between B and C. Therefore the optimum level for factor A, B and C are $A_1B_1C_1$ as they exhibit the highest SNR.

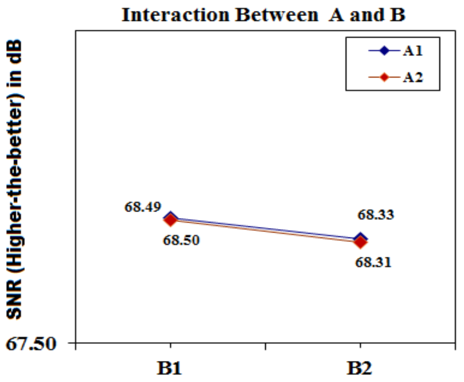

Figure 5: The Interaction Test for AxB

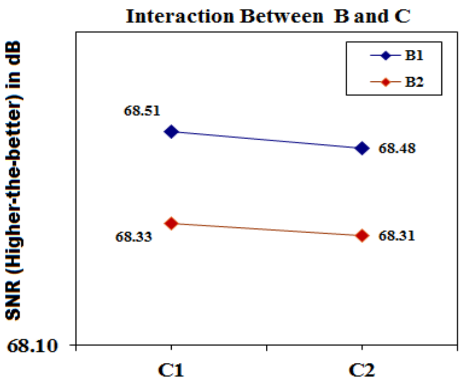

Figure 6: The Interaction Test for BxC

5.2 *Analysis of Variance (ANOVA)*

The ANOVA was utilized to figure out the most significant process parameters that influenced the I_{ON} value in the WSi_x/TiO_2 vertical double-gate NMOS device. In addition, the contribution of each process parameter was also determined by computing the percentage of factor effect on SNR. Table 13 shows the results of pooled ANOVA.

Table 13: Results of ANOVA

Factor	DF	SSQ	MS	F-value	Factor effect on SNR (%)	Dominant/ Significant/ Neutral
A	1	0	0	0	0	Neutral
B	1	0	0	0	2	Neutral
N(AxB)	1	0	0	0	0	-
C	1	0	0	0	0	Neutral
D	1	2	0	11	67	Dominant
M(BxC)	1	0	0	0	0	-
E	1	0	0	1	7	Neutral

The F-ratio were evaluated for 95% level of confidence. Factor D (S/D implant energy) were the most significant factors that contribute to the higher I_{ON} value. Based on SNR analysis, interaction test and ANOVA, the optimal combination levels of process parameters for the highest I_{ON} value is $A_1B_1C_1D_2E_1$.

5.3 *Verification Test*

Verification test was executed because the optimal combination levels of process parameters, i.e. $A_1B_1C_1D_2E_2$ in the present study did not match any experiment of the orthogonal array in Table 10. The best level setting of the process parameters for the WSi_x/TiO_2 vertical double-gate NMOS device suggested by Taguchi method is shown in Table 14.

The final step is to verify the increase of I_{ON} value by simulating the device once again using the best level setting of process parameters. The results of the final simulation of the device are recorded in Table 15.

Table 14: Best Level Setting of Process Parameters

Sym.	Process Parameter	Units	Best Value
A	V_{TH} Implant Energy	kev	20
B	Halo Implant Dose	atom/cm^3	$1.86x10^{13}$
C	Halo Implant Tilt	degree	25
D	S/D Implant Energy	kev	5
E	S/D Implant Tilt	degree	80

Table 15: Verification Results for I_{ON} using L_8 OA

Drive Current, I_{ON} (µA/µm)				SNR (Higher-the-better) in dB
I_{ON1} (U_1V_1)	I_{ON2} (U_1V_2)	I_{ON3} (U_2V_1)	I_{ON4} (U_2V_2)	
2855.5	2859.7	2853.2	2852.2	68.98

The SNR for the WSi_x/TiO_2 vertical double-gate NMOS device after the optimization approach was 63.98 dB. The value was within the predicted SNR range of 68.41 to 69.55 dB. The highest possible I_{ON} value was observed to be 2859.7µA/µm. Table 16 shows the comparison of I_{ON} values before the optimization, after optimization without the interaction test, after optimization with the interaction test and the ITRS 2013 prediction.

Table 16: Comparison of the I_{ON} values from Different Approaches

Device Characteristics	Before Optimization	Optimization without the Interaction Test	Optimization with the Interaction Test	ITRS 2013 Prediction [4]
I_{ON} (µA/µm)	2514	2849.2	2859.7	≥ 1480

It is observed that the final results after the optimization with the interaction test has yielded the highest I_{ON} value. There is an improvement of 12.1 % in I_{ON} value if compared to the I_{ON} value before optimization approach (2514 µA/µm). The I_{ON} value was observed to be further improved by 0.37% when utilizing the optimization with the interaction test approach. Furthermore, the I_{ON} value of 2859.7 µA/µm exceeds the expected I_{ON} value for high performance (HP) multi-gate (MG) technology for the year 2020 as predicted by ITRS 2013 [4].

6. CONCLUSIONS

Based on the analysis of the results, it can be concluded that the I_{ON} value of the vertical double WSi_x-based gate NMOS device has successfully been optimized by using Taguchi method. The most significant factors (process parameters) identified from the ANOVA are S/D implant energy and S/D implant tilt where each of them contributes 90% and 9% of factor effect on SNR accordingly. The optimal I_{ON} value retrieved from the Taguchi analysis without the interaction test is observed to be 2849.2 µA/µm. Meanwhile, the optimal I_{ON} value retrieved from the Taguchi analysis with the interaction test is observed to be 2859.7 µA/µm. There is a slight improvement of 0.37% compared to the result retrieved from the Taguchi analysis without the interaction test. The results have proven that the interaction test of the Taguchi method is capable of finding the robust process recipe for higher I_{ON} value in vertical double WSi_x-based gate NMOS device.

ACKNOWLEDGEMENT:

The authors would like to thank to the Ministry of Higher Education (MOHE), MyBrain15 and the Centre for Telecommunication Research and Innovation (CeTRI), Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for sponsoring this research study under the research grants (PJP/2014/FKEKK(6B)/S01341).

REFERENCES:

[1] J. Rahul, S. Yadav, V.K. Bohat, "Effects of Metal Gate Electrode and HfO_2 in Junction less Vertical Double Gate MOSFET", *International Journal of Scientific Engineering and Technology*, Vol. 674, No. 3, 2014, pp. 671-674.

[2] I. Saad, R. Ismail, "Self-aligned vertical double-gate MOSFET (VDGM) with the oblique rotating ion implantation (ORI) method", *Microelectronics Journal*. Vol. 39, No. 12, 2008, pp. 1538-1541.

[3] M. Masahara, Y. Liu, S. Hosokawa, T. Matsukawa, K. Ishii, H. Tanoue, K. Sakamoto, T. Sekigawa, H. Yamauchi, S. Kanemaru, E. Suzuki, "Ultrathin Channel Vertical DG MOSFET Fabricated by Using Ion-Bombardment-Retarded Etching", *IEEE Transactions on Electron Devices*, Vol. 51, No. 12, 2004, pp. 2078-2085.

[4] ITRS, "Table PIDS2a High-performance (HP) Logic Technology Requirements-TCAD," International Technology Roadmap Semiconductor, 2013 Report; https://www.dropbox.com/sh/qz9gg6uu4kl04vj/AACy2nA7lJHLaN9np1ZTheNva/PIDS_2013Tables.xlsx?dl=0

[5] R. Chau, S. Datta, M. Doczy, B. Doyle,J. Kavalieros, M. Metz, "High-k/metal-gate Stack and its MOSFET characteristics", *IEEE Electron Device Letters*, Vol. 5, No. 6, 2004, pp. 408-410.

[6] N. Atan, I. Ahmad, B. Y. Majlis, I. A. Fauzi, "Effects of High-k Dielectric with Metal Gate for Electrical Characteristics of Nanostructured NMOS", *Mathematical Methods in Engineering and Economics*, Vol. 1, 2014, pp. 111-115.

[7] A. H. Afifah Maheran, P.S. Menon, I. Ahmad, S. Shaari, "Optimisation of Process Parameters for Lower Leakage Current in 22nm n-type MOSFET Device using Taguchi Method", *Jurnal Teknologi (Sciences & Engineering)*, Vol. 68, No. 4, 2014, pp. 1-5.

[8] F. Salehuddin, I. Ahmad, F. A. Hamid, A. Zaharim, U. Hashim, P.R. Apte, "Optimization of input process parameters variation on threshold voltage in 45 nm NMOS device", *International Journal of the Physical Sciences*, Vol. 6, No. 30, 2011, pp. 7026-7036.

[9] F. Salehuddin, K.E. Kaharudin, A.S.M. Zain, A.K. Mat Yamin, I. Ahmad, "Analysis of process parameter effect on DIBL in n-channel MOSFET device using L_{27} orthogonal array", *AIP Conf. Proc.*, 2014, pp. 322-328.

[10] F. Salehuddin, I. Ahmad, F.A. Hamid, A. Zaharim, H.A. Elgomati, B.Y. Majlis, "Impact of SALICIDE and Source / Drain Implants on Leakage Current and Sheet Resistance in 45nm NMOS Device", *Journal of Telecommunication, Electronic and Computer Engineering*, Vol. 2, No. 1, 2010, pp. 35-41.

[11] A.H. Afifah Maheran., P.S. Menon, I. Ahmad, S. Shaari, H.A. Elgomati, B.Y. Majlis, F. Salehuddin, "22nm NMOS device with lowest leakage current optimized using Taguchi Method", *Communications, Circuits and Educational Technologies*, 2014. pp. 170-173.

[12] A.H. Afifah Maheran., P.S. Menon, I. Ahmad, S. Shaari, H.A. Elgomati, B.Y. Majlis, F. Salehuddin, "Design and Optimization of 22nm NMOS Transistor", *Australian Journal of Basic and Applied Sciences*, Vol. 6, No. 7, 2012, pp. 1-8.

[13] A.H. Afifah Maheran, P.S. Menon, I. Ahmad, S. Shaari, H.A. Elgomati, F. Salehuddin, "Design and Optimization of 22 nm Gate Length High-*k*/Metal gate NMOS Transistor", *Journal of Physics: Conference Series*, Vol. 431, 2013, pp. 1-9.

[14] K.E. Kaharudin, A.H. Hamidon, F. Salehuddin, "Impact of Height of Silicon Pillar on Vertical

DG-MOSFET Device”, *International Journal of Computer, Information, Systems and Control Engineering*, Vol. 8, No. 4, 2014, pp. 576-580.

[15] K.E. Kaharudin, A.H. Hamidon, F. Salehuddin, “Implementation of Taguchi Modeling for Higher Drive Current (I_{ON}) in Vertical DG-MOSFET Device”, *Journal of Telecommunication, Electronic and Computer Engineering*, Vol. 6, No. 2, 2014, pp. 11-18.

[16] S. Kamaruddin, Z.A. Khan, S.H. Foong, “Application of Taguchi Method in the Optimization of Injection Moulding Parameters for Manufacturing Products from Plastic Blend”, *International Journal of Plastics Technology*, Vol. 14, No. 6, 2010, pp. 152-166.

[17] M.S. Phadke, “Signal-to-noise Ratio,” in *Quality Engineering Using Robust Design*, Pearson Education, 2001, pp. 111.