CONTROL OF THREE LEVEL INVERTER BASED DYNAMIC VOLTAGE RESTORER

[1]S.LEELA, [2]S.S.DASH

[1] Research Scholar, Dept.of Electrical & Electronics Engg., Bharath University, Chennai, India-600073.

[2] Prof., Department of Electrical & Electronics Engineering, SRM University, Chennai, India -603203.

E-mail: sleela13@yahoo.in , munu_dash_2K@yahoo.com

ABSTRACT

This paper deals with modelling and digital simulation of three level inverter based Dynamic Voltage Restorer(DVR). The control of DVR that injects a voltage in series with a distribution feeder is presented. DVR is a power electronic controller that can protect sensitive loads from disturbances in supply system. It is observed that DVR can regulate the voltage at the load. Circuit model is developed and the same is used for simulation studies.

Keywords: *Dynamic Voltage Restorer(DVR), Matlab simulink, Series Compensation, 3 level inverter*

1. INTRODUCTION

A power electronic converter based series compensator that can protect critical loads from all supply side disturbances other than outages is called a dynamic voltage restorer. The restorer is capable of generating or absorbing independently controllable real and reactive power at its AC output terminal. This device employs solid state power electronic switches in a pulse width modulated (PWM) inverter structure. It injects a set of three phase AC output voltages in series and synchronism with the distribution feeder voltages. The amplitude and phase angle of the injected voltages are variable there by allowing control of the real and reactive power exchange between the device and the distribution system. The DC input terminal of the restorer is connected to an energy source or an energy storage device of appropriate capacity.The reactive power exchanged between the restorer and the distribution system is internally generated by the restorer without AC passive reactive components. The real power exchanged at the restorer output AC terminals is provided by the restorer input DC terminal from an external energy source or energy storage system. In August 1996, Westinghouse Electric Corporation installed world's first dynamic voltage restorer in Duke Power Company's 12.47 kV substation in Anderson, South Carolina. This was installed to provide protection to an automated rug manufacturing plant. Prior to this connection, the restorer was first installed at the Waltz Mill test facility near Pittsburgh for the full power tests. The test results are discussed in [1]. The next commissioning of the restorer was done at Westinghouse in February 1997 in Powercor's 22 kV distribution system at Stanhope, Victoria, Australia to protect a diary milk processing plant. The saving that results from the installation of this installation is estimated at over $100,000 per year [2]. In the next phase of development, Westinghouse (now taken over by Siemens) installed world's first platform mounted dynamic voltage restorer to protect Northern Lights Community College and several other smaller loads in Dawson Creek, British Columbia, Canada [3].

This paper extends the concept of dynamic voltage restorer further to tightly regulate the load voltage. It can also perform the primary functions of the restorer, i.e., to protect the load from temporary voltage interruption, sag/swell etc. This device is called a dynamic voltage regulator (DVR). For the control operation of DVR we stipulate that real power supplied by the device in steady state is zero. Based on this stipulation, the references of the voltages that are to be injected in series are generated. This requires online extraction of the fundamental positive sequence based on the sampled values. Once the reference voltage s are obtained, they are tracked by the VSIs realizing the DVR.

The actual implementation of the DVR using inverters raises additional issues of switch frequency injection. To eliminate these, two different filter structures are discussed here. The inclusion of the filters further complicates the problem of voltage tracking. To facilitate proper voltage tracking a switching band control scheme is used here. The proposed DVR is validated through digital computer simulation studies. New approach to load balancing and power factor correction is given by Ghosh[4]. Power inverter operations for series compensation is given by [5]. Transient analysis of alternator is given by [6].

The above literature does not deal with the modelling of DVR system using matlab simulink. In this work, an attempt is made to model and simulate the DVR system using simulink.

2. DVR CHARACTERISTICS

In this section we shall present the fundamental, positive-sequence, steady state analysis of a DVR connected power system.The voltage regulation scheme is shown in Figure.1. This consists the following:

- DVR: represented by voltage sources V_{fa}, V_{fb} and V_{fc}
- Supply voltage: represented by sources V_{sa}, V_{sb} and V_{sc}

The DVR is connected between a terminal bus on the left and a load bus on the right. The voltage sources are connected to the DVR terminals by a feeder with an impedance of R+jX. We shall assume that the loads are balanced and the load impedance is given by $Z_l = R_l + jX_l$. It is to be noted that the phase angle Φ_l between the load terminal V_l and the line current i_s depends on the load impedance and is independent of the line impedance or the DVR voltage.

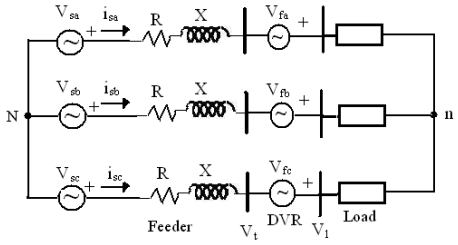

Figure.1. Schematic diagram of a DVR connected to a power system.

The objective of the discussion presented below is to regulate the magnitude of the load voltage equal to that of the source voltage through DVR voltage injection. Further we stipulate the following condition on the DVR:

- The DVR does not supply any real power in the steady state. This implies that the phase angle difference between DVR voltage phasor and line current phasor must be Π /2 in the steady state.

Let us assume that the load current lags the load voltage. To draw a phasor diagram of the steady state operation, we assume that the load voltage is fixed at V per unit and the source voltage is allowed to vary. Since the primary target is to make the magnitudes of $V_l$and Vs equal, the locus of desirable V_s is the arc NB as shown in Figure.2.

To make the magnitude of the load voltage equal to that of the source voltage, the RI_s drop must be less than NM. If the drop is less than this limiting value, the DVR must compensate the entire reactive drop in the feeder and provide additional injection such that the source voltage becomes V per unit.

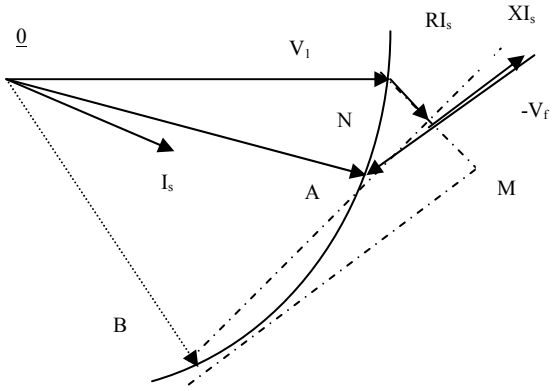

Figure.2. Phasor diagram showing multiple solutions

It can be seen from Figure.2 that there are two possible intersection points with the arc-one at A and the other at B. This implies that two possible values of DVR voltage and can be obtained for each feeder drop. For the first value, the source voltage will be along OA, while for the other value, it will along OB. It is needless to say that the best choice is the A intersection requiring much smaller voltage injection from the DVR.

Example 1: In this example, we illustrate the procedure for the steady-state computation of

DVR voltage. Let the feeder impedance be 0.5+j0.3 per unit, while the load impedance be 2.5+j2 per unit. We now connect a DVR aiming to regulate the load voltage to 1.0 per unit. Let us assume that rms load voltage is given by $\vec{V}_l = 1\angle 0^0$ per unit. The line current is then

$$I_S = \frac{1\angle 0^0}{R_l + jX_l} = 0.3123\angle -38.66^0 \text{ p.u}$$

For zero DVR power, its voltage must be in quadrature to the line current. We then have

$$\vec{V}_f = \left|\vec{V}_f\right| e^{j\angle(\vec{I}_s+90)} = \left|\vec{V}_f\right|\angle 51.34^0 = \left|\vec{V}_f\right|(a_1 + jb_1) \longrightarrow (1)$$

where a_1+jb_1 is a unit phasor at 90^0 to $\vec{I}_s$. Again from Fig.1 we get

$$\vec{V}_s + \vec{V}_f = \vec{V}_l + (R + jX)\vec{I}_s = \vec{V}_l + a_2 + jb_2 \longrightarrow (2)$$

where a_2 + jb_2 represents the feeder drop. Subsituting (1) in (2) and rearranging we get

$$\vec{V}_s = \vec{V}_l + a_2 + jb_2 - \left|\vec{V}_f\right|(a_1 + jb_1) \longrightarrow (3)$$

The following quadratic equation is then obtained from the magnitude condition of (3)

$$\left|\vec{V}_f\right|^2 - 2\left\{a_1\left(\left|\vec{V}_1\right| + a_2\right) + b_1 b_2\right\}\left|\vec{V}_f\right| + \left(\left|\vec{V}_l\right| + a_2\right)^2 + {b_2}^2 - \left|\vec{V}_s\right|^2 = 0 \longrightarrow (4)$$

Let us assume that the magnitude of the source voltage is 1.0 per unit. Then solving the above equation we get

$$\left|\vec{V}_f\right| = 0.1137 \,\&\, 1.3231$$

These two values of the magnitude of the injected voltage correspond to two operating points (A and B) in Figure 2. We shall obviously choose the lower of the two values.

3. SIMULATION RESULTS

Digital simulation is done using the blocks of Matlab simulink and the results are presented here. Three level inverter system is shown in Figure 3a. The output of the inverter without filter is shown in Figure 3b. The output with filter is shown in Figure 3c. DVR using multilevel inverter is shown in Figure 4a. The output of the inverter is injected into line through a transformer. At t=0.2sec, the additional load is switched on. The voltage across load 1 decreases as shown in Figure 4b. DVR injects the voltage at t=0.4secs. The voltage across the loads 1 & 2 will resume to the normal value. FFT analysis for the output voltage is shown in Figure 4c. THD is 27.3%.

DVR system with LC filter is shown in Figure 5a. Injected voltage and the voltage across loads 1 & 2 are shown in Figure 5b. FFT analysis for the output voltage is shown in Figure 5c. THD reduces to 0.8%. Thus the harmonics are reduced from 27.3% to 0.8%.

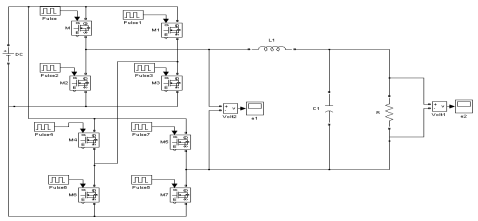

Figure 3a. THREE LEVEL INVERTER

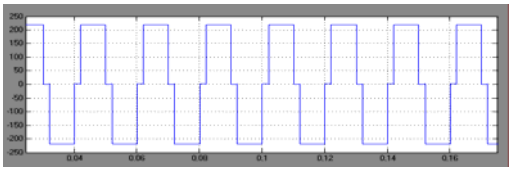

Figure 3b. OUTPUT OF THREE LEVEL INVERTER WITHOUT FILTER

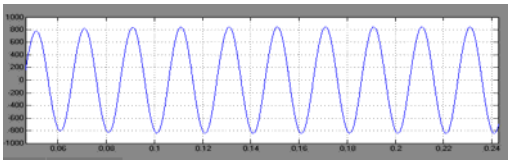

Figure 3c. OUTPUT OF THREE LEVEL INVERTER WITH FILTER

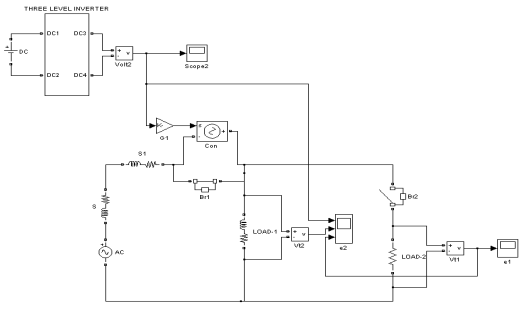

Figure 4a. DVR WITHOUT LC FILTER

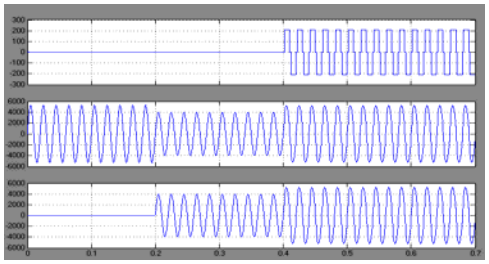

Figure 4b. VOLTAGE ACROSS EXTERNAL, LOAD-1 &LOAD-2

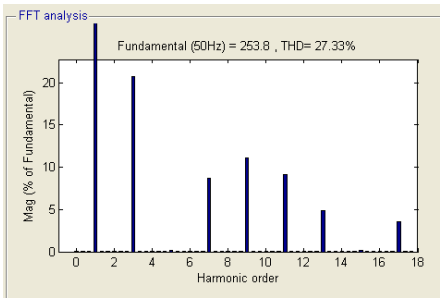

Figure 4c. FFT ANALYSIS FOR VOLTAGE

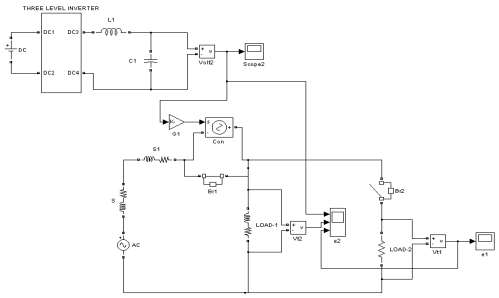

Figure 5a. DVR WITH LC FILTER

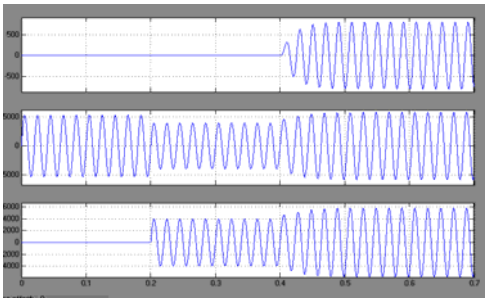

Figure 5b. VOLTAGE ACROSS EXTERNAL, LOAD-1 &LOAD-2 WAVEFORMS

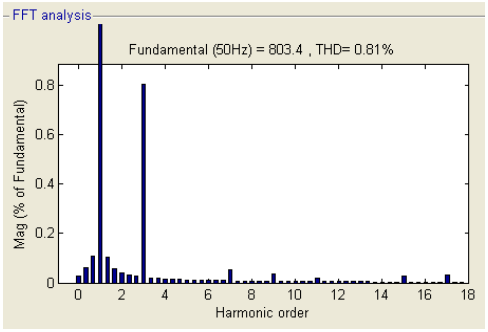

Figure 5c. FFT ANALYSIS FOR VOLTAGE

4. CONCLUSION

This paper presents circuit modelling and simulation of DVR using cascaded three level inverter. The pulses given to the inverter-II are shifted by 36^0 with respect to the pulses given to the inverter-I to reduce the harmonics.This paper demonstrates the capability of DVR to improve the voltage quality. Two different DVR structures are studied and the corresponding results are presented. It is better to use a filter in the output of inverter to reduce heating.

The simulation is based on the assumption of balanced load and single phase circuit model is considered. The simulation results are in line with the predictions.

5. REFERENCES:

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BIOGRAPHY:

S.Leela received her BE degree in Electrical & Electronics Engineering from Bharathidasan University, Trichy in 1990 and she received her ME degree in Power Electronics and Industrial Drives from Sathyabama Institute of Science and Technology, Chennai in the year 2006. She is a research scholar of Bharath University, Chennai. Currently, she is an Assistant Professor at Trichy Engineering College, Trichy. Her interests are in power quality improvement.

Dr. S.S. Dash received the ME in Power Systems from U.C.E, Orissa , in 1996. He received the Ph.D. degree in Electrical Engineering from Anna University, Chennai in 2006. Currently, he is a professor at SRM University, Chennai. His research interests include Power Systems, Power Electronics and Power Quality Improvement.