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ANALYSIS OF SHIFT REGISTER USING INTEGRATED POWER AND CLOCK DISTRIBUTION NETWORK BASED MASTER SLAVE FLIP FLOP

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ABSTRACT

The increase in integrated circuit design complexity density and performance, specifically in 3-D integration, requires more complicated power, ground, and clock distribution network. This network consumes a large portion of the limited on-chip metal resources. In digital ICs, the clock distribution network (CDN) distributes the clock signal, which acts as a timing reference within the system. Since the clock signal is heavily loaded, has the highest capacitance and operates at high frequencies, the CDN consumes a large amount of the total power in synchronous systems. The integrated power and clock distribution network (IPCDN) is used to reduce the metal requirements, routing complexity, and power. The IPCDN is proposed in order to eliminate the need for the global and local clock distribution network. In IPCDN, a differential power clock signal with a suitable dc voltage level and sinusoidal voltage-swing clock from the differential positive power clock and negative power clock signals. IPCDN does not require any change to be made to the conventional combinational and sequential circuit design. The element of IPCDN, including the LC differential power clock signal driver and the clock buffer, have been simulated using Taiwan semiconductor manufacturing company 65-nm CMOS technology with a power clock signal, a 1-volt dc component, and 400-mv sinusoidal swing at a frequency of 5 GHz. The behaviour of a master slave flip flop with IPCDN was integrated at extreme corners. From these results we can implement this master slave flip flop in the shift register applications and compare the results with respect to shift register based on normal master slave flip flop.

Keywords : *Clock Buffer, Clocked Inverter (Domino Logic), Combinational, Pass Transistor, Distribution Network, LC Differential Driver, Power–Clock, Sequential.*

1. INTRODUCTION

In digital integrated circuits, design complexity is more and also requires more power and area. Mainly in 3-D integration designs, the clock distribution network (CDN), act as a time reference within the system. It has high frequencies and heavily loaded clock signals and highest capacitance. In recent developments of 3-D integration multiplane synchronization is required, for that metal has over head and require more power .To eliminate the CDN, globally integrated power and clock (GIPAC) distribution network was proposed [5]. In GIPAC the local power and local clock is separated the integrated power and clock by using low-pass and high pass filters. The entire CDN, global and local is eliminated by using the integrated power and clock distribution network (IPCDN).Basically the CDN require four metal layers for GIPAC and six metal layers to distribute the power and clock. In IPCDN, giving the Pwr_clk+ and Pwr_clk- to the circuit, and reduce the area and power and routing .for the power clock signal generated by the LC differential driver, a clock buffer is needed. In order to extract a full-swing clock signal to feed the clock port in sequential elements. In circuit design, the pass transistors and domino logic is use for reduce power and area and routing complexity.

2. IPCDN

The power clock signal has generated from the driver directly to the VDD port in combinational and sequential elements. The full swing of clock signal extracted from the clock buffer. . The arrows in Figure3 represent the flow of current when the inverter is charging (I_R) or discharging (I_F) a load capacitance through the TG. We can break the connection between the inverter cells and use the

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circuit of Figure 2, without substantially affecting the operation of the circuit. The symbol for the clocked inverter shown in Figure 2 is common, but by no means a standard. We can use the clocked inverter to replace the inverter–TG pairs in latches and flip-flops. For example, we can replace one or both of the inverters I1 and I3 (together with the TGs that follow them) in Figure 3 by clocked inverters. There is not much to choose between the different implementations in this case, except that layout may be easier for the clocked inverter versions (since there is one less connection to make).

More interesting is the flip-flop design: We can only replace inverters I1, I3, and I7 (and the TGs that follow them) in Figure 3 by clocked inverters. We cannot replace inverter I6 because it is not directly connected to a TG. We can replace the TG attached to node M with a clocked inverter, and this will invert the sense of the output Q, which thus becomes QN. Now the clock-to-Q delay will be slower than clock-to-QN, since Q (which was QN) now comes one inverter later than QN. If we wish to build a flip-flop with a fast clock-to-QN delay it may be better to build it using clocked inverters and use inverters with TGs for a flip-flop with a fast clock-to-Q delay. In fact, since we do not always use both Q and QN outputs of a flip-flop, some libraries include Q only or QN only flip-flops that are slightly smaller than those with both polarity outputs. It is slightly easier to layout clocked inverters than an inverter plus a TG, so flip-flops in commercial libraries include a mixture of clocked-inverter and TG implementations.

They have smaller areas than conventional CMOS logic (as does all Dynamic Logic).Parasitic capacitances are smaller so that higher operating speeds are possible. Operation is free of glitches as each gate can make only one transition. Only non-inverting structures are possible because of the presence of inverting buffer. The largest difference between static and dynamic logic is that in dynamic logic, a clock signal is used to evaluate combinational logic. However, to truly comprehend the importance of this distinction, the reader will need some background on static logic.

In most types of logic design, termed static logic, there is at all times some .mechanism to drive the output either high or low. In many of the popular logic styles, such as TTL and traditional CMOS, this principle can be rephrased as a statement that there is always a low-impedance DC path between the output and either the supply voltage or the ground. As a side note, there is of course an exception in this definition in the case of high impedance outputs, such as a tri-state buffer; however, even in these cases, the circuit is intended to be used within a larger system where some mechanism will drive the output, and they do not qualify as distinct from static logic.

In contrast, in dynamic logic, there is not always a mechanism driving the output high or low. In the most common version of this concept, the output is driven high or low during distinct parts of the clock cycle. During the time intervals when the output is not being actively driven, its impedance causes it to maintain a level within some tolerance range of the driven level.

Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used or refreshed before the charge in the output capacitance leaks out enough to cause the digital state of the output to change, during the part of the clock cycle that the output is not being actively driven.

Static logic has no minimum clock rate the clock can be paused indefinitely. While it may seem that doing nothing for long periods of time is not particularly useful, it leads to two advantages:

- Being able to pause a system at any time makes debugging and testing much easier, enabling techniques such as single stepping.
- Being able to run a system at extremely low clock rates allows low-power electronics to run longer on a given battery.

Being able to pause a system at any time for any duration can also be used to synchronize to asynchronous events. (While there are other mechanisms to do this, such as interrupts, polling loops, processor idling input pins [like RDY on the 6502], or processor bus cycle extension mechanisms such as WAIT inputs, using hardware to gate the clock to a static-core CPU is simpler, is more temporally precise, uses no program memory and does not consume power in the CPU while it is waiting. In a basic design, for starting to wait, the CPU writes to the register to set a binary latch bit which would be AND ed or ORed with the clock, stops the processor. A signal from a peripheral device resets the latch and resumes the operation of CPU. The hardware logic must gate the latch control inputs as necessary to ensure that a latch output transition causes the clock signal level to instantaneously neither high nor low. In particular,

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although many popular CPUs use dynamic logic only static cores CPUs designed with fully static technology are usable in space satellites due to their higher radiation hardness .Most satellites do not use CMOS circuits anyway; gallium arsenide is more popular in these applications.

Dynamic logic if designed properly can be more than twice faster than static also it uses o the fast N number of transistors, which makes the transistor sizing optimizations better. Static logic resembles slow due to it's twice the capacitive loading, higher thresholds, and uses slow P transistors for logic. Dynamic logic can be harder to work with, but it may be the only choice when increased processing speed is needed. Most electronics running at over 2 GHz these days requires the dynamic logic, although manufacturers like Intel have completely switched to static logic to reduce power consumption. Note that reducing power use not only extends the running time with limited power sources such as batteries or solar arrays but also decreases the thermal design needs, reducing the size of needed heat sinks, fans, etc., which in turn reduces system weight and cost.

In general, dynamic logic greatly increases the number of transistors that are switching at any instant that improves power requirement compared to static CMOS. There is several power saving techniques that can be implemented in a dynamic logic system. Each rail conveys a number of bits, and there are no glitches. Power saving and asynchronous techniques are much more natural in dynamic logic.

3. PROPOSED PASS TRANSISTOR

Pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. This decreases the number of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes, for switches directly connected to supply. This decreases active devices number, instead has the drawback that difference of the voltage between high and low logic levels decreases. Transistor that is in series is lightly saturated at the output compared to the input. When more devices are put in a chain in series in a logical path, a constructed gate will be necessary to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply, so logic levels in the sequential chain does not reduces. As the isolation between input signals and outputs are less, it is required to take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the sequence of circuits, hence charge sharing, sneak paths, and also slow switching speed can be avoided. Simulation of circuits may be required to ensure adequate perform.

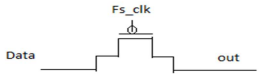

Figure 1: Pass Transistor

The pass transistor is driven by a periodic clock signal and act as an access switch to either charge up or down the parasitic capacitance CX depending on the input signal Vin .It having the two operation mode logic 1 and logic 0.static and dynamic types of pass transistor logic with different properties with respect to speed ,power and low-voltage operation .the disadvantages of pass transistor logic become significant ,the threshold voltage of transistors becomes large compared to supply voltage.

B. proposed domino logic

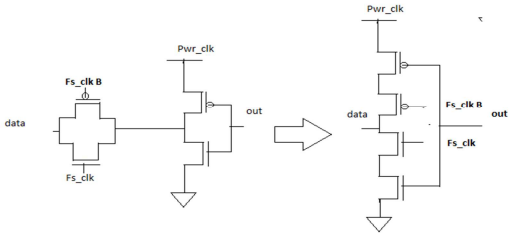

Figure 2: Clocked Inverter

The structure of a clocked inverter from the series combination of inverter and a transmission gates are shown in the figure. . In fact, since we do not always use both Q and QN outputs of a flip flops, few libraries consists of Q only or QN only flip flops that are slightly smaller than those with both polarity outputs. layout of clocked inverters are easier to implement than an inverter pulse transmission gate, so flip flop in commercial libraries include a mixture of clocked inverter and transmission gate implementations. They have smaller area than conventional CMOS logic .parasitic capacitances are smaller so that higher operating speed are possible .The proposed method having two advantages, one is being able to pause a system at any time and makes debugging and testing easier, techniques for enabling like single stepping. Second is run a system at extremely low clock rate allows low-power electronic to run longer on a given battery.

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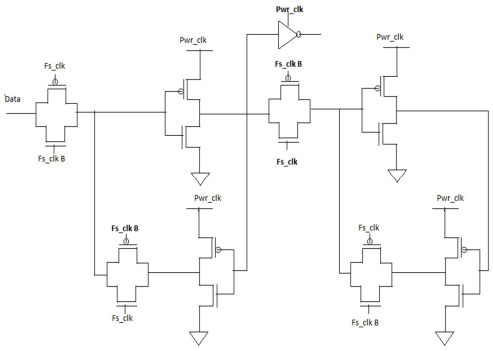

Figure 3: Master-Slave Flip-Flop With IPCDN.

The operation of LC differential driver was investigated with a network capacitance of 8pf, for which a 127-ph inductor is needed in order to generate a power clock signal with an oscillating frequency of 5 GHz [1]. The 5 GHz full swing clock signal is extracted from the power clock using the proposed clock buffer. Both output signals are give to the transmission gate inputs (Fs-clk and Fs-clkB) and the power clock signal is given instead of VDD, the remaining performance of the circuit is act as a Master slave flip flop.

4. METHODOLOGY USED

The performance of the proposed system is high compared with existing system. In that according to the pass transistor logic the power dissipation is less, but the pass transistor logic having only NMOS mode and it is working for high data input. The operation of the LC differential driver was investigated with a network capacitance of 8 pF, for which a 127-pH inductor is needed in order to generate a Pwr_Clk signal with an oscillating frequency of 5 GHz. The width of the PMOS/NMOS transistors in the driver was equal to 40/20 *W*min, where *W*min is the minimum allowable width for a transistor in the 65-nm technology which is equal to 120 nm. The pulse width of the reference signal VREF1 is 70 ps.

The extraction of a 5-GHz full-swing clock signal from the *Pwr_Clk*using the proposed clock buffer is shown in Fig. 2. Since the *Pwr_Clk* signals are applied to the gates of the pass transistors MN5 and MN6, nodes X and Y reach the highest voltage level as the *Pwr_Clk*+ and *Pwr _Clk*− signals reach it, respectively. The output inverters generate full-swing clock signals FS_CLK and FS_CLKB with sharp edges as illustrated in the figure. All the PMOS and NMOS transistors used in the clock buffer were minimum-sized transistors. As shown in the figure4, *Pwr_Clk*is directly connected to the *V*DDport of the flip-flop. The clock ports are connected to the FS_CLK and FS_CLKB signals generated from the clock buffer. In order to investigate the behaviour of the master-slave flip-flop IPCDN at a frequency of 5 GHz, the output of the flip-flop was simulated with power supplies of 1.2, 1, and 0.8 V and the *Pwr_Clk* signal. For the same *T*setup, the *T*CLKQ varies by approximately 18 ps between the 1.2 and 0.8 V power supplies. The flip-flop with IPCDN is around 6 ps faster as compared to that with the 0.8-V supply.

Proposed method-I

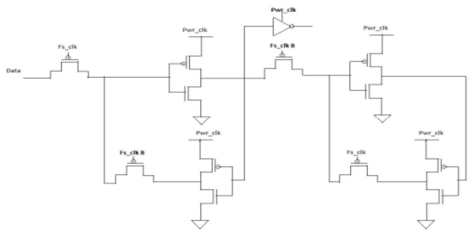

Fig.4: Master Slave Flip Flop Using Pass Transistor Logic With IPCDN

With this logic area, power and routing complexity is reduced. Another master slave flip flop was designed with clocked inverter or domino logic .The performance of master slave flip flop is same as existing system, but area and power was reduced. Considering that the system is better than the existing system.

Proposed method-II

Second proposed system is

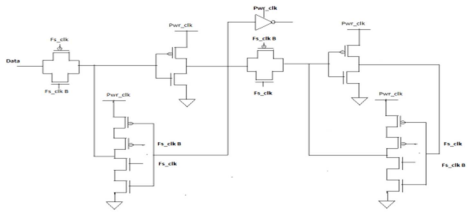

Figure 5: Master Slave Flip Flop Using Clocked Inverter Logic With IPCDN

In this method, the logic has changed, and the same method followed by the flip flop .The logic used is domino logic or clocked inverter logic and 5%of power and area are reduced using this logic. The operation of the LC differential driver was investigated with a network capacitance of 8 pF, for which a 127-pH inductor is needed in order to generate a *Pwr_Clk*signal with an oscillating frequency of 5 GHz. The width of the PMOS/NMOS transistors in the driver was equal to 40/20 *W*min, where *W*min is the minimum allowable width for a transistor in the 65-nm

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technology which is equal to 120 nm. The pulse width of the reference signal VREF1 is 70 ps.The extraction of a 5-GHz full-swing clock signal from the *Pwr_Clk*using the proposed clock buffer is shown in Fig. 2. Since the *Pwr_Clk* signals are applied to the gates of the pass transistors MN5 and MN6, nodes X and Y reach the highest voltage level as the *Pwr_Clk*+ and *Pwr _Clk*− signals reach it, respectively. The output inverters generate full-swing clock signals FS_CLK and FS_CLKB with sharp edges as illustrated in the figure9. All the PMOS and NMOS transistors used in the clock buffer were minimum-sized transistors. As shown in the figure4, *Pwr_Clk*is directly connected to the *V*DD port of the flip-flop. The clock ports are connected to the FS_CLK and FS_CLKB signals generated from the clock buffer. In order to investigate the behaviour of the master-slave flip-flop IPCDN at a frequency of 5 GHz, the output of the flip-flop was simulated with power supplies of 1.2, 1, and 0.8 V and the *Pwr_Clk* signal. For the same *T*setup, the *T*CLKQ varies by approximately 18 ps between the 1.2 and 0.8 V power supplies. The flip-flop with IPCDN is around 6 ps faster as compared to that with the 0.8-V supply.

The master slave flip flop power consumption with IPCDN is 2µw which is 34% less than the case with the 1-v power supply. However, this reduction in power was overcome by the power consumption of the clock buffer required with IPCDN which is around twice the power of the flip flop. The power of the clock buffer was reduced by sharing the clock buffer between three flip fops with a penalty of reducing the peak of the generated clock signal to 750mv.the power consumption of the master slave flip flop with the shared clock buffer exhibits 43% increase compared to the case with IV power supply.

Table.1: Performance Analysis Of Methods

Methods	Power dissipation	Delay
Existing method	2794.046mw	83ns
Proposed method 1	2741.348mw	86ns
Proposed method 2	2738.041mw	85ns

Table represents the performance analyses of existing, proposed method 1 and proposed method II.All the three methods have given different power and delay values .Comparing the three systems the power and area are reduced in both clock inverter logic and domino logic .In shift register application also performance of both the systems are same ,but power and area are reduced.

5. SIMULATION RESULTS

A. EXISTING METHOD MASTER SLAVE FF:

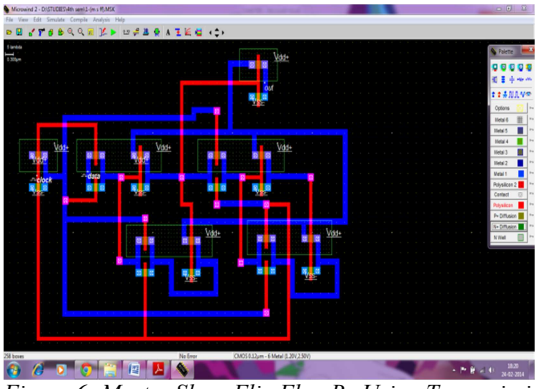

Figure 6: Master Slave Flip Flop By Using Transmission Gate

Output waves:

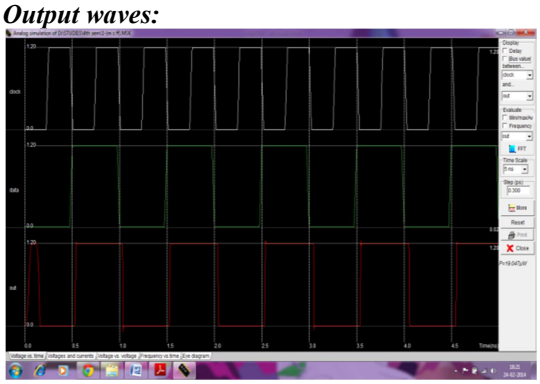

Figure 7: Out Waves For Master Slave FF By Using Transmission Gate

B. PROPOSED METHODS:

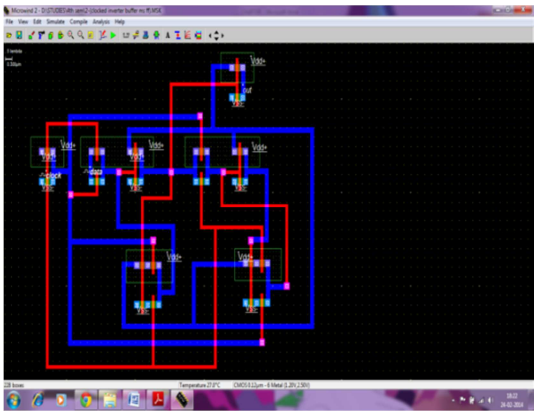

Figure8: master slave flip flop by using clocked inverter

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Output waves:

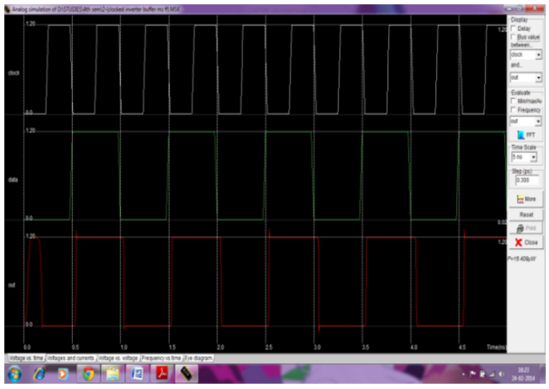

Figure9: Output Waves- Master Slave Flip Flop By Using Clocked Inverter

Proposed method 1:

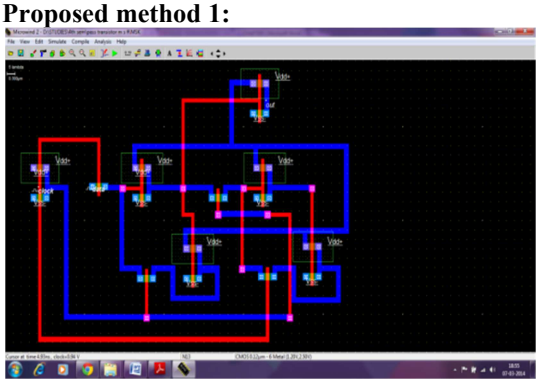

Figure10: Master Slave Flip Flop By Using Pass Transistor Logic

Output waves:

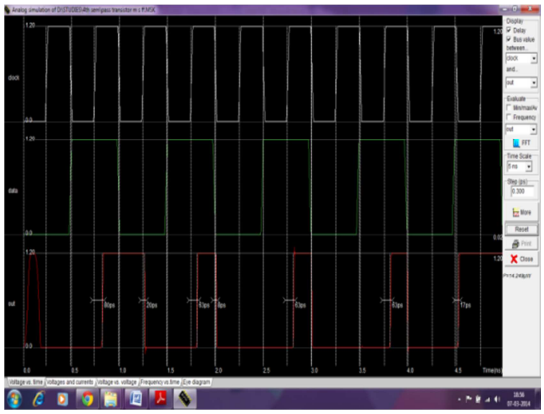

Figure11: Output Waves For Master Slave Flip Flop By Using Pass Transistor

Master slave ff with IPCDN:

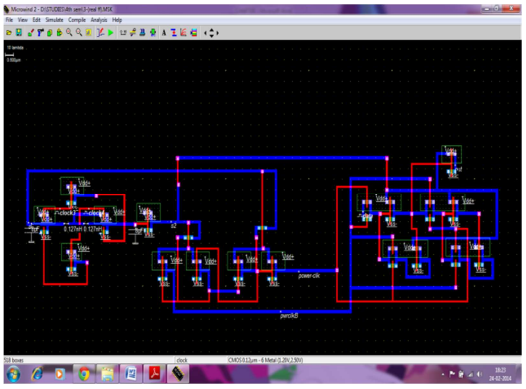

Figure12: Master Slave Flip Flop By Using With IPCDN

Output waves:

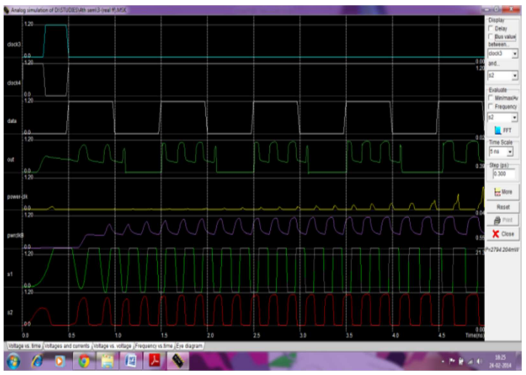

Figure13: Output Waves For Master Slave Flip Flop By Using With IPCDN

Master slave ff with IPCDN modified:

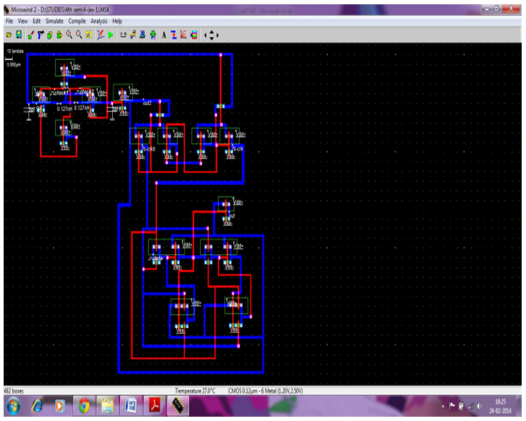

Figure14: Master Slave Flip Flop By Using Clocked Inverter With IPCDN

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Output waves:

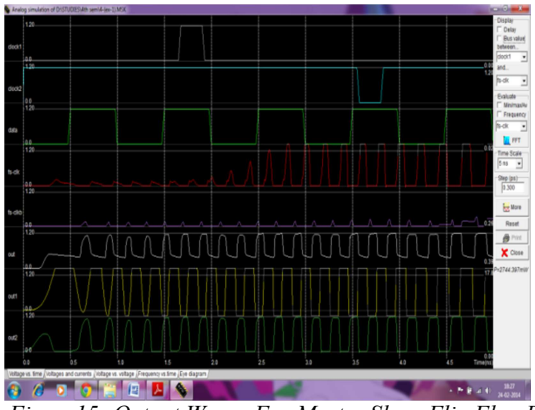

Figure15: Output Waves For Master Slave Flip Flop By Using Clocked Inverter With IPCDN

Proposed methods II:

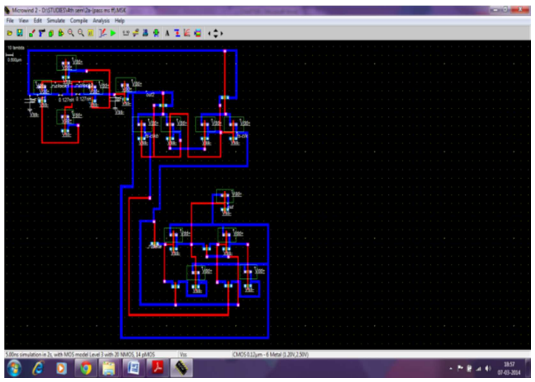

Fig.16: Master Slave Flip Flop By Using Pass Transistor IPCDN

Output waves:

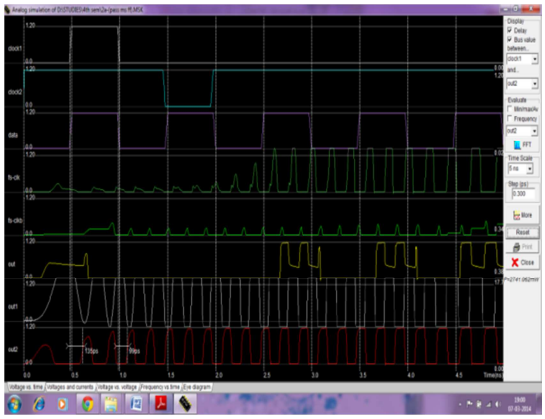

Figure17: Output Waves- Master Slave Flip Flop By Using Pass Transistor IPCDN

C.Applications:

Shift registers (SISO):

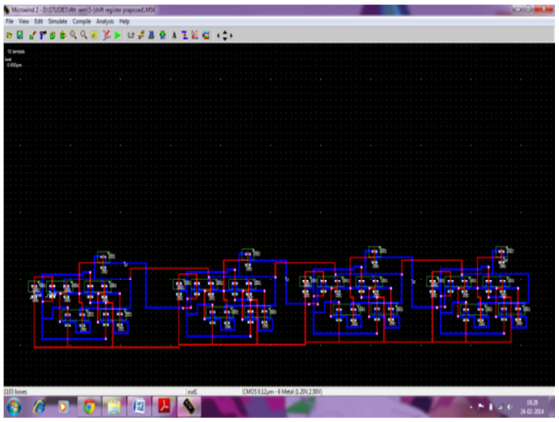

Figure18: Master Slave Flip Flop By Using Transmission Gate

Output waves:

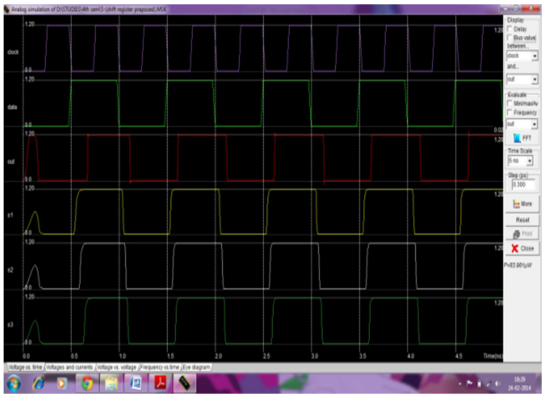

Figure19: Output Waves- Master Slave Flip Flop By Using Transmission Gate

Proposed application 1:

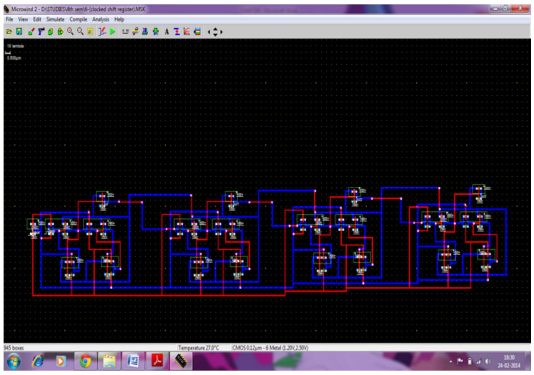

Figure 19: Master Slave Flip Flop By Using Clocked Inverter

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Output waves:

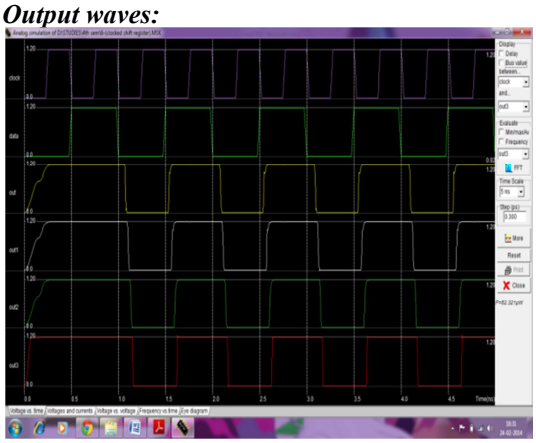

Figure20: Output Waves Master Slave Flip Flop By Using Pass Transistor

Proposed application 2:

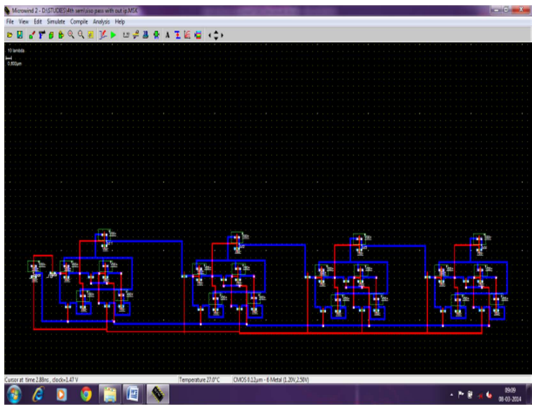

Figure21: Master Slave Flip Flop By Using Pass Transistor

Output waves:

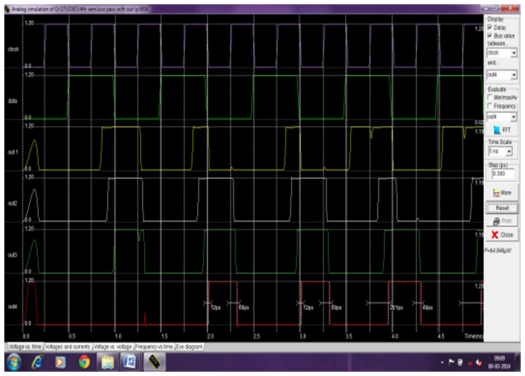

Figure 22: Output Waves Master Slave Flip Flop By Using Pass Transistor

Siso proposed pass transistor logic:

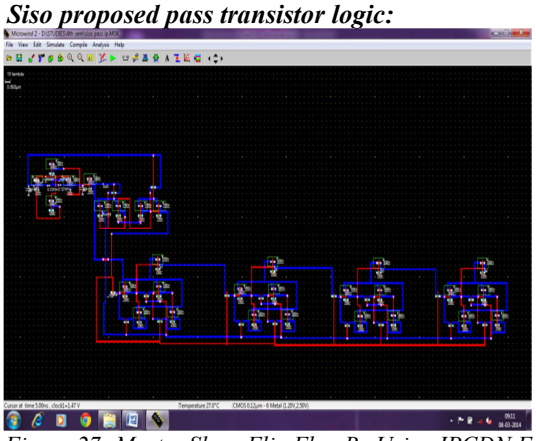

Figure 27: Master Slave Flip Flop By Using IPCDN For PIPO

Output waves:

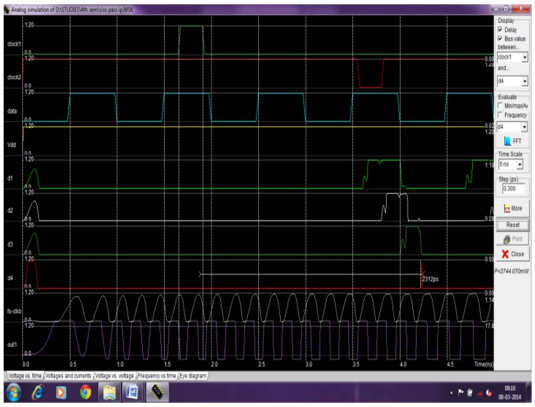

Figure 28: Output Waves Master Slave Flip Flop By Using IPCDN For PIPO

PIPO for proposed clocked inverter:

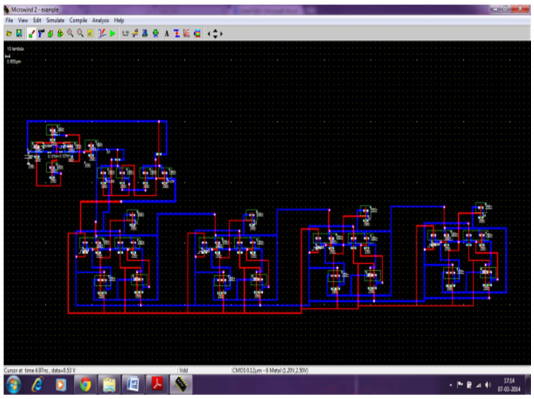

Figure 31: Master Slave Flip Flop By Using CI With IPCDN For PIPO

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Output waves:

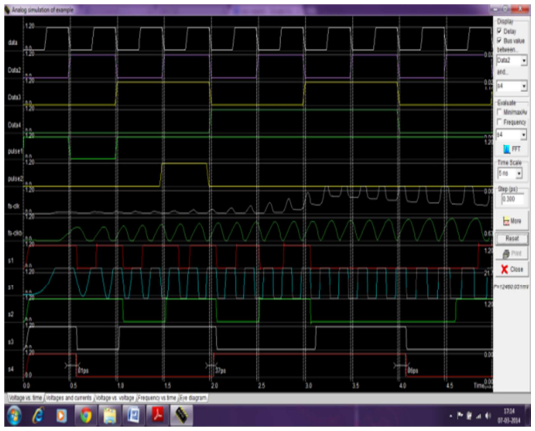

Figure 32: Output Waves Master Slave Flip Flop By Using CI With IPCDN For PIPO

PIPO for proposed pass transistor:

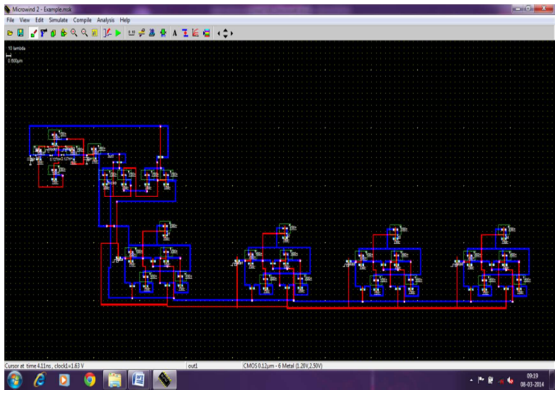

Figure 33: Master Slave Flip Flop By Using PS With IPCDN For PIPO

Output waves:

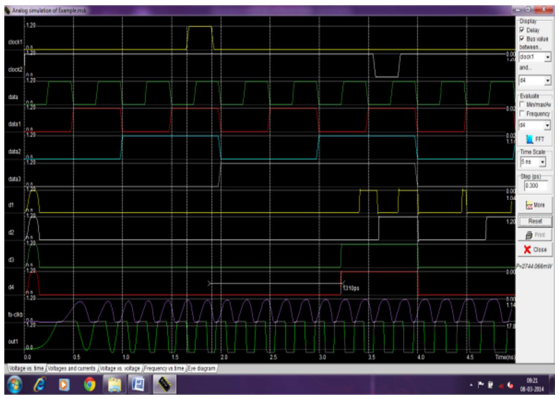

Figure 34: Output Waves Master Slave Flip Flop By Using PS With IPCDN For PIPO

6. CONCLUSION

The number of flip-flops and the size of the network are dependent on each system. The percentage of power reduction achieved with IPCDN is less compared to that achieved with the square-wave CDN as a function of the clock capacitance (*CCLK)* and the number of flip-flops (*N)*. Simulation results showed correct operation of the LC differential clock driver and clock buffer with TSMC 65-nm CMOS technology at a frquency of 5 GHz. In order to satisfy high current requirements, several LC drivers are distributed to drive different blocks. This would increase area overhead associated with the inductors. Implementing inductors on top of active metal layers can reduce the area overhead with a penalty of reduced quality factor. Magnetic inductors are another alternative to reduce area. Comparing IPCDN to a buffered square-wave CDN illustrates that IPCDN achieves around 20% reduction in power when the network is heavily loaded. In IPCDN the power and clock has been given as one signal, and generated by the circuits. In master slave flip flop instead of transmission gate it was changed using different logic gates. Hence, area, power and routing complexity are reduced using IPCDN network. Comparing the transmission, pass transistor logic and domino logic power and area was reduced.

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