Journal of Theoretical and Applied Information Technology
10th August 2015. Vol.78. No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

SIMULATION AND COMPARISON OF SPWM AND SVPWM CONTROL FOR TWO LEVEL UPQC

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ABSTRACT

Unified Power Quality Conditioner (UPQC) is an effective tool to solve the power quality problems. The main purpose of UPQC is to compensate harmonics present in the utility voltage and source current. The UPQC has the ability of improving the power quality at the point of installation in power distribution systems. This paper discusses unit vector template generation control strategy with a focus to mitigate harmonics present in the utility voltage. The main aim of this paper is to evaluate the performance of two level voltage source converter(VSC) based UPQC for effective harmonic reduction in the load voltage and source current when adopted Sinusoidal Pulse Width Modulation(SPWM) and Space Vector Pulse Width Modulation (SVPWM). The adoption of SVPWM technique allows better compensation of load voltage and source current harmonics. Simulation results based on MATLAB/ SIMULINK are presented to verify effective compensation of voltage and current harmonics when adopted SVPWM technique.

Keywords: *Power Quality, Harmonics, UPQC, Pulse Width Modulation, MATLAB / SIMULINK.*

1. INTRODUCTION

The increased number of electronic equipment required by industry and residential applications pose a serious problem in electrical systems as these devices require high quality supply. These power electronic based loads are responsible for injecting harmonics into the system[1].

Power electronic based devices are compact in size and also offers better controllability , higher efficiency. But, because of the switching actions, these devices behave as non-linear loads and inject harmonics into the network, when connected to the system[2]. It is very important to compensate voltage harmonics as these have been serious in power systems. All these days, passive filters and capacitors were used to filter these harmonics.

With the advent of advanced power electronic technology, devices to mitigate power quality problems have been developed. One of such device is Unified Power Quality Conditioner which is a combination of series and shunt active filters connected back to back through a common dc link[3]. With this combination, it is possible to achieve compensation of supply voltages and load currents simultaneously. Hence, the voltage supplied to the load and current drawn from the supply are sinusoidal and balanced.

The major contribution in this work was to assess the performance of two level VSC based UPQC when adopted SPWM and SVPWM techniques for effective compensation of harmonics in load voltage and source current as per the standards of IEEE-519 which are reflected for Non-linear loads. Finally , the relative performance of the two control techniques is studied.

2.GENERAL UPQC

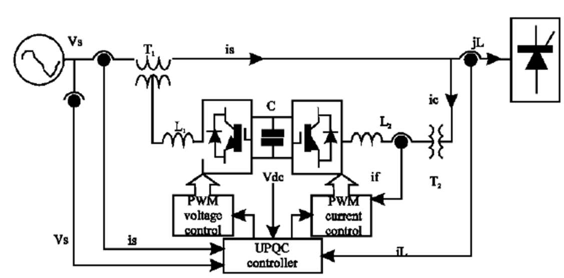

Fig.1 : General Arrangement Of UPQC

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

Fig.1 shows a basic block diagram of UPQC. The two active filters based on voltage sources converters principle are connected back to back with a common dc link. The inverter connected in shunt with the load acts like a Shunt Active Power Filter (SAPF) compensates load current harmonics while maintaining the dc link voltage constant. The other inverter is connected in series with the utility grid and maintains the load voltage constant. Thus, UPQC is capable of improving the power quality at the point of common coupling in the power system. Hence, it is considered to be one of the important solution for large capacity loads that are sensitive to voltage harmonics[4].

3. CONTROL STRATEGY FOR UPQC

Unit Vector Template generation is used to generate the reference signals for shunt and series APFs [5].The input voltage at PCC contains fundamental as well as distorted components. The unit input vector U_S is obtained by multiplying the sensed input voltage by a gain of $1/V_m$, where V_m is the peak amplitude of fundamental of the input voltage. After taking these unit voltage vectors to phase locked loop (PLL), unit vector templates are generated by considering proper phase delay.

$$\mathbf{U_a=\sin\omega t}$$

$$\mathbf{U_b=\sin(\omega t-120^{\circ})} \qquad \textbf{(a)}$$

$$\mathbf{U_c=\sin(\omega t-240^{\circ})}$$

The reference load voltage signals are generated by multiplying the above unit vectors with peak amplitude of fundamental input voltage such that $\mathbf{V_{labc}{*}=V_m.U_{abc}}$

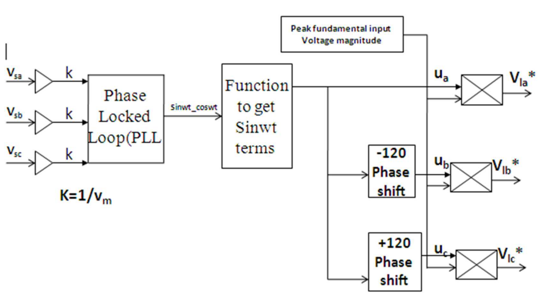

Fig.2 Extraction Of Unit Vector Templates And Reference 3-Phase Load Voltages

In order that the load voltage is distortion-less, load voltage must be equal to the above reference signals. For this, the load voltages are compared with reference voltages and the error is processed though a PWM generator to generate signals for series APF [5].

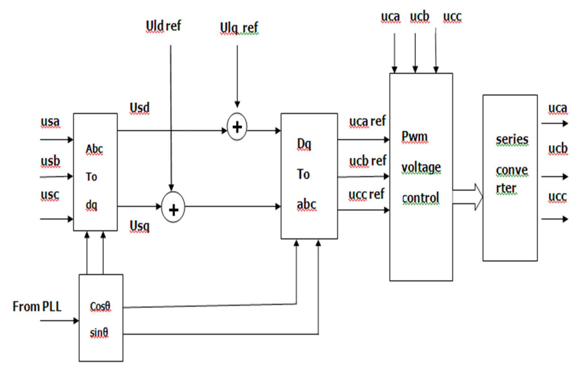

Fig: 3 Control Block Diagram Of The Series Converter Of The UPQC

In the similar manner, the unit vector template can be applied even for shunt APF in order to compensate the current harmonics generated by nonlinear loads.

In order that the shunt APF compensates current harmonics and maintains the dc link voltage constant , the sensed dc link voltage is compared with reference dc voltage and the error is processed through a PI controller.

The output of PI controller is multiplied by vector templates to generate reference current signals. In order that the source current is free from distortions, it must follow the reference current signal. For this , the source currents are compared with reference currents and the generated error is processed through a PWM controller to generate gate signals for shunt APF [5].

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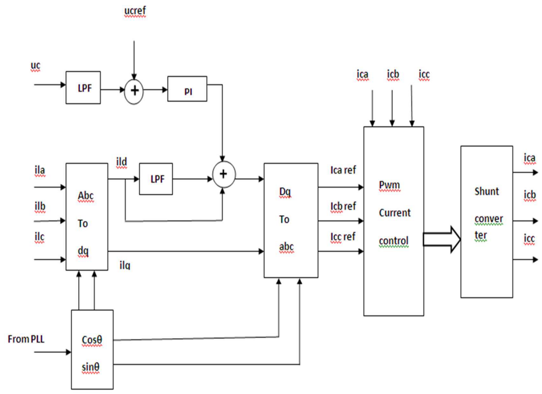

Fig4: Control Block Diagram Of The Shunt Converter Of The UPQC

4. CONTROL TECHNIQUES FOR UPQC:

A) Sinusoidal Pulse Width Modulation:

In this modulation technique, sinusoidal reference signal at 50Hz is compared with high frequency carrier signal (triangular waveform) . Whenever the reference signal is greater than carrier signal , three switches out of six are turned ON and the other three switches will remain in OFF position. Similarly, when the reference signal is less than the triangular signal , then the switches which are in OFF position are turned ON and the counter switches will go to OFF state. The modulation index depends on the magnitude of the reference signal.

B)Space Vector Pulse Width Modulation:

The Space Vector Pulse Width Modulation (SVPWM) method is more popular than conventional modulation techniques and can be easily implemented using digital processors.

SVPWM have better utilization of the DC link voltage, less commutation losses and higher efficiency. Because of its superior characteristics, it is finding wide spread application[6], [7].

The set of balanced three phase voltages can be represented in a stationary reference frame by a space vector of magnitude equal to the amplitude of voltages and rotating at an angular speed of $\omega=2\pi f_{REF.}$

In a given switching cycle, the rotating reference vector is approximated by switching between two nearest active vectors and null vectors. In order to maintain minimum switching frequency of the power devices, the sequence of toggling of vectors is arranged such that only one leg is affected for each step.

The status of the switches being ON or OFF can be known from the location of the reference vector in αβ - plane. The eight possible switching states of the inverter are represented as six active vectors and two null vector forming a hexagon.

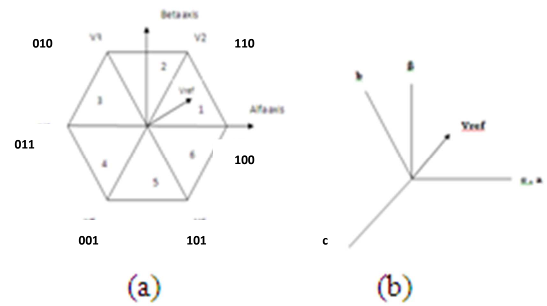

Fig.5 (A) Space Vector Diagram For 2 Level Inverter (B) Reference Vector In abc And αβ Planes.

Table 1: Voltage Vectors Created From Different Combination Of The Switches

Voltage vectors	Switching vectors	Vector classification
V0	000	Zero State
V1	100	Active State
V2	110	Active State
V3	010	Active State
V4	011	Active State
V5	001	Active State
V6	101	Active State
V7	111	Zero State

For the upper switches, 1 means OFF, 0 means ON. The lower switches forms complementary to the upper switches and hence possible combinations of the switching states are : 000, 001, 010, 011, 100, 110, 110, 111. There are 8 possible switching states in which six are active states and the balance two are the null switching

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states. The active vectors are represented as V1-V6 and are placed at the corners of the hexagon while zero vectors denoted as V0 & V7 are positioned at the origin.

The three-phase system is assumed to be balanced:

$V_{a0}+V_{b0}+V_{c0} = 0$

The instantaneous phase voltages are:
Va = V sin (θ)
Vb = V sin (θ+2π/3)
Vc = V sin (θ+4π/3)
With the help of Clark's transformation, the magnitude and angle of the rotating vector represented by
Vref = V α + jVβ can be found as

$$\text{magnitude} = |Vref| = \sqrt{V\alpha^2 + V_\beta^2}$$

$$\text{and angle } \theta = \tan^{-1}\frac{V\alpha}{V\beta}$$

The reference voltage can also be expressed as

$$V\alpha + jV_\beta = [\ v_a + v_b e^{j2\pi/3} + v_c e^{-j2\pi/3}\ ]$$

The voltage vectors in α -β plane can be expressed as

$$\begin{pmatrix} V\alpha \\ V\beta \end{pmatrix} = 2/3 \begin{pmatrix} 0 & \cos 2\pi/3 & -\cos 2\pi/3 \\ 1 & \sin 2\pi/3 & -\sin 2\pi/3 \end{pmatrix} \begin{pmatrix} Va \\ Vb \\ Vc \end{pmatrix}$$

$$V\alpha = 2/3(va - 1/2vb - 1/2vc)$$

$$V\beta = 2/3(\sqrt{3}/2vb - \sqrt{3}/2vc)$$

The time duration of vectors V_1 to V_6 can be calculated with the help of following general expression:

$$T_1 = \frac{\sqrt{3}\, T_Z\, V_{ref}}{V_{dc}}\left(\sin\left(\frac{n\pi}{3} - \alpha\right)\right)$$

$$T_2 = \frac{\sqrt{3}\, T_Z\, V_{ref}}{V_{dc}}\left(\sin\left(\alpha - \frac{n-1}{3}\pi\right)\right)$$

$$T_0 = T_Z - T_1 - T_2$$

Where n= 1 through 6 (sector number), $0 \leq \alpha \leq 60^0$ and T_Z is the sampling time.

The following table indicates the switching times of each switch in different sectors

Table 2 : Switching Time Calculation At Each Sector

sector	Upper switches (S_1 S_3 S_5)	Lower switches (S_4 S_6 S_2)
1	S1 = T1 + T2 + T0 / 2 S3 = T2 + T0 / 2 S5 = T0 / 2	S4 = T0 / 2 S6 = T1 + T0 / 2 S2 = T1 + T2 + T0 / 2
2	S1 = T1+ T0 / 2 S3 = T1+T2 + T0 / 2 S5 = T0 / 2	S4 = T2+T0 / 2 S6 = T0 / 2 S2 = T1 + T2 + T0 / 2
3	S1 = T0 / 2 S3 = T1 + T2 + T0 / 2 S5 = T2 + T0 / 2	S4 = T1 + T2 + T0 / 2 S6 = T0 / 2 S2 = T1 + T0 / 2
4	S1 = T0 / 2 S3 = T1+ T0 / 2 S5 = T1 + T2 + T0 / 2	S4 = T1 + T2 + T0 / 2 S6 = T2 + T0 / 2 S2 = T0 / 2
5	S1 = T2 + T0 / 2 S3 = T0 / 2 S5 = T1 + T2 + T0 / 2	S4 = T1 + T0 / 2 S6 = T1 + T2 + T0 / 2 S2 = T0 / 2
6	S1 = T1 + T2 + T0 / 2 S3 = T0 / 2 S5 = T1+T0 / 2	S4 = T0 / 2 S6 = T1 +T2+ T0 / 2 S2 = T2 + T0 / 2

Space vector switching pattern for sector –I is shown in fig 6.

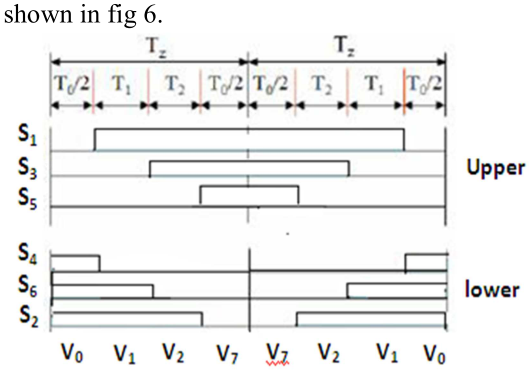

Fig .6 .Space Vector Switching Pattern Of Sector –I

We can deduce the switching patterns for other sectors also in the same manner.

At any instant, the combination of the upper/lower switch signals will give an 'M' shaped

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wave, which is compared with a triangular signal to give gate pulses to the switches in the converter.

5. SIMULATION RESULTS:

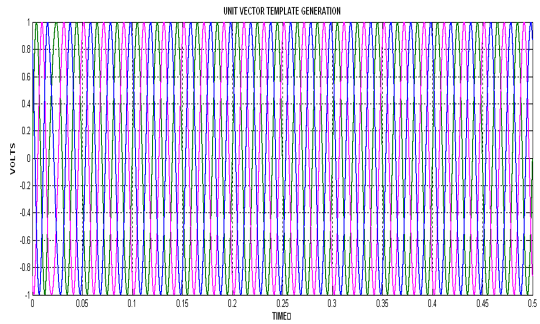

Fig. 7 . Unit Vector Template Generation

The fig.7 shows the unit-vector templates generated by using proposed control technique. It should be noted that, the unit vector template is pure sinusoidal because of use of Phase Locked Loop(PLL) and this template generation is useful to get accuracy in output.

In order to validate the performance of UPQC for mitigation of harmonics, 5th and 7th harmonics are deliberately injected into the source voltage. The UPQC system as shown in fig. 1 which is connected to a non-linear load is simulated using MATLAB/SIMULINK and the following results clearly show the response of UPQC.

a) Total Harmonic Distortion Analysis Of Load Voltage And Source Current Using Sinusoidal Pulse Width Modulation:

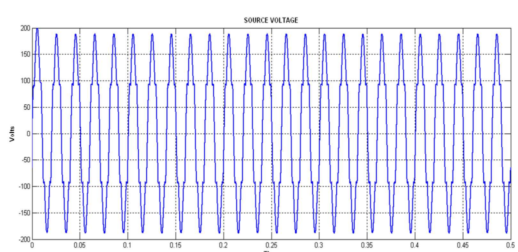

Fig.8. Source Voltage

Fig .8. shows source voltage where the 5th and 7th harmonics are deliberately injected into the source voltage to find the response of the UPQC.

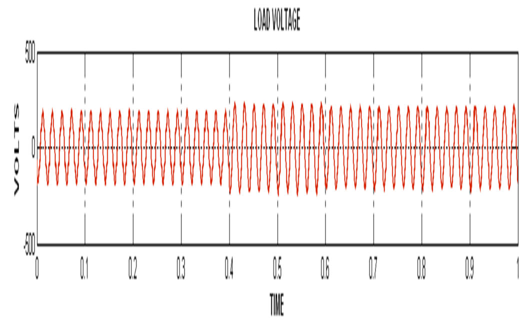

Fig.9. Load Voltage

In Fig.9, before 't=0.4s' when both APFs are not in operation, the load voltage is equal to the distorted input voltage with a total harmonic distortion (THD) of 12.33%.

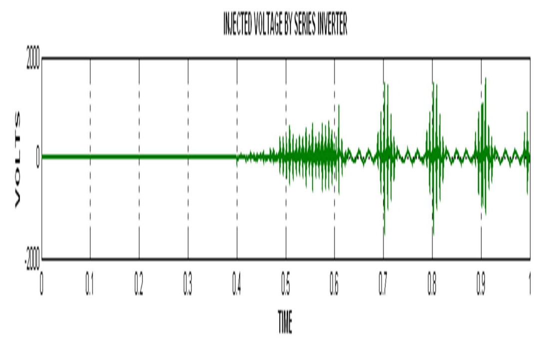

Fig. 10. Voltage Injected By Series Inverter

The series inverter is put into operation at 0.4sec and it immediately started compensating the load voltage by injecting voltage through series line transformer as shown in Fig.10. At time 't=0.6 sec' shunt active power filter is put in to operation such that THD of the load voltage is reduced to 4.32%. FFT analysis is done for load voltage before and after connecting UPQC.

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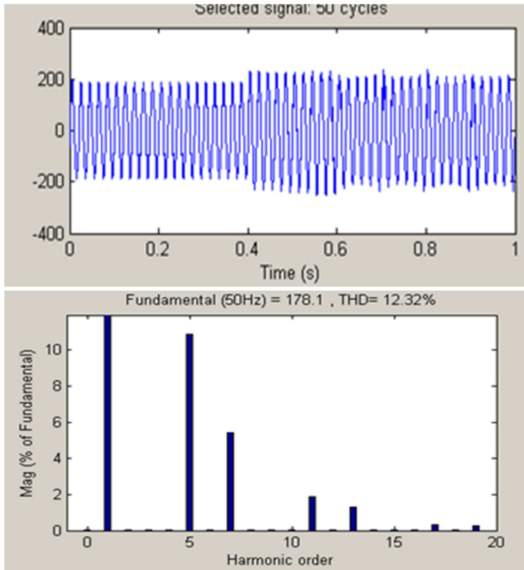
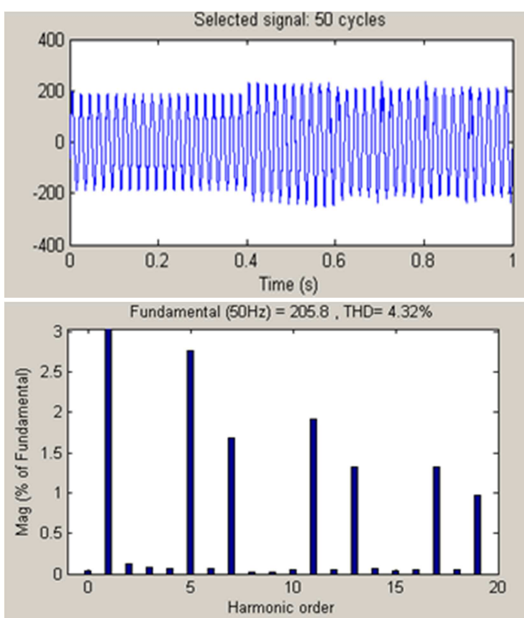
FFT Analysis Of Load Voltages:



FFT analysis is done for load voltage at 0.2sec, before switching ON both series and shunt filters where the load voltage is same as source voltage and THD is found to be 12.32%.



The FFT analysis is done at 0.8sec when both series and shunt filters are in operation and the measured THD is 4.32% which is well within the prescribed limits as per IEEE – 519 standards. It is very clear that there is a reduction of 65% in the measured THD after connecting UPQC.

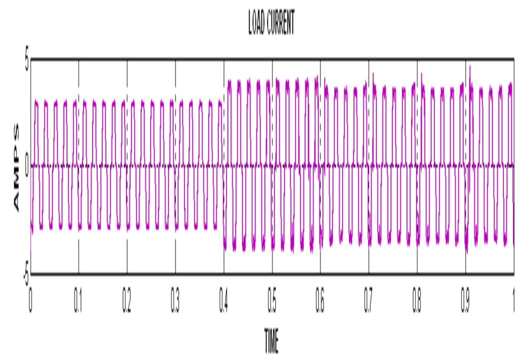


Fig. 11. Load Current

From Fig.11 , it is clear that the load current is distortional due to the non- linear load

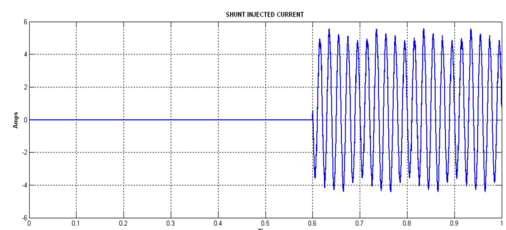


Fig. 12. Current Injected By Shunt Inverter

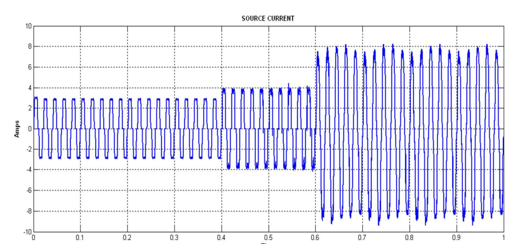


Fig. 13. Source Current

In Fig. 12 , the shunt filter started injecting current from 0.6 sec and Fig. 13 clearly shows the elimination of source current harmonics from the instant at which shunt APF is put into operation.

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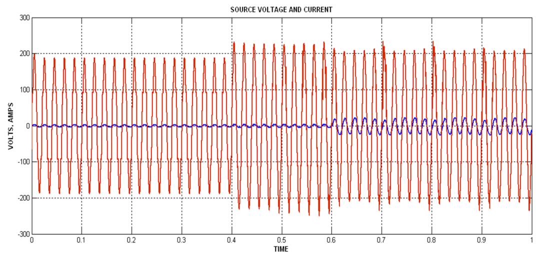
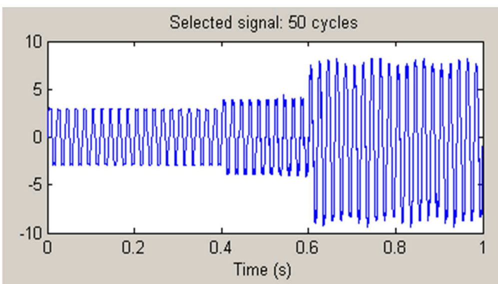
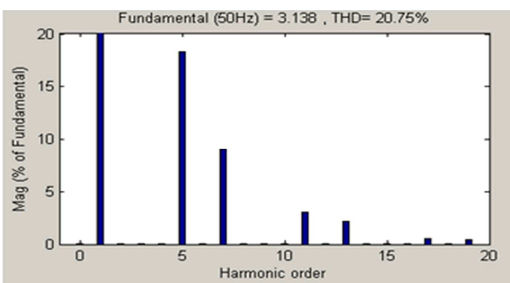


Fig.14. Source Voltage And Current

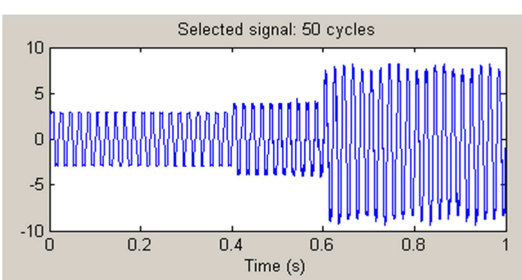
In the above Fig.14, from 0.6 sec at which shunt APF is put into operation, the source voltage and source current are almost in phase.

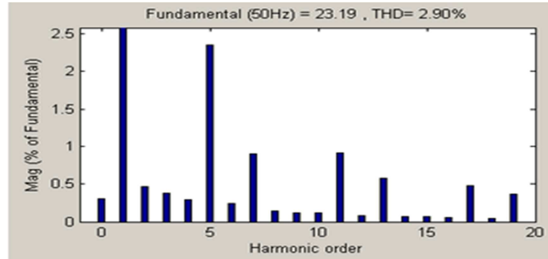
FFT Analysis Of Source Current:





FFT analysis is done for source current at 0.2sec, before switching ON both series and shunt filters and THD is found to be 20.75%.





Again FFT analysis is done at 0.75sec when both series and shunt filters are in operation and THD measured is 2.90% which is well within the prescribed limits as per IEEE – 519 standards. Here also, there is reduction of 86% in the THD after connecting the UPQC.

b) Total Harmonic Distortion Analysis Using Space Vector Pulse Width Modulation:

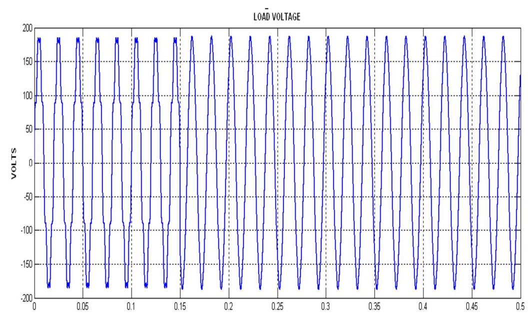


Fig. 15. Load Voltage

In the above Fig.15, before t = 0.15sec when both APFs are not put into operation, the load voltage is same as the source voltage. The series filter started injecting voltage from 0.15sec as shown in Fig.16. Also the shunt APF is put into operation at 0.3 sec.

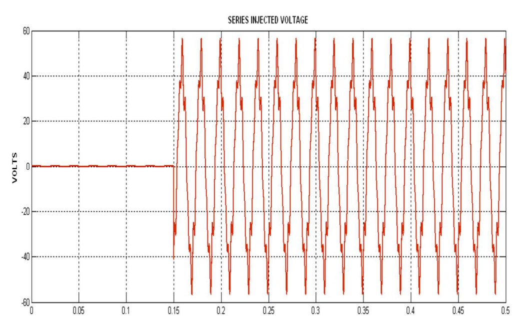


Fig.16 Series Injected Voltage

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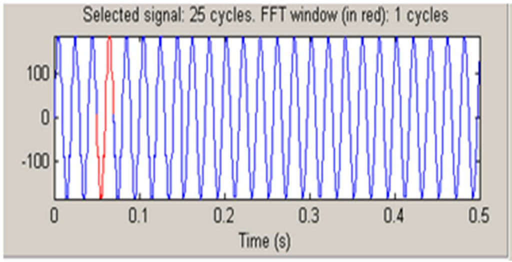
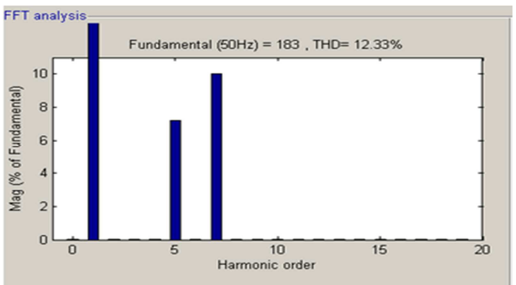
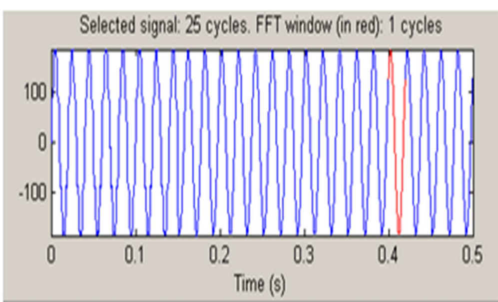
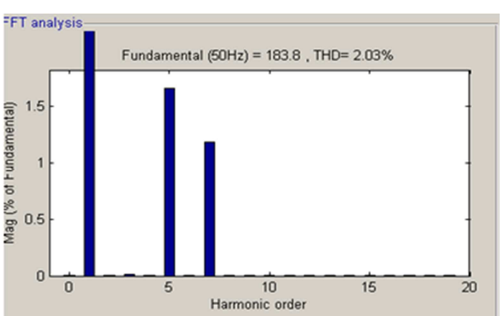
FFT Analysis Of Load Voltage:





The THD was measured at 0.05 sec , where both series and shunt filters are not in operation and is found to be 12.33%





FFT analysis is again done at 0.4 sec when both series and shunt filters are in operation. The measured THD is 2.03%. The reduction in the THD after connecting UPQC is 83.5%

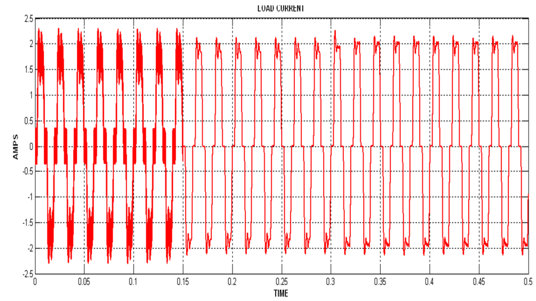


Fig.17. Load Current

From Fig.17, it is found that the load current is distortional due to non-linear load.

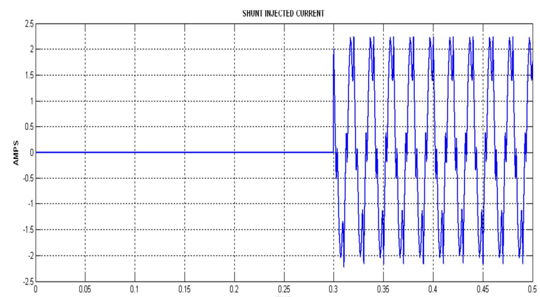


Fig.18. Current Injected By Shunt APF

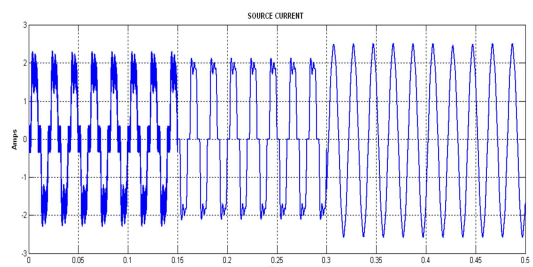


Fig.19. Source Current

From Fig.19, it is clear that the source current harmonics are eliminated from the instant at which shunt APF is operated.

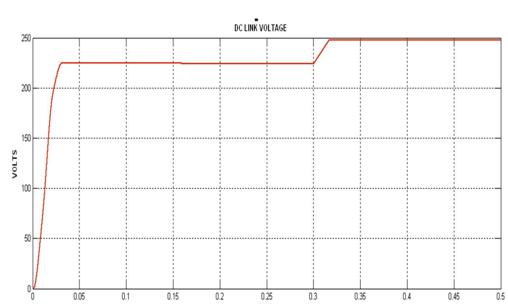


Fig.20. D.C. Link Voltage

Journal of Theoretical and Applied Information Technology
10th August 2015. Vol.78. No.1

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

It is clear from Fig.20 that after both the inverters are put into operation at 0.3 sec, the dc link voltage is maintained constant.

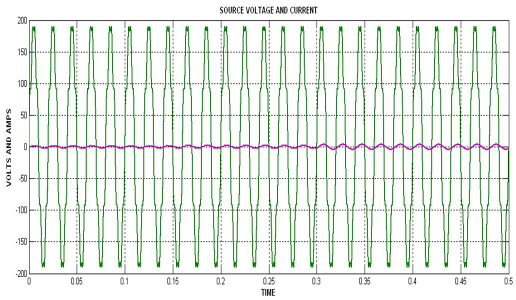
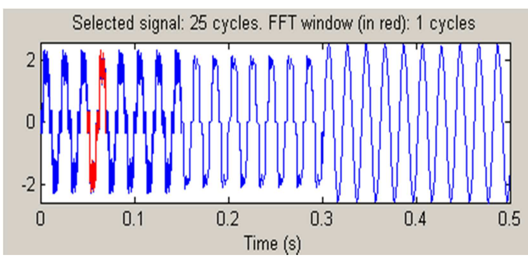
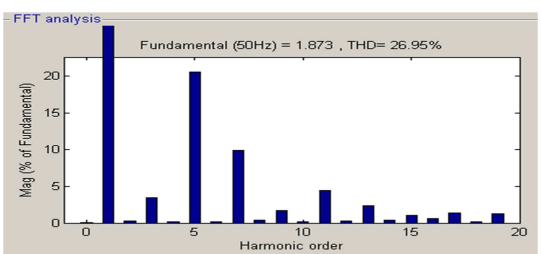


Fig.21. Source Voltage And Current

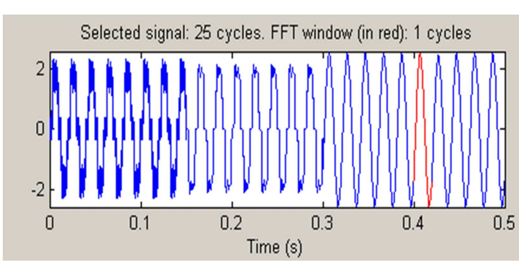
In Fig.21. , it is seen that from 0.3 sec at which shunt APF is switched 'ON', the source voltage and current are almost in phase.

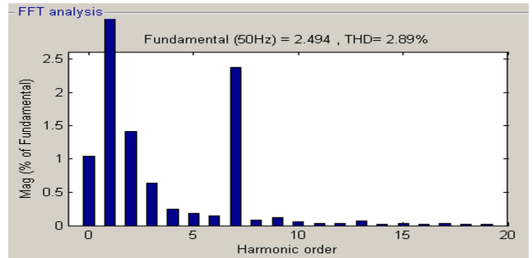
FFT Analysis Of Source Current:





FFT analysis is done at 0.05 sec before switching ON the series and shunt filters and THD is 26.95%





THD is again measured at 0.4 sec after connecting both series and shunt filters and is found to be 2.89% which shows reduction of 89%.

Table.3: Results Of Two Level UPQC With SPWM And SVPWM Control Schemes.

Control Scheme	Load voltage		Source current	
	%THD Before compen-sation	%THD After compen-sation	%THD Before compen-sation	%THD After compen-sation
SPWM	12.32	4.32	20.75	2.90
SVPWM	12.33	2.03	26.95	2.89

The above Table 3 shows the THD content in the load voltage and source current before and after connecting 2 level UPQC employing SPWM and SVPWM.

In the literature, the two level VSCs are used for the evaluation of the performance of UPQC with SPWM control technique. In this paper, an attempt is made to apply SVPWM control technique to two level UPQC for better compensation of harmonics in load voltage and source current which is very clearly observed from the simulation results and also mentioned in the FFT analysis.

6. CONCLUSION:

The performance of UPQC has been evaluated for harmonic elimination based on unit vector template generation control. The harmonics are deliberately injected into the system to validate the performance of the UPQC connected to a non-linear load. The UPQC has successfully reduced the harmonics from the load voltage and source current. Simulations were carried using Sinusoidal Pulse Width Modulation and Space Vector Pulse Width Modulation techniques. The simulation results show that the Total Harmonic Distortion of the load voltage after UPQC is put into operation is

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

less in case of SVPWM compared to SPWM. The above results comply with IEEE-519 standards.

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