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FPGA IMPLEMENTATION OF OFDM TRANSMITTER USING SIMULINK AND XILINX SYSTEM GENERATOR

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ABSTRACT

Growth in technology has led to unmatched demand for high speed architectures for complex signal processing applications. In 4G wireless communication systems, bandwidth is a precious thing, and service providers are continuously trying to accommodate more no of users within a limited available bandwidth. To increase data rate of wireless medium with higher performance and to overcome the frequency selective fading, inter-symbol interference (ISI) effectively, Orthogonal Frequency Division Multiplexing (OFDM) is used. It will be a hard core technology used in the future mobile communications. The basic principle of OFDM is studied in this paper and modeling was carried out in MATLAB followed by Verilog HDL implementation. The Verilog code is written and simulated in XILINX 14.2 and tested using FPGA Spartan-3E board.

Keywords: OFDM (Orthogonal Frequency Division Multiplexing), ISI (Inter Symbol Interference), FPGA (Field Programmable Gate Array), HDL (Hardware Descriptive Language), 4G (4th Generation

1. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) is a technique of transmission which ensures well organized utilization of the spectrum by the concept of overlap of carriers. It is an amalgamation of modulation with multiplexing that is used in the transmission of information and data. With the increase in traffic the need for efficient use of the spectrum plays a crucial role in future wireless modulation. The 4G communication system is being used in some of the developed countries like USA and UK. It is expected to have higher data rates, high spectral efficiency. To achieve this data rate, selection of multicarrier modulation scheme is required. Some of the techniques being used are FDMA, TDMA, CDMA, WCDMA, OFDMA, etc. Among them OFDM is the latest technique which has many applications such as Digital Audio Broadcasting (DAB), Digital Video Broadcasting (DVB), and for Asymmetric

Digital Subscriber Line (ADSL) high data rate wired links. Independent signals which are a subset of a main signal multiplexed in OFDM and the signal is first splitted into independent channels, data is modulated and then remultiplexed to create OFDM

Carrier. Orthogonality of subcarriers is the principle concept in OFDM. It allows simultaneous transmission of a lot of sub-carriers in a tight frequency space without interference from each other. This acts as a fulsome advantage in OFDM.



Figure 1: Block Diagram Of OFDM

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In a conventional S/P block, the symbols are transmitted sequentially along the frequency spectrum, each data symbol allowed to occupy the entire available bandwidth .When the data rate is sufficient high, several adjacent symbols may be completely distorted over frequency selective fading or multipath delay spread channel. The spectrum of an individual data element normally occupies only a small part of available bandwidth. Because of dividing an entire channel bandwidth into many narrow sub bands, the frequency response over each individual sub channel is relatively flat. A parallel data transmission system offers possibilities for alleviating this problem encountered with serial systems.

2. IMPLEMENTATION OF OFDM USING SIMULINK

Simulink, technologically advanced by Math Works, which is a data flow graphical programming language which consists of in built tools for modeling, simulating and analyzing multi domain dynamic systems. It offers tight integration with the rest of the MATLAB environment and can either drive MATLAB or be scripted from it. Simulink is widely used in digital signal processing for multi domain simulation and Model-Based Design

2.1 DESIGNED MODEL IN SIMULINK



Figure 2: Designed model of OFDM in Simulink



Figure 3: Transmitted Signal



Figure 4: Received Signal



Figure 5: Transmitter Scatter Plot

2.2 RESULTS OBTAINED

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Figure 6: Receiver Scatter plot



Figure 8: Data Source

3.2. Serial to Parallel Converter



Figure 7: Error Signal

3. IMPLEMENTATION OF OFDM TRANSMITTER ON FPGA

3.1. Data Source

The Simulink block for the source is implemented using a Bernoulli binary generator which generates random binary numbers using a Bernoulli distribution with parameter 'p' produces zero with probability p and one with probability 1-p. It has a mean value 1-p and variance p(1-p). The parameter probability of a zero, p can be any real number between zero and one. For the block we assumed the value as p as 0.6, initial seed 67 samples per second. The output data which is double is given to a serial to parallel converter Serial to parallel converter is used to convert groups of samples into single sample as bits, as the modulation process can operate only on bits.



Figure 9: Serial to parallel converter

Signal Constellation specified for a QPSK modulation with m=4 is [0.7071 + 0.7071i 0.7071 - 0.7071i - 0.7071i - 0.7071i - 0.7071i - 0.7071i]. The pattern is generated using multiplexer



Figure 10: QPSK Mapping

SELECT(a,b)	MUX 1	MUX 2
(a,a)	-0.7070	-0.7070

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10010 1002 0010		<u></u>		
(a,b)	-0.7070	0.7070		
(b,a)	0.7070	-0.7070		
(b,b)	0.7070	0.7070		
	Table 1	·		

The data generated is mapped by the multiplexer output and the output of is given to a Inverse Fast Fourier Transform

3.3. Inverse Fourier Transform

IFFT converts the signal from frequency domain to time domain. It plays a major role in OFDM. The FFT block is to set '1' for IDFT operation and '0' before the start of the transform, so a pulse generator is connected to fwd_inv_we pin in FFT block.





A pulse generated is created for the start pin to start the conversion process for every high pulse. The FFT output needs to be manually scaled for the factor of 1/N. The scaling can be done either by using the scaling input or shifting the FFT output. The output is converted to a workspace.

3.4 Designed Model For Ofdm Transmitter Using System Generator Blocks



Figure 12: OFDM Transmitter



Figure 13: Simulation Outpu

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The System Generator block provides control of system and simulation parameters, and is used to summon the code generation process. The designed model should contain elements from the Xilinx System Generator block.

<u> </u>	System	Generator: untitled	-	□ ×
Compilation Clo	cking Gener	ral		
Compilation :				
> HDL Netlist				Settings
Part :				
> Spartan3E xc3	s1200e-4fg320			
Synthesis tool :		Hardware description	on language :	
XST	~	VHDL	*	
Target directory				
./netlist				Browse
Project type :				
Project Navigator			~	
Synthesis strate	gy :	Implementation stra	tegy :	
XST Defaults*	V	ISE Defaults*	~	
Create interface	document urable subsystem	Create testbench		
Performance Tips	Generate	OK Apply	Cancel	Help

Figure 14: System generator block parameters

After giving the substantial information for the system generator block, VHDL code will be generated.



Figure 15: VHDL Code generation



Figure 16: Code Compilation Status

3.6. FIELD PROGRAMMABLE GATE ARRAY

FPGA (Field Programmable Gate Array) is an IC designed for reprogramming the desired application or functionality requirements after manufacturing by a customer or a designer. Nexys2 circuit board is a ready-to-use circuit developed by Xilinx Spartan 3E FPGA. It consists of 16Mbytes of RAM and ROM, I/O devices, ports and an onboard power. So the Nexys2 board can be used with a notebook computer to create a truly portable design station.



Figure 17: Nexys 2 board

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After successful compilation a JTAG hardware Co simulation block will be created which is used to check the output corresponding to hardware. Both the results are compared. The inputs of the JTAG are connected to the respective inputs of the designed model and the outputs are connected either by scopes or workspaces.



Figure 18: JTAG Hardware Co simulation Block



Figure 19: Designed model

The results which are obtained from the hardware are stored in the wave scope



Figure 20: Result from JTAG Co Simulation Block

RTL Schematic

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TECH Schematic

Design Summary

transmitter_xilinx1_cw Project Status (03/24/2015 - 12:06:04)			
Project File:	transmitter_xilinx1_cw.xise	Parser Errors:	No Errors
Module Name:	transmitter_xilinx1_cw	Implementation State:	Synthesized
Target Device:	xc3s500e-4fg320	Errors:	No Errors
Product Version:	ISE 14.2	• Warnings:	91 Warnings (0 new)
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Xiinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	Final Timing Score:	

	Devic	e Utilization Summary (est	imated values)			
ogic Utilization		sed	Available		Utilization	
Number of Slices		11		4656		
Number of Slice Flip Flops		17		9312		
Number of 4 input LUTs		3		9312		
Number of bonded IOBs		63	232			
Number of GCLKs		1	1 24			
		Detailed Reports				
Report Name	Status	Generated	Errors	Warn	ings	Infos
Synthesis Report	Current	Tue 24. Mar 12:06:03 2015	0	<u>91 Wa</u>	rnings (0 new)	<u>1 Info (0</u>
Translation Report	Out of Date	Tue 24. Mar 12:04:21 2015	0	35 Wa	rnings (35 new)	0

Figure 23: Design Summary

SUMMARY

The Orthogonal Frequency Division Multiplexing transmitter is implemented using both Simulink and Xilinx blocks on FPGA. The system hardware interface circuit is simple, convenient and efficient. The results from software simulation and hardware results of Xilinx blocks are compared and both are verified in Xilinx Spartan3E FPGA. In future with the designed model of transmitter we can also design the receiver.

Figure 22: Technological Schematic

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