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MODELING AND SIMULATION OF A THREE PHASE MULTILEVEL INVERTER FOR HARMONIC REDUCTION BASED ON MODIFIED SPACE VECTOR PULSE WIDTH MODULATION (SVPWM)

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ABSTRACT

A multilevel inverter is a preferred choice for most medium-voltage and high-power applications, as well as cascaded H-bridge (CHB) two-level inverters due to its advantages such as low cost, light weight and compact size. Space vector modulation is widely used in real-time digital control for power inverter and better DC utilization. It is suitable particularly for use in a cascaded H-bridge multilevel inverter due to reduced total harmonic distortion (THD). This paper discusses harmonic reduction of a three-phase (CHB) multilevel inverter. Harmonic content in multilevel inverters can be investigated by generating a space vector pulse width modulation algorithm (SVPWM) signal based on a standard two-level SVPWM. It uses a simple mapping to generate gating signals for the inverter. The proposed modulation was compared for two-, three- and five-level cascaded inverters to reduce high total harmonic distortion, high switching losses and reduce cost based on the cascaded H-bridge two-level consists of one lookup table 6 switching one DC source, three-level consists of two lookup table 12 switching two DC sources and five-level consists of four lookup table 24 switching four DC source inverters. The algorithm can be easily extended to an N-Level inverter. It is an application to cascade H-bridge topology as well. The proposed scheme has been designed using MATLAB/Simulink and it only consists of four switching cells (CHB) and four DC voltage supplies for five-level with R-L load that can be used to any level.

Keywords: *Multilevel Inverter, Cascaded H-Bridge (CHB); SVPWM; Total Harmonic Distortion (THD) DC Sources.*

1. INTRODUCTION

A multilevel inverter is a preferred choice for most medium-voltage and high-power applications, as well as cascaded H-bridge (CHB) two-level inverters due to its advantages such as lower common-mode voltage, lower dv/dt, reduced total harmonic distortion (THD) in output voltage current and reduced voltage on power switching for a general circuit of 5-level cascaded H-bridge inverter as shown in Figure 1 [1]. Converting a static structure that comprises mainly applications of power electronic is becoming increasingly important for power of the topology. It has to adapt to the growth of the power to convert a multilevel inverter, for example three topology cascaded H-bridge (CHB), diode clamped (NPC) and flying capacitor (FC) [2] [3]. Space vector modulation is a more attractive candidate and its advantage is the six sector voltage $(V_1 - V_6)$ that operates starting from each switching vector as a point in complex (~) space and consists of six sectors, with each having an angle of 60 degree as shown in Figure 2 [4]. Each sector consists of $(n-1)^2$ triangle. SVPWM diagram of an n-level inverter consists of 125 five- level, 27 three-level 27 and 8 two-level switching states [6].

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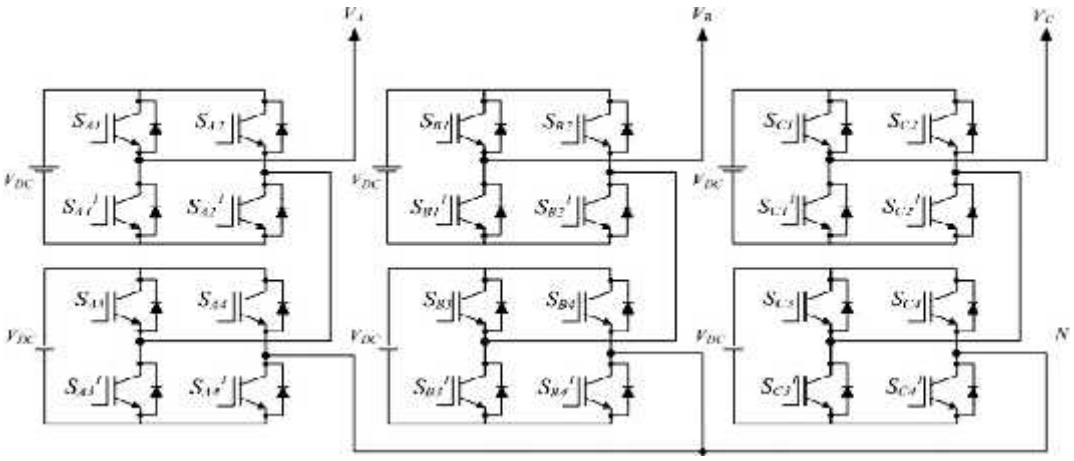

Figure. 1. General circuit of a three-phase five-level cascaded H-bridge multilevel inverter [5].

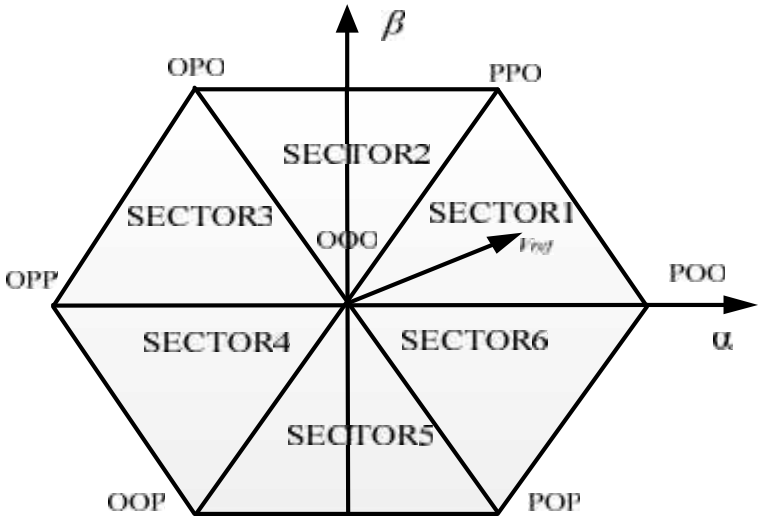

Figure 2. Space Vector Diagram For A Two-Level Inverter.

This paper discusses harmonic reduction of a three-phase (CHB) multilevel inverter. Harmonic content in a multilevel inverter can be investigated by generating SVPWM signal based on standard stander two-level SVPWM. The circuit structure and switching states of a 2 five-level cascaded H-bridge inverter are introduced. The proposed modulation is compared with 2 three- and five-level cascaded inverter to reduce high total harmonic distortion, high switching losses and reduce cost based on two-level cascaded H-bridge that consists of one lookup table 6 switching one DC source inverters, three-level that consists of two lookup table 12 switching two DC source inverters, and five-level that consists of four lookup table 24 switching four DC source inverters. The comparison study for CHB of two five-level inverter features higher operating voltage series, better THD output for current and voltage and lower electromagnetic interference (EMI) [7]. Space vector modulation (SVM) for five-level inverter consists of 16 triangles, in which triangle one has 13 switching states vectors, triangle two-four have 10 switching states vectors, triangle three has 11 switching states vectors, triangle five-seven-nine have 7 switching states vectors, triangle six-eight have 8 switching states vectors, triangle ten-twelve-fourteen- sixteen have 4 switching states vectors and triangle eleven-thirteen-fifteen have 5 switching states vectors [8]. A three-level inverter consists of four triangles; triangle one consists of 7 switching states vectors, triangle two consists of 4

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switching states vectors, triangle three consists of 5. switching states vectors and triangle four consists of 4 switching states vectors as shown in Figure 3 [9]. The algorithm can be easily extended to an ON-level inverter. Its application is for cascaded H-bridge topology as well. The proposed scheme is designed using MATLAB/Simulink and it only consists of switching cell (CHB) and four DC voltage supplies for five levels with R-L load that can be used at any level.

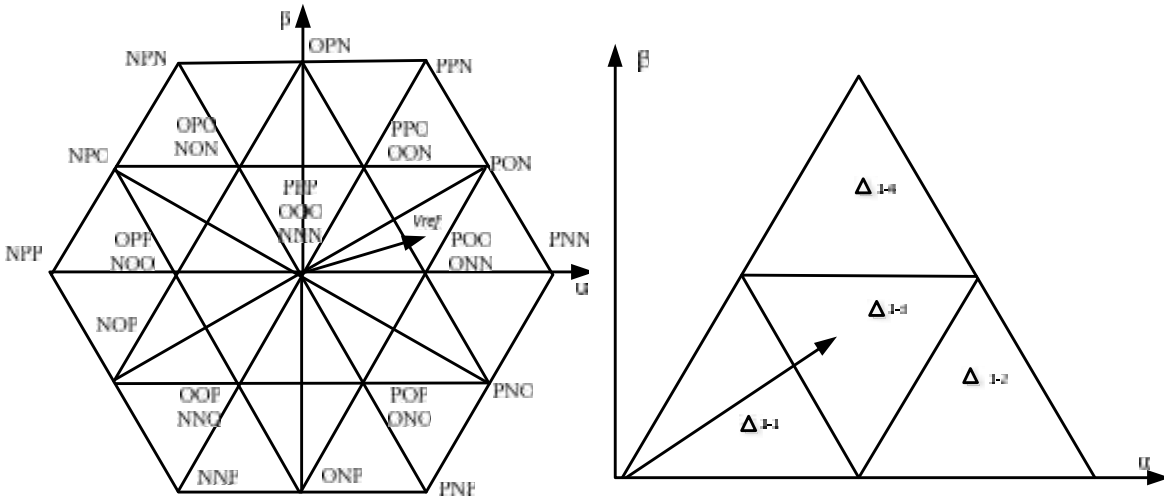

Figure. 3. Space Vector Diagram Of Three-Level CHB-MLI, Generator Sector One For Three-Level SVM [10].

2. SVPWM ALGORITHM FOR CHB-MLI

This section presents the general space vector modulation applied in the presented three-phase n-level CHB inverter. h $(0.866 = \sqrt{3}/2)$ [11] is the height of a sector Si, which is an equilateral triangle of unity side as shown in Figure 4. Space vector selection and switching state sequence of the inverter are discussed. The line-to-line voltage, V_R, V_S, V_T can be obtained through the inverter phase voltage:

$$V_R = m\sin(2® fs + 90) \quad (1)$$

$$V_S = m\sin(2® fs + 90 - \frac{2®}{3}) \quad (2)$$

$$V_T = m\sin(2® fs + 90 + \frac{2®}{3}) \quad (3)$$

According the three-phase to two-phase frame transformation, the output voltage of the three-level N-level cascaded H-bridge inverter can be represented by a space vector in the ~ frame:

$$\begin{bmatrix} V \\ V_{\sim} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \cos\frac{2®}{3} & \cos\frac{4®}{3} \\ 0 & \sin\frac{2®}{3} & \sin\frac{4®}{3} \end{bmatrix}\begin{bmatrix} V_R \\ V_S \\ V_T \end{bmatrix} \quad (4)$$

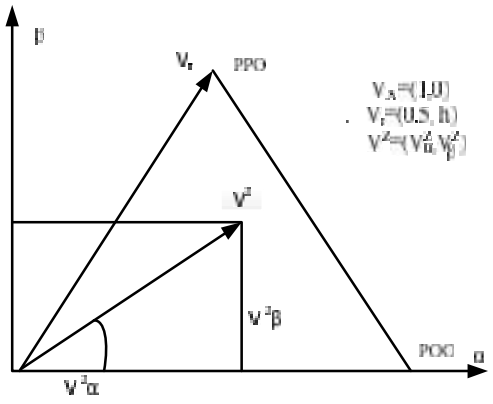

Figure. 4. Sector one for two-level inverter [11].

Where $V_{\sim}$ and V are the real and imaginary components of the space vector respectively.

$$\overline{V} = \left|\overline{V}\right| e^{j\measuredangle} \quad (5)$$

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Where $/\vec{V}/ = \sqrt{V_{\sim}^{\ 2} + V^{\ 2}}$ (6)

$$¥ = \tan^{-1}\left(\frac{V}{V_{\sim}}\right) \quad (7)$$

$/\vec{V}/$ is the magnitude and ¥ is the phase angle of the space vector. The space vector, reference vector, two-level inverter, on-time calculation within a sector Si, i = 1, 2, .., 6. for a two-level inverter volt-second equation is [12]:

$$V^{Z}T_s = V_X T_a + V_Y T_b \quad (8)$$

The volt-second equation in terms of components V^{Z}, V_X and V_Y along ~ − axis are:

$$V_{\sim}^{Z}T_s = T_a + 0.5T_b \quad (9)$$

$$V^{Z}T_s = hT_b \quad (10)$$

$$T_s = T_a + T_b + T_o \quad (11)$$

Solving Eqs. (9)-(11) produces equations for ON-time calculation,

$$T_a = T_S\left[V_X^{Z} - \left(\frac{V^{Z}T_S}{2h}\right)\right] \quad (12)$$

$$T_b = T_S\left[\frac{V^{Z}}{h}\right] \quad (13)$$

$$T_o = T_s - T_a + T_b \quad (14)$$

To apply SVPWM technique, first, the angle (¥) and sector (S_i) of $Vref$ need to be determined by using:

$$¥ = rem\left(\frac{-}{®/3}\right) \quad (15)$$

$$S_i = int\left(\frac{-}{®/3}\right) + 1 \quad (16)$$

In Eqs. (15) and (16), $0(0^{\circ} \le 0 \le 360^{\circ})$ is the angle of the reference vector with respect to ~ axis, $¥(0^{\circ} \le ¥ \le 60°)$ is the angle within the sector and $S_i(1 \le S_i \le 6)$ is its sector operation, and *int* and *rem* are standard mathematical functions of integer and reminder, respectively. The space vector diagram of a three-phase voltage source inverter is a hexagon, consisting of six sectors.

$$Z_1 = int\left(V_{\sim}\frac{V}{\sqrt{3}}\right) \quad (17)$$

$$Z_2 = int\left(\frac{V}{0.866}\right) \quad (18)$$

The purpose of SVPWM algorithm is to identify the triangle in which the tip of the reference vector is located. Each triangle can be treated as a vector of a two-level inverter. The ON-time can be calculated using the small vector analogy of the ON-time equation of a two-level inverter. Figure 5 shows the space vector diagram for a five-level inverter. In each sector, the triangles can be classified into two types. Type 1 triangle has its base side at the bottom, whereas type 2 triangle has its base side at the top, as described in the next section. The triangle number Δ_j can be determined in terms of two integer variables Z_1 and Z_2, which are dependent on the position of reference vectors ($V_{\sim}$, V). This rhombus is made of two triangles. Suppose ($V_{\sim S}$, $V_{\ S}$) are the coordinates of the reference vector with respect to the origin of the rhombus.

$$V_{\sim i} = V_{\sim} - Z_1 + 0.5Z_2 \quad (19)$$

$$V_{\ i} = V_{\ } - Z_2 0.866 \quad (20)$$

For a down triangle, Δij is obtained by Eq. (21) and the coordinates of $Vref$ are given by Eqs. (22) and (23).

$$\Delta ij = Z_1^2 + 2Z_2 \quad (21)$$

$$V_{\sim}^{s} = V_{\sim i} \quad (22)$$

$$V^{s} = V_{\ i} \quad (23)$$

For an up triangle, Δij is obtained by Eq. (24) and the coordinates of $Vref$ are given by Eqs. (25) and (26).

$$\Delta ij = Z_1^2 + 2Z_2 + 1 \quad (24)$$

$$V_{\sim\circ}^{s} = 0.5 - V_{\sim i} \quad (25)$$

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$$V^{s}_{\circ} = 0.866 - V_{i} \quad (26)$$

In Eqs. (21) and (24), Δ indicates the triangle and j is the triangle number and hence, Δj is an integer and signifies j^{th} triangle in the sector. Eqs. (21) and (24) are used to identify the triangles in a sector and ON-times are calculated using Eqs. (12)-(15). Δj is formulated to provide a simple way of arranging the triangle, leading to ease of identification and extension to any level, and it also greatly simplifies the PWM process as switching state can be easily mapped with respect to Δj [4]. The sector and switching states mapping are shown in Table 1.

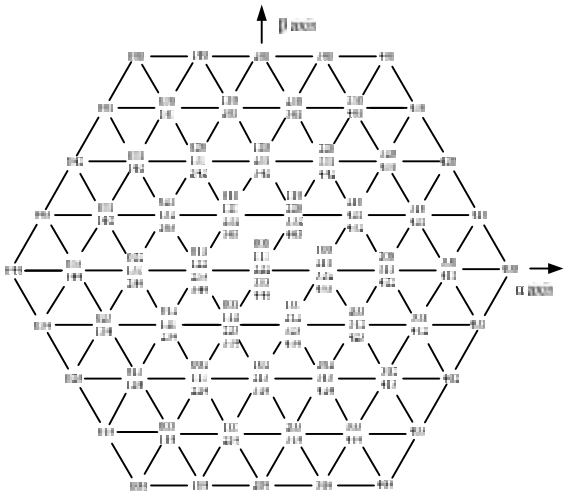

Figure 5. Space Vector Diagram For Five-Level Inverter [10].

Table 1.Sector And Switching States Mapping.

Sector	Phase A	Phase B	Phase C
S1	Sa	Sb	Sc
S2	-Sb	-Sc	-Sa
S3	Sc	Sa	Sb
S4	-Sa	-Sb	-Sc
S5	Sb	Sc	Sa
S6	-Sc	-Sa	-Sb

A three-phase five-level CHBMLI circuit diagram is shown in Figure 5. Table 2 lists the general characteristics of CHBMLI. Each of the three phases of the inverter shares a common DC bus, which has been subdivided by four capacitors into five levels. The voltage across each capacitor is Vdc, and the voltage stress across each switching device is limited to Vdc through CHBMLI. Table 3 lists the output voltage levels possible for one phase of the inverter with negative DC rail voltage V0 as a reference. State condition 'P' means the switch is ON and 'O' means the switch is OFF.

Table 2. General characteristics of CHBMLI.

CHBMLI	**A**	**B**	**C**	**D**	**E**	**F**	**G**
N-level	6(n-1)	(n-1)	n^3	$n^3-(n-1)^3$	$(n-1)^3$	2n-1	4n-3
2-level	6	1	8	7	1	3	5
3-level	12	2	27	19	8	5	9
5-level	24	4	125	61	64	9	17

A = number of switches.
B = number of consecutive switches of each leg to be in ON-state.
C = number of different voltage states of the inverter.
D = number of unique voltage states of the inverter.
E = number of redundant voltage states of the inverter.
F = line voltage levels.
G = phase voltage levels.

Table 3. Output Voltage Levels Possible For One-Phase CHBMLI.

Voltage Va	**Switching State**							
	*Sa*1	*Sa*2	*Sa*3	*Sa*4	*Sa*'	*Sa*'2	***Sa'* 3**	*Sa*'4
V_4=4Vdc	P	P	P	P	O	O	O	O
V_3=3Vdc	O	P	P	P	P	O	O	O
V_2=2Vdc	O	O	P	P	P	P	0	O
V_1=1Vdc	O	O	O	P	P	P	P	O
V_0=0	O	O	O	O	P	P	P	P

3. Proposed Design of Switching Space Vector Modulation

Seven-segment scheme has two types of switching state sequence of the CHB inverter in each region. Both type I and type II can meet the first design criterion. However, the switching state sequence based on the two types is different. Type I triangle type has its side at the bottom as shown Figure 6A, which can be assumed to sector 1 of a two-level inverter if Ao is equal to 0 vector real two level. Vector Ao *P* defines the small vector $v^{s}(v^{s}\sim_{\circ}, v^{s}{}_{\circ})$. ON-times $t_a(tA_a), t_b(tA_b),$ and $t_o(tA_o)$ are calculated by using Eqs. (12)-(14), where the operation only requires Eqs. (12)-(13). In Table 4, the first four switching states of type I are [ONN], [OON], [OOO] and [POO]. In the ~ -

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frame, the direction of their sequence is counterclockwise. On the contrary, the direction of the four switching states in type II is clockwise. A type II triangle has its side at the top as shown Figure 6B, if Aa is equal to 0 vector real two level. In this example, vector Aa *P* represents small vector $v^s(v^s_{\sim\circ}, v^s{}_{\circ})$. ON-times $t_a(tA_o), t_b(tA_b)$, and $t_o(tA_a)$ are calculated using Eqs. (12)-(14).

Type 4. Two Types Of Switching State Sequence.

Segment	Type I	Type II
1st	$\overline{V}$ [ONN]	$\overline{V}_{1P}$ [POO]
2nd	$\overline{V}$ [OON]	$\overline{V}_{0}$ [OOO]
3rd	$\overline{V}$ [OOO]	$\overline{V}_{2N}$ [OON]
4th	$\overline{V}$ [POO]	$\overline{V}_{1N}$ [ONN]
5th	$\overline{V}$ [OOO]	$\overline{V}_{2N}$ [OON]
6th	$\overline{V}$ [OON]	$\overline{V}_{0}$ [OOO]
7th	$\overline{V}$ [ONN]	$\overline{V}_{1P}$ [POO]

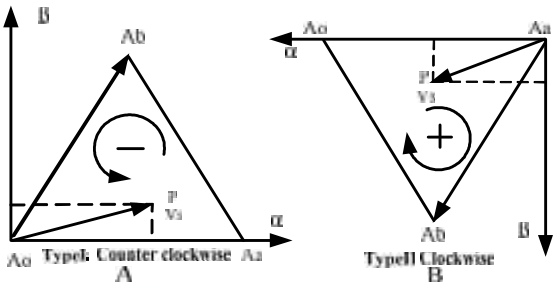

Figure 6. Direction of switching sequence based on the two types.

4. SIMULATION RESULT AND DISCUSSION ON MULTILEVEL INVERTER

In order to validate the performance of the proposed schemes, a simulation model for a three-phase CHB multilevel inverters was developed. In this simulation, the diagram for a two-level inverter using SVPWM technique to generate a cascaded H-Bridge inverter consisted of 6 IGBT switches and one DC source as shown in Figure.7. The parameters of the multilevel inverters were produced using MATLAB/Simulink. SVPWM algorithm can generate any level to extend 3 five-level inverters consist of 12 and 24 switches of IGBT block respectively in CHB inverters. The harmonic and THD profiles of the output voltage and current of the CHB inverters have been investigated. THD for voltage and current at 2 five-level output Cascaded H-Bridge in multilevel inverters was measured when Modulation Index (MI) was equal to 0.8 to 0.95. Three phase R-L load contains a balance, in which the values of the resistance R=3.69 and inductive L=2 mH. The fundamental frequency, f was 50Hz and the inverter switching frequency was 18 kHz.

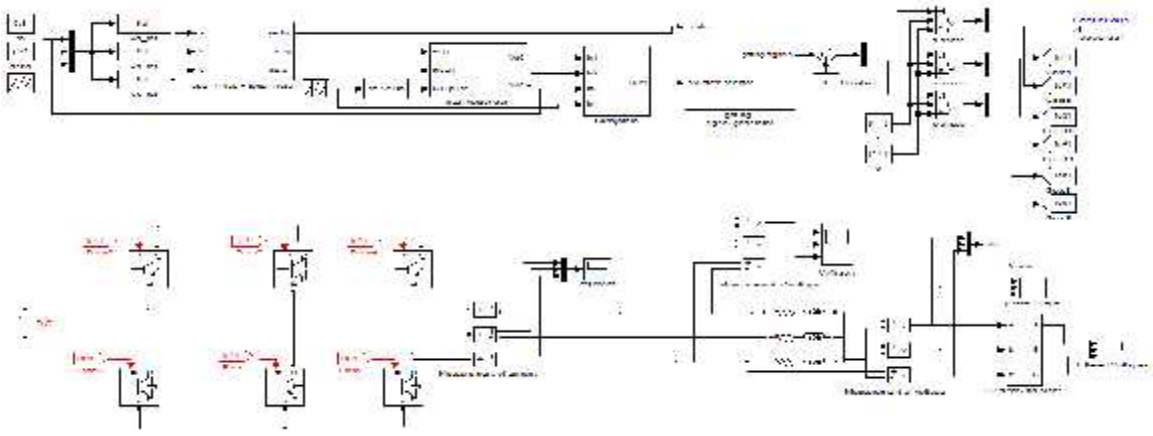

Figure. 7. Simulation Modeling Of SVPWM Generating Two-Level CHB Inverters.

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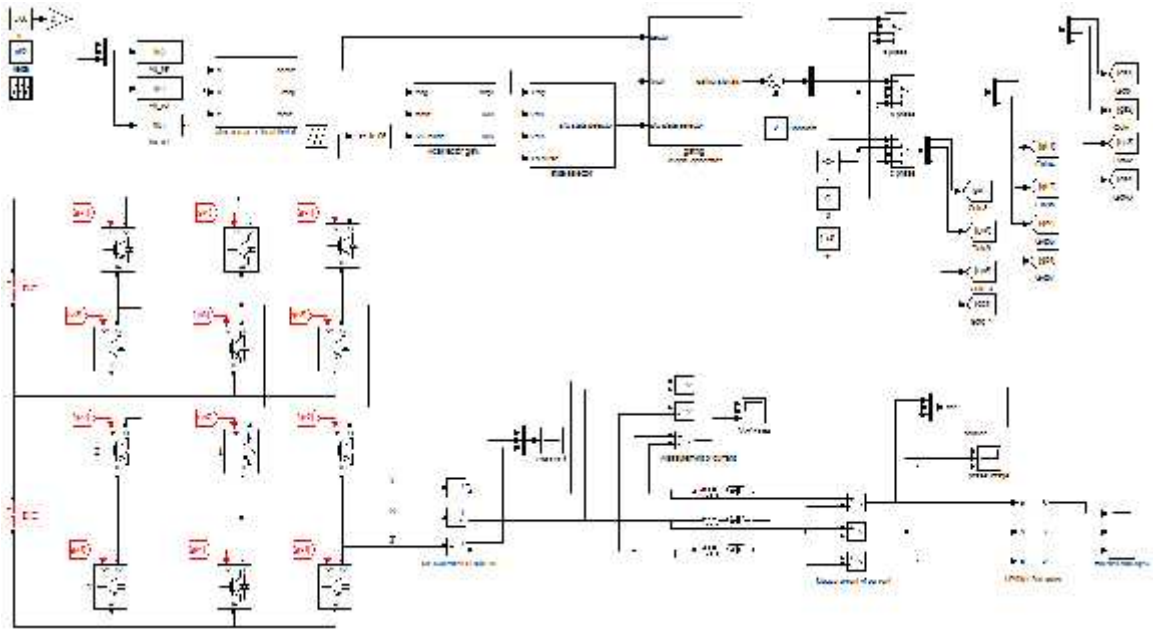

Figure. 8. Simulation Modeling SVPWM Generating Three Level CHB Inverters.

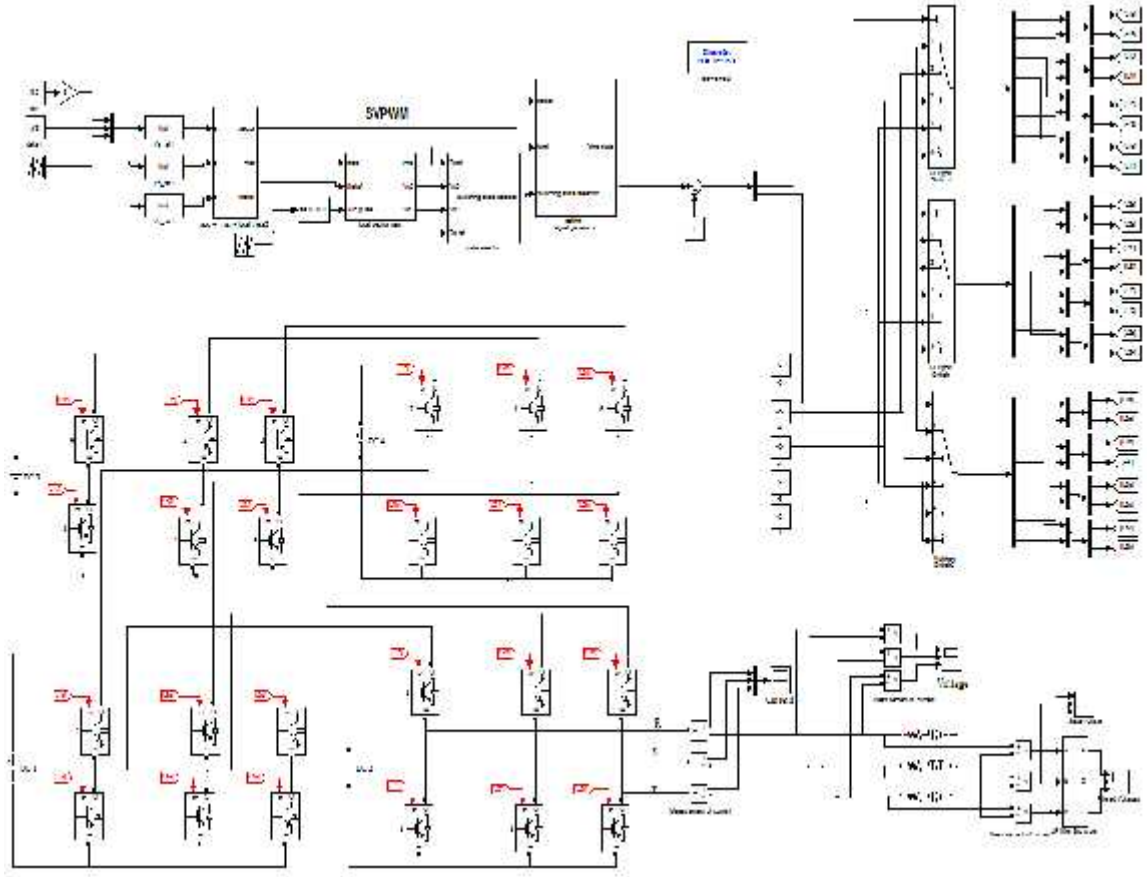

Figure. 9. Simulation Modeling SVPWM Generating Five Level CHB Inverters.

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4.1 Two-level cascaded H-Bridge inverter.

Line voltage and filtered voltage for the three-phase cascaded H-Bridge two-level inverter with modulation index of 0.8-0.95 are shown in Figures 8-9 and Figure 10, respectively. Meanwhile, current measurement for the three-phase inverter is shown in Figure 11. FFT analysis of the two-level cascaded H-bridge inverter with SVPWM is shown in Figures 12-13. For the two-level multilevel inverter, at MI=0.8, THD is equal to 36.61% as compared to THD of 28.07% at MI=0.95. Figure 14 shows that harmonic voltage filtered for two-level inverter is equal to 3.44%. THD measurement current is 3.94% as shown in Figure 15.

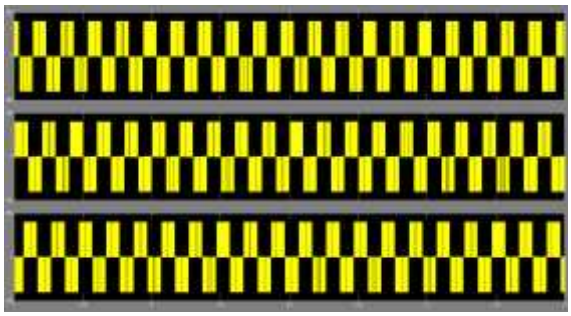

Figure 8. Line Voltage For Two-Level Inverter At MI=0.8.

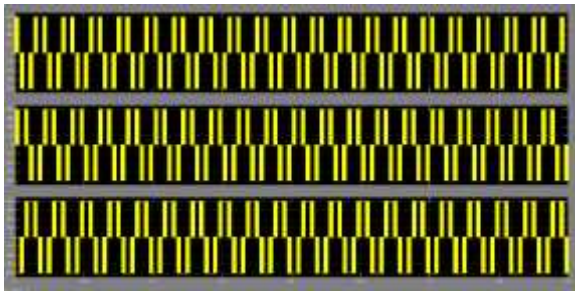

Figure 9. Line Voltage For Two-Level Inverter At MI=0.95.

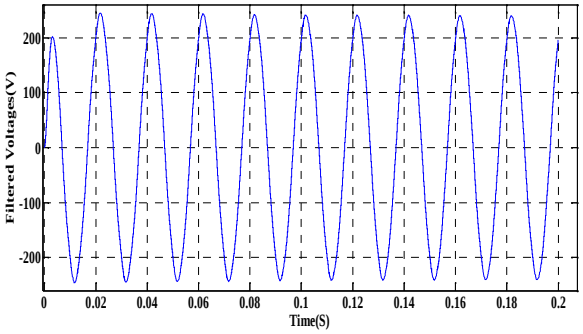

Figure 10. Filtered Voltage For Two-Level Inverter.

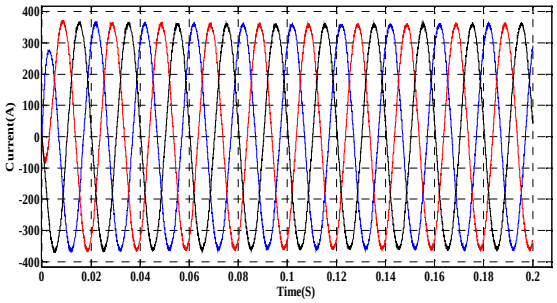

Figure 11. Three-phase current for two-level inverter.

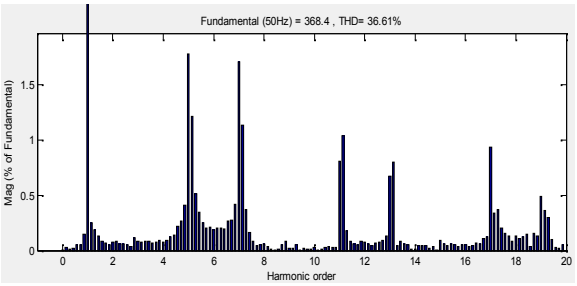

Figure 12. Harmonic Voltage For Two-Level Inverter At MI=0.8.

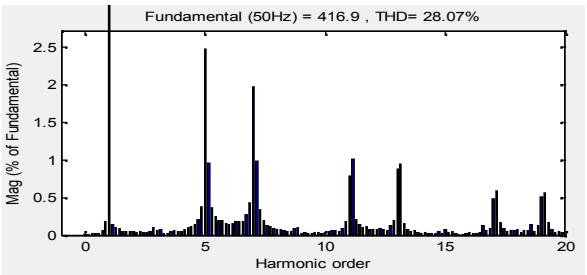

Figure 13. Harmonic Voltage For Two-Level Inverter At MI=0.95.

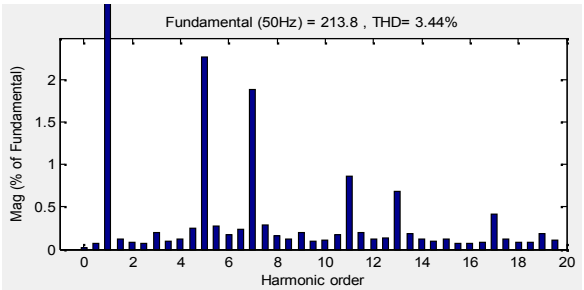

Figure 14. Harmonic Voltage Filtered For Two-Level Inverter.

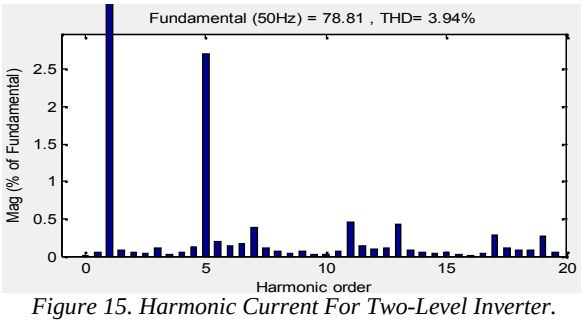

Figure 15. Harmonic Current For Two-Level Inverter.

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4.2 Three-level cascaded H-Bridge inverter

Line voltage and filtered voltage for the three-phase cascaded H-Bridge three-level inverter with modulation index of 0.8-0.95 are shown in Figures 16-17 and Figure 18, respectively. Meanwhile, current measurement for the three-level inverter is shown in Figure 19. FFT analysis of the three-level cascaded H-bridge inverter with SVPWM is shown in Figures 20-21. For the three-level inverter, at MI=0.8, THD is equal to 31.08% as compared to THD of 25.91% at MI=0.95. Figure 22 shows that harmonic voltage filtered for the three-level inverter is equal to 1.73%. THD measurement current is 1.61% as shown in Figure 23.

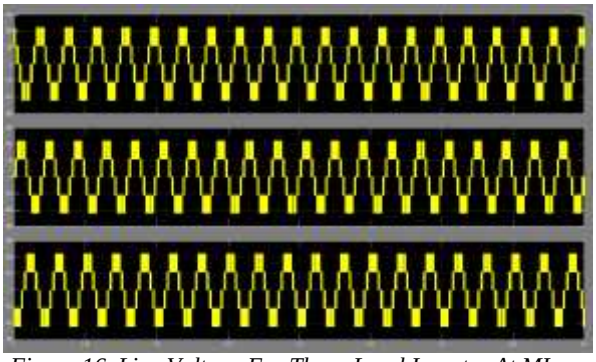

Figure 16. Line Voltage For Three-Level Inverter At MI= 0.8.

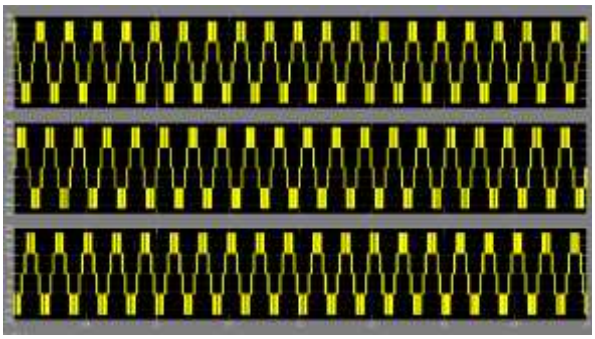

Figure 17. Line Voltage For Three-Level Inverter At MI=0.95.

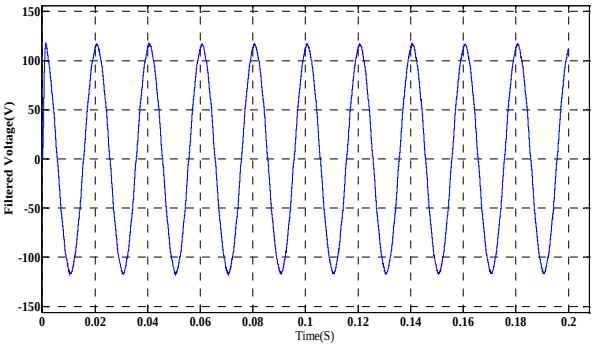

Figure 18. Filtered Voltage For Three-Level Inverter.

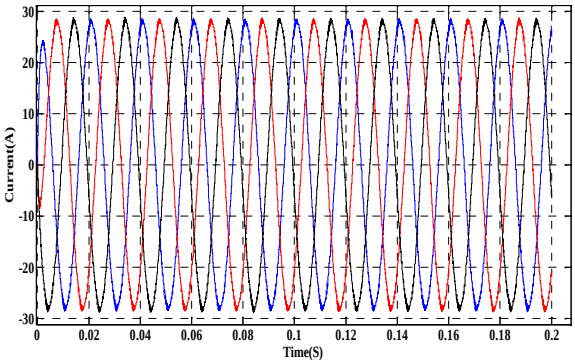

Figure 19. Three-Phase Current For Three-Level Inverter.

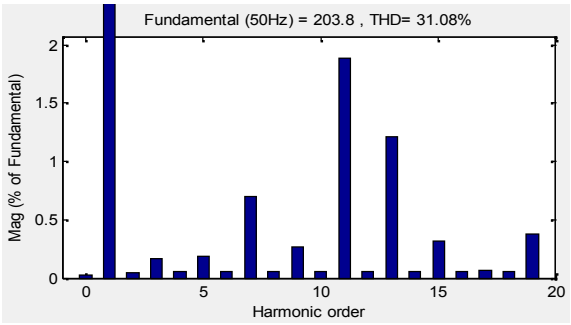

Figure 20. Harmonic Voltage For Three-Level Inverter At MI=0.8.

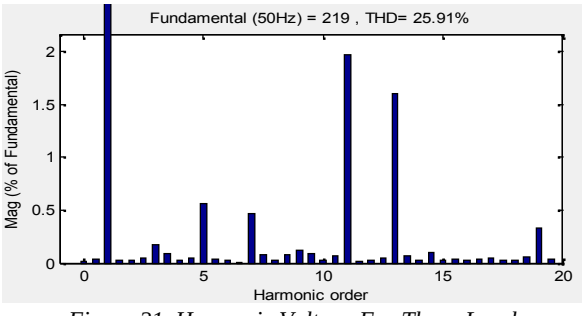

Figure 21. Harmonic Voltage For Three-Level Inverter at MI=0.95.

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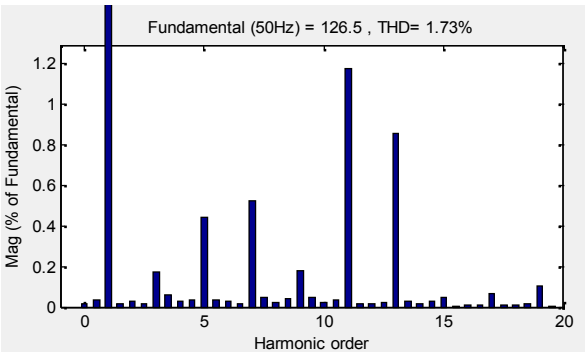

Figure 22. Harmonic Voltage Filtered For Three-Level Inverter.

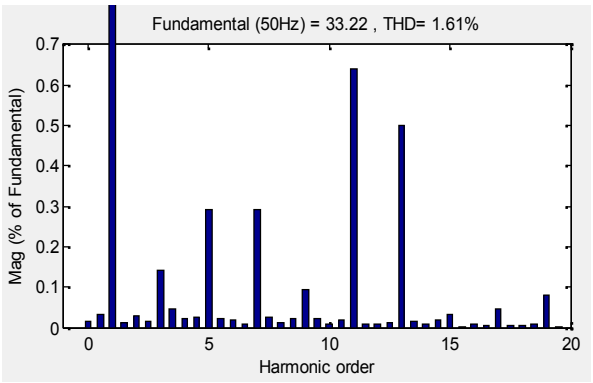

Figure 23. Harmonic Current For Three-Level Inverter.

4.3 Five-level cascaded H-Bridge inverter

Line voltage and filtered voltage for the three-phase cascaded H-Bridge five-level inverter with modulation index of 0.8-0.95 are shown in Figures 24-25 and Figure 26, respectively. Meanwhile, current measurement for the five-level inverter is shown in Figure 27. FFT analysis of the five-level cascaded H-bridge inverter with SVPWM is shown in Figures 28-29. For the five-level inverter, at MI=0.8, THD is equal to 24.72% as compared to THD of 21.62% at MI=0.95. Figure 30 shows that harmonic voltage filtered for the five-level inverter is equal to 0.83%. THD measurement current is 1.15% as shown in Figure 31. Figure 32 presents the comparison of n-level inverters in terms of total harmonic distortion.

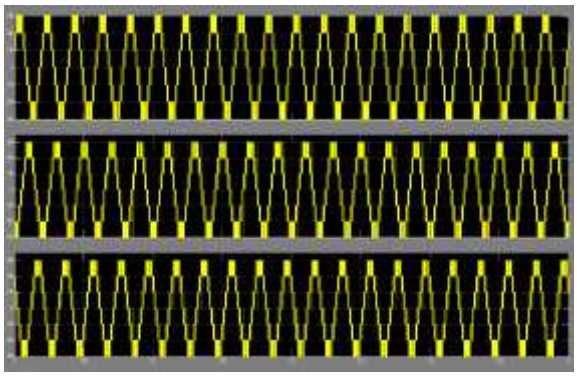

Figure 24. Line To Line Five Level MI 0.8.

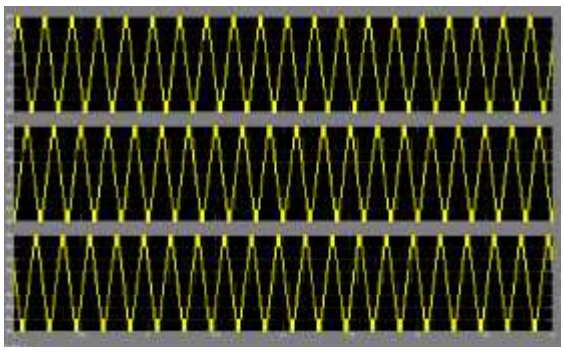

Figure 25. Line To Line Five Level MI 0.95.

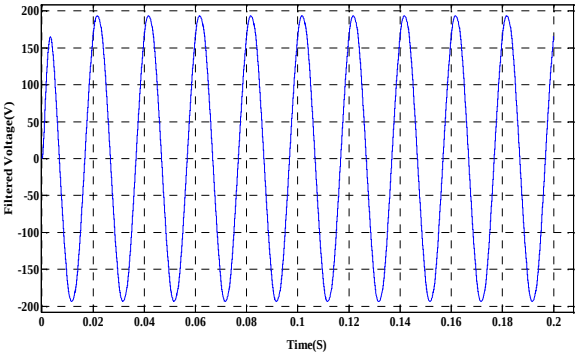

Figure 26. Filtered Voltage For Five-Level Inverter.

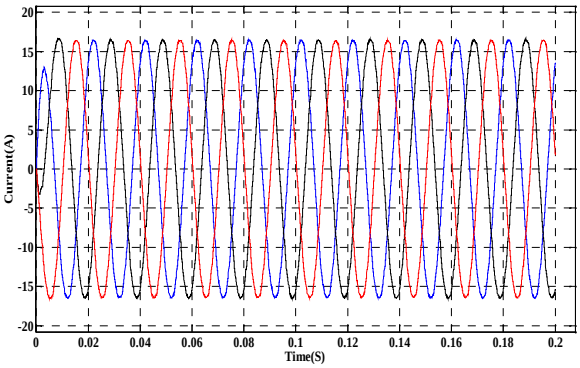

Figure 27. Three-Phase Current For Five-Level Inverter.

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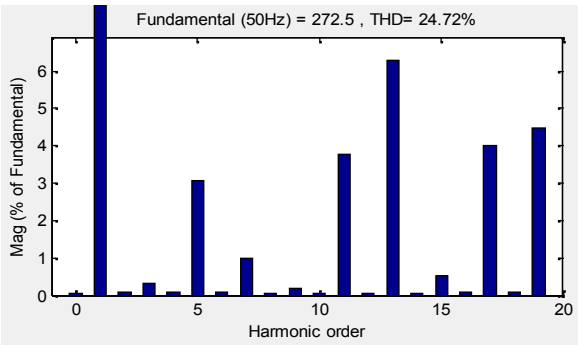

Figure 28. Harmonic Voltage For Five-Level Inverter At MI=0.8.

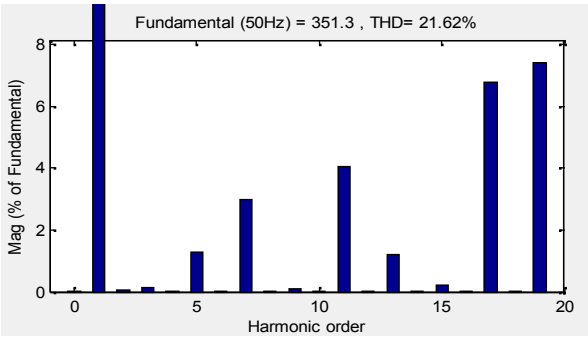

Figure 29. Harmonic Voltage For Five-Level Inverter At MI=0.95.

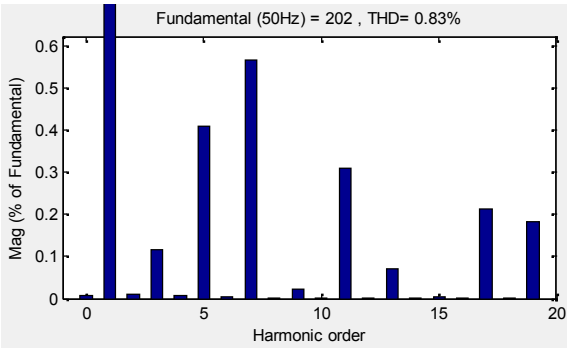

Figure 30. Harmonic Voltage Filtered For Five-Level Inverter.

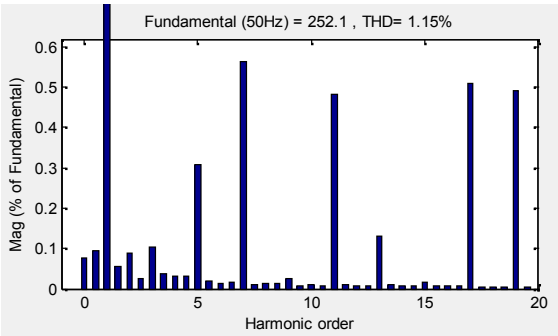

Figure 31. Harmonic Current For Five-Level Inverter.

5. CONCLUSION

This paper presents harmonic comparative study of a three-phase (CHB) multilevel inverter by proposing a general SVPWM algorithm based on standard 2 five-level SVPWM. Simulink models were developed for the space vector modulation CHB inverter. The proposed modulation was compared to 2 three- and five-level cascaded inverters to reduce high total harmonic distortion, high switching losses and reduce cost based on CHB. From the study, better performance is obtained when the modulation index increases.

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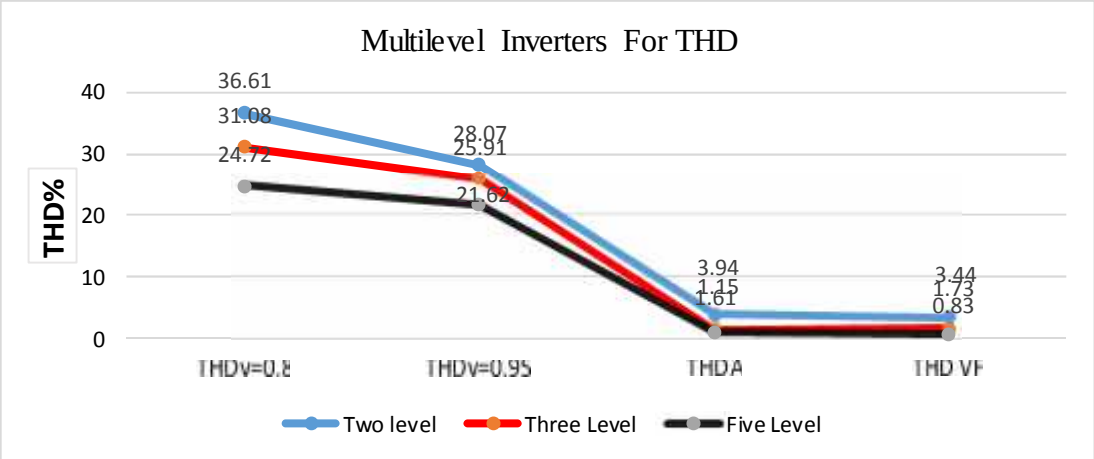

Figure 32. N-Level Inverter For Harmonic Reduction.

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