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REVIEW OF LOW POWER DIGITAL DELAY LOCKED LOOP (DLL)

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ABSTRACT

Digital delay locked loop (DLL) mainly designed to solve the clock skew in a system. This review presents the advances of DLL structure and its comparison overviews in various applications from past to advance applications. Digital DLL evolutions, parameters and performance characteristic in reducing total power consumption are discussed and shall work as a guideline for the researchers who wish to undertake related research projects.

Keywords: *Digital delay-locked loops, Low power, Low power consumption, Phase frequency detector*

1. INTRODUCTION

Clock phase accuracy is important in many appliances from past to present. Therefore, a dynamic de-skew circuit is needed to solve the clock skew of applications. DLL is a digital circuit design and the structure is similar to a phase-locked loop (PLL). The main difference between DLL and PLL is an internal voltage-controlled oscillator (VCO) of PLL is replaced by a delay line in DLL. The delay-locked loop (DLL) is a dynamic de-skew circuit that adjust the internal circuit delay (circuit clock signal phase) with the circuit signal reference. DLLs are newer than PLLs and used more in digital applications. DLLs use variable phase to achieve lock and lock onto a fixed phase difference whereas PLL's use variable frequency block as they adjust their frequency until there is a lock. DLL widely used in electronic systems such as processors, audio-video devices, memories and global systems for mobile communications. DLL commonly operate in non-linear analog, digital and mixed mode DLL [1].

Register-controlled DLL is one type of DLL and exponentially increase of delay cells amount versus increase of control bits number [2]. Another type of DLL is counter-controlled DLL which used to replace of register-controlled for controller hardware reduction [3]. A successive approximation register-controlled (SAR) - binary access algorithm is used for licked time reduction [4]. The popular DLL is time to digital converter (TDC). Both TDC and SAR are hard to track upon its operation in wide frequency range with high power and area requirements [5].

This paper organized as follows. DLL overview in Section II will provide information of the DLL elements used to develop a complete DLL system. Section III highlights the implementation of low power DLL module in various applications and gives bigger perspectives of DLL block to the reader. The discussions addressed in Section III. Finally, Section IV provides our conclusions.

2. DLL OVERVIEW

Digital DLL contains three main components that include phase detector (PD), control mechanism (CM) and digital controlled delay line (DCDL) depicts in Figure 1.

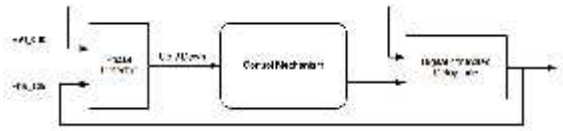

Figure1: Basic DLL Block Diagram

Phase Detector (PD): PD is the main component in DLL that drives the subsequence counter of system output. PD needs to spend minimum time in Setup and Hold times for better performance in different application. Single D flip-flop (DFF) is a simple PD (Phase detector) as shown in Fig 2. The DFF detects differences between Q and clock reference as an input. When Q is in logic low, it means that the output clock is leading the input clock reference and the delay of delay line is increased to compensate the variance in PD until attaining the lock condition [6].

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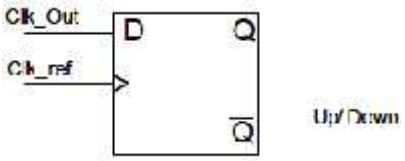

Figure 2: D-Flip Flop Phase Detector [6]

Another type of PD is dual output phase detector which is a regular phase error decisions as lag and lead based on Hold and Setup times respectively. This PD contains of two identical blocks, creating UP or DOWN output signal. Each block has two stages with pre-charge PMOS first stage output, controls the pre-charging of the second stage.

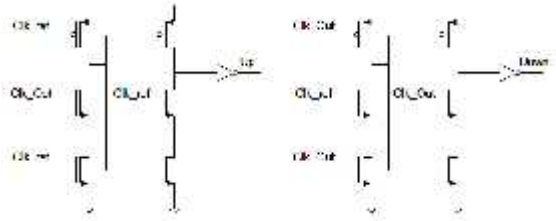

Figure 3: Dual Output Pd [7]

Control Mechanism: There are two types of control mechanism depend on different application of DLL. The first type DLL control mechanism is straight forward controlling mechanism shown in Figure 4. PD controls the clock differences among output, CLKOUT of the digital controlled delay line and clock reference as an input of PD. For instance, when CLKOUT output is in logic low, this indicates the output clock is leading the input clock reference and cause the delay of delay line increased to compensate with the difference in PD until attaining the lock condition.

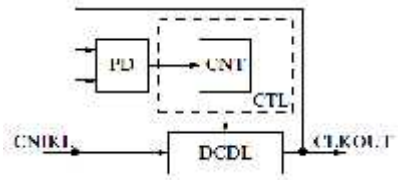

Figure 4: DLL Controlling Mechanism [8]

Another DLL control mechanism is finite state machine (FSM) as depicts in Figure 5. This module is placed in between phase detector output and up/down counter. The FSM functions send a high or low signal to counter based on both output of PD and FSM internal state according to system initial conditions.

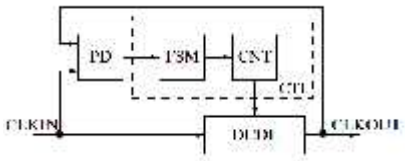

Figure 5: Controlling Mechanism Based On Finite State Machine [8]

Digital Controlled Delay Line: This module is an important structure in DLL which consists of two delay lines: Coarse Delay Line (as Gate-delay) and fine delay line (as Sub gate-delay). The coarse delay lines are made from CMOS logic gates in a cascade mode. It forms a delay line and the simplest delay lines are a sequence (chain). The chain constructed by cascaded inverters with each stage consisting of a couple of inverters and the necessary output tap is selected by multiplexer. The minimum delay of every stage is 2TD where TD is the common CMOS gate delay and requires $Log_2\ N$ storage elements where N is stages number [9]. Figure 6 shows coarse delay line design discussed in [10].

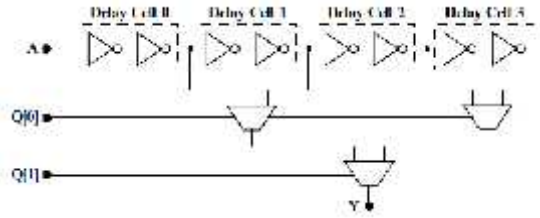

Figure 6: Digital Controlled Coarse Delay Line As Inverter [10]

Figure 7 illustrates another implementation of coarse delay line. The delay line is composed of multiple delay cells connected. Each delay cell is made of multiplexer (MUX) along with a buffer. The input1 from the MUX of first delay cell is linked to VDD and then for all the other delay cells the input1 is linked to the previous stage cell output.

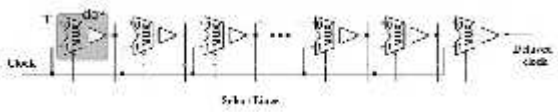

Figure 7: Digital Controlled Coarse Delay Line As MUX [9]

Fine Delay Line structures shown in Figure 8 and it used RC delay to generate delay. In Fig 8, the structure depends on cell resistance changes. Digital bits are used to control the

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branches. Figure 9 shows the second design that RC delay increases with the quantity of ON devices. The digital control bits could be encoded thermometric and logarithmic codes as a result of linear characteristics of the circuit. In former structure the dynamic range increases by cascading several stages [6]. These RC based delay line are discussed in more detail in [8]

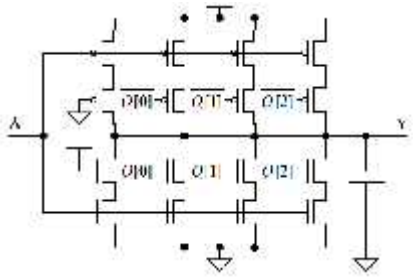

Figure 8: Common Digital Controlled Fine Delay Line [8]

3. DLL IMPLEMENTATIONS

Maintaining a low DLL operating supply voltage in a system is always a design concern. Low input power supply contributes to limit power consumption and heat dissipation as operating frequency is increased. DLL needs a number of cycle lock time during its initialization sequence.

Different type of applications using DLL techniques is shown in Figure 9 in order to meet the speed performance requirement. The advantages and disadvantages of each application are highlighted for quick review.

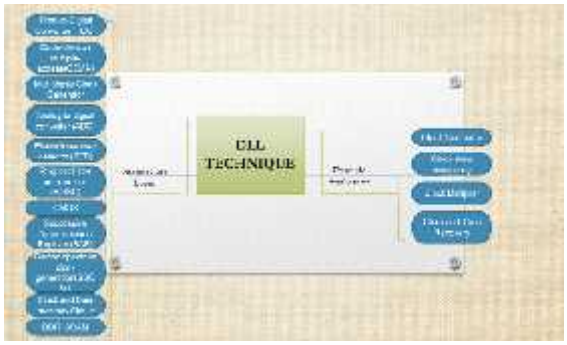

Figure 9: Different Type Of Applications And Architectures Using DLL

Analog to digital converter (ADC): The utilization of the DLL has created various architectures. Jinlong and Nicole reported DLL performance used in analog to digital converter (ADC) [10]. The benefits of using ADC mainly low power and area saving solutions for multi frequency cell impedance. ADC will loosen the limit of sampling rate and reduces the amount of bits in the counter to ensure the clock frequency of the counter may be reduced. ADC also saves the energy of the chip. As an example it's off before the comparator's output changes from low to high.

DDR SRAM: This architecture presented in [11][12][13][1]. DDR SRAM will operate synchronized with dual system clocks or dual loops with single replica block. DDR SRAM provides suitable output impedance for various memory systems and its different-type dual DCC at input and output, replay mode function, rising edge scanner and self-calibrated power down controller (SCPDC) for stable power management. DDR SRAM also features a phase mixer for DCC operation. Using this phase mixer, it could operate despite having big external clock's duty error, increase the total amount of unit delay for coarse locking, resets to completely clean arrival the registers of delay lines and control signals and achieves good quality data communication for computer speed. Besides that, it's clock de-skewing with good jitter performance which is suffering from slow locking and performance degradation as a result of sensitivity to variations of process and temperature. DLL in DDR SRAM operates only following the dual - loops of every locking. It fails in locking operation, if the external duty error is too large to feed the delay line and it can't be on-off controlled freely.

Time to Digital converter (TDC): DLL implementations in Time-to-Digital Converter (TDC) architecture was presented by Dongsuk et al. [14][15]. These works show DDL was used to convert enough time of a binary signal right into a digital value. The main advantage of the TDC is it always decreases the phase error and jitter, and range doublers to double its operating frequency range with a negligible increase of power and area. TDC has fast lock times, design simplicity, robustness and it features a configuration that is comparable to the clock-synchronized Delay (CSD). Furthermore, TDC solves the coarse resolution problem by adopting the best possible code generator. DLL built in CMOS technology was also presented by Dongwan et al. and Min-Han et al [16][17].

CMOS inverter was used as delays to digital temperature outputs, enables low energy and high bandwidth, facilitates fast thermal monitoring and synthesizes multiple temperature-independent delay references. It serves as a TDC and compares

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temperature-dependent inverter delays to the multiple delays. CMOS inverter can lock to a reliable clock, which also drives the open-loop delay line. This design has turned into a challenge as a result of trends related to CMOS scaling, high leakage current and low supply voltage. The key benefit of using CMOS design techniques is of its simplification to design for wide and fast-locking range requirements. The disadvantages of these techniques are jitters and variations of supply cause fluctuations in the digital outputs. This limited phase capture range on completely synchronous environments and complicates the start-up circuitry.

Ring oscillator architecture (ROSC): The ROSC based on DLL is reported by Zheng et al. [18]. The DLL used in the ROSC enables the system for sampling the reference clock series to obtain the period average of clock reference. The main advantage of ROSC is its operation with better skew and jitter performance. ROSC needs longer lock time, loop dependent process parameters. Besides that it is simpler to migrate to have much better tolerance which causes low supply voltage requirements. ROSC uses small active area, low power consumption and wide range of operating frequency.

Clock and Data Recovery (CDR): The usage of DLL block is to recover clock from sampling the input data and DLL clock generator prepare the clock signal of MUX to select the right data [19]. DLL CDR has better stability, lower noises and easy to design. However without VCO module in the CDR, phase errors frequently occur caused by supply and substrate noise

Successive Approximation Register (SAR): The function of SAR is to remove the harmonic locking issue in wide range performance, fast locking and close loop operation. SAR manages the application clock with small power consumption and low jitter [20][21]. In these reported works DLL provides better skew and jitter performance with immunity process but suffer harmonic locking issue and difficult process migration.

Phase frequency detector (PFD): Soh et al. worked on phase detector which is designed to overcome the limitation of speed and decrease the dead zone of the sequential [22]. The benefit of implementing PFD in DLL is dual path tuning. PFD also act as lock control circuit to check the switching between dual paths rapidly to perform better stability. In opposite, it has disadvantages as high output jitter and quantization errors.

Spread Spectrum clock generation (SSCG): The function of SSCG is to reduce the electromagnetic emissions through synchronizing the digital systems. SSCG produce conventional period locking mechanism. Delay relies on delay cells of DLL and its feedback caused the quick accommodation happen when clock input is changed. DLLs are used to solve the problem of synchronization between communication of SSC and non-SSC clock domain. DLL output frequently is in lock condition when the initial harmonic is close to some other harmonics.

4. DISCUSSIONS

Recent design technology concept is continuously revised to improve such important criteria as low power consumptions and higher quality of performance. Various DLL architectures have been developed to meet low power consumption. Since 1997 a DLL designed in 0.35 µm CMOS technology consumed 3.2 mW power operated at 100 MHZ under 2 V supply voltage [23]. The works reported in [1] tried to reduce power consumption between range of 36 mA – 29 mA with 1.8V, 1.6V, 1.6 V power supply respectively. Circuit design power consumption has been dramatically decreased to µW size and operated under 1.2 – 1.8 V input power supply voltage [10][16]. Table 1 shows DLL performance in different implementations reported between 1997 and 2014. There are few algorithms presented and reported have achieved reductions of power consumption including in ADC [10], microprocessor thermal [16] and AD-DLL [31] with 86.4 µW, 0.799 mW and 0.0194 Watt respectively. DLL is found for better performance because of its revolution in area size technology which is led to low power consumption and brings low jitter and wider range of operation phase.

We have described DLL's design considerations that include additive jitter, lock time, lock range, and power concern. From this study, jitter is identified as an important parameter in high-frequency operation. In order to reduce the jitter effects in a system, it is necessary to reduce the DLL's clock path. We found digital DLLs offer better jitter performance with low power consumption. The modelling part in designing a good DLL performance is very important and high standard simulation tool should be adopted to adjust and fix the clock skew. This paper has been

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categorized into two areas to present the selected topics separately. From the review, we found that fully digital DLLs offer promising technology to deal with the stringent power consumption and high operating frequency requirements."

5. CONCLUSIONS

Several digital DLL architectures are presented and discussed. Increased clocking system complexity, process variation, and wider supply voltage ranges are making DLL much more prevalent today. In this review, we presented a few low power DLL implementations proposed in previous study. DLL advantages and disadvantages in different application are reviewed. Future works will include the development of digitally controlled DLL circuit design simulation and the construction of mask design by using industrial standard design tool (Mentor Graphics). This review has also serves its purpose to provide initial guideline for the researches.

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Table 1: Table of DLL Performance And Power Consumption Comparison

Year	Application	Supply Voltage	Power Consumption	No. References
2014	Digital-to-Time Converter	0.9 V	0.5 mW	[14]
2013	Clock multiplication technique	1.1 V	890 µW	[24]
2012	Uses ADC	1.8 V	86.4µW	[10]
2011	Uses microprocessor thermal monitoring	1.2 V	799.8643 µW	[16]
2011	Ring Oscillator	1.2 V	5.2 mW	[18]
2011	Solid State Circuit	1.2 V	14.5 mW	[17]
2011	A synchronization-free spread spectrum clock generation	3.3 V	1.45 mW	[25]
2011	Clock and data recovery circuit	1.8 V	799.8643 µW	[19]
2011	CMOS auto calibrated I/O generator	1.2 V	-	[26]
2011	SAR technique	1.35 V	2.25 mW	[20]
2010	Clock synchronization in SoC.	1.0 V	1.012 mW	[27]
2009	Generation of multiphase clock	1.5 V	4.8 mW	[28]
2008	Code-division multiple access	2.0 V	1.65 mW	[29]
2007	variable Successive Approximation Register Algorithm	1.8 V	12.6 mW	[21]
2005	Fast-lock mixed-mode DLLs	1 V	2.43 mW	[30]
2004	production DDR SDRAMs	2.5 V	12 mA	[13]
2003	Time- to- Digital Converter	1.6 V	29 mA	[1]
1998	All-digital delay-locked loop	5 V	19.4 µW	[31]
1997	Low power all-digital delay-locked loop	2 V	3.2 mW	[23]