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A LOW POWER PHASE FREQUENCY DETECTOR FOR DELAY-LOCKED LOOP

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ABSTRACT

High performance phase frequency detector (PFD) is one of the key modules in high speed delay-locked loop (DLL). The operation of DLL depends on the performance of its detector. The demand for the reduction of power dissipation in CMOS design is a challenge in order to optimize circuit power consumption. A low power dynamic pseudo-PMOS PFD is proposed to make DLL system more reliable. In this work NOR gate of typical TSPC PFD is replaced with a low power dissipation pseudo-PMOS AND gate built of 3 PMOS transistors. Pseudo-PMOS AND integrated into proposed TSPC PFD to run maximum frequency at 1G Hz with 1.8 V input power supply. This proposed PFD has been implemented in Mentor Graphics 0.18 µm CMOS process technology and consumed 163.36 μm^2 active layout area with 206 nW total power dissipation will further trim down the total cost of the DLL.

Keywords: *DLL, Dynamic PFD, Low Power PFD, Low Noise PFD, Pseudo-PMOS*

1. INTRODUCTION

Phase-Locked Loop (PLL) and Delay-Locked Loop (DLL) frequently used to remove clock delay in various applications. DLL was derived from the PLL for the past ten years and it has attracted great attention especially in integrated system. Moreover, to remove clock distribution delay, DLL is embedded in frequency synthesis (clock multiplication and clock division) and clock conditioning (duty cycle correction and phase shifting). DLL is illustrated in simplest form as shown in Figure 1 [1]. It consists of variable delay line which is able to remove the delay between source clock and its loads. Control logic is a feedback with clock-in.

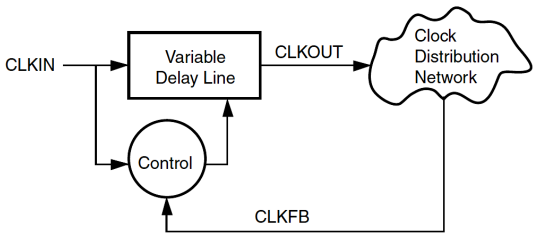

Figure 1: Dll Block Diagram [1]

As for quick review Figure 2 illustrating the PLL block diagram consists of control logic without feedback to clock-in in order to compensate the clock distribution delay and voltage controlled oscillator to replace variable delay line [2].

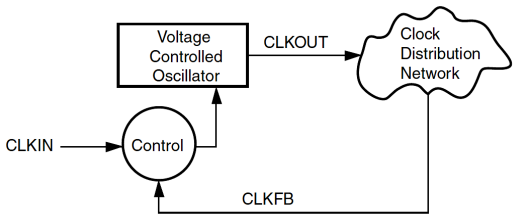

Figure 2: Dll Block Diagram [1]

Figure 3 depicts the element of DLL block. First-order closed-loop architecture utilized to dynamically align its output clock signal with reference clock signal [3]. Four main blocks in this system are phase frequency detector (PFD), charge pump (CP), loop filter (LF) and Voltage Controlled Delay Line (VCDL).

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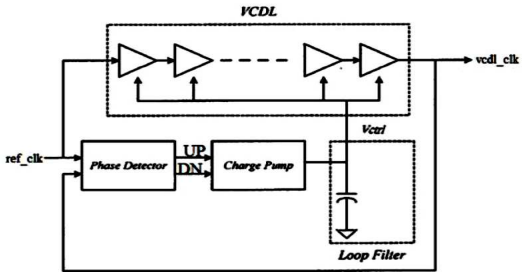

Figure 3: DLL Block Elements [3]

DLL input clock signals propagate through the VCDL and produce phase shift at every delay stage of the VCDL. The phase shift of each delay stage is regulated by the voltage of a loop filter. C CP and PFD generate controlled voltage. The output phase of delay stages will be compared with the PFD input signal. Clock skew is recognized as one of the main concern in high speed clock system. PFD plays an important role to overcome this drawback. PFD is used to detect phase and frequency difference between the reference frequency and the controlled slave frequency. The detected phase or frequency errors transmitted into current or voltage in order to regulate the output frequency of VCO thru the CP.

2. LITERATURE REVIEW

Phase noise of conventional PFDs is a great concern. Minimum phase noise can be achieved by trading off the PFD gain. Increase the transistor sizes is one of the approaches to improve the noise but it will increase power dissipation [4-5]. High power dissipation is inevitable in high frequency operations as in can caused PFD internal nodes not entirely pull up or pull down. Therefore, several optimization methods are proposed to minimized number of transistors by using pseudo-NMOS AND gate, pair of positive edge triggered true single phase clocked (TSPC) flip-flop and optimize transistor sizing in order to achieve the low power and compact PFD circuit design area. Conventional PFD built from large number of logic gates illustrated in Figure 4 [6] and Figure 5 [7]. Logic level of D flip-flop circuit design depicts in Figure 6 [8].

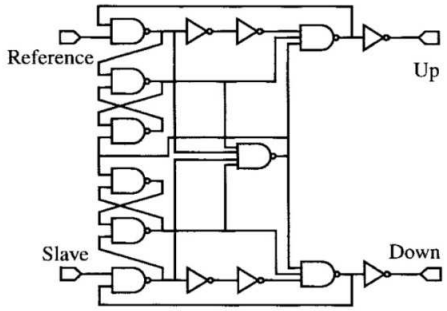

Figure 4: Conventional PFD At Logic Gate Level [6]

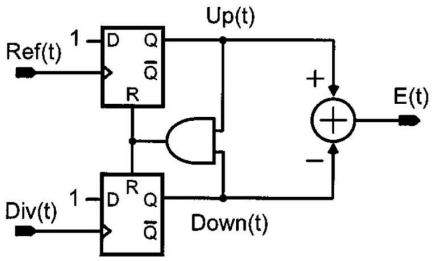

Figure 5: Conventional PFD Consists Of D Flip-Flop [7]

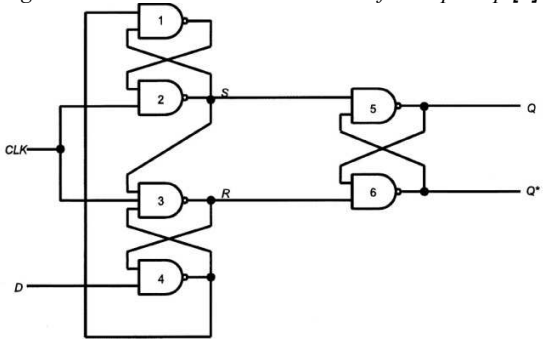

Figure 6: Standard D Flip-Flop [8]

TSPC DFF element utilized by Lee et al. 1999 and Krishna et al 2010 [9-10] can optimize system operating speed by modifying the circuit to operate under dynamic and sequential circuit or clocked circuit. Conventional positive edge triggered TSPC illustrated in Figure 7 built of 6 transistors only. A standard D flip-flop depicted in Figure 6 consists of 6 NAND gates (24 transistors) where large number of switching in the circuit caused high power dissipation.

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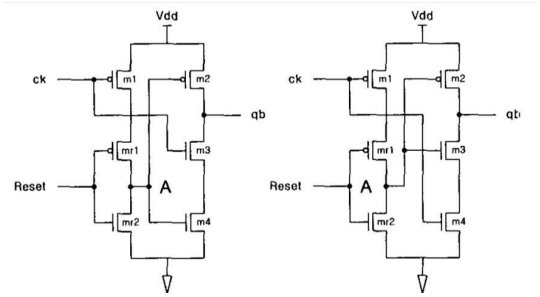

Figure 7: Dynamic TSPC D Flip-Flop [9]

Dynamic TSPC DFF achieved low power dissipation by having shortest signal routes in the circuit, reset time is increased from VDD to reset signal path before discharge to the ground. Internal switching node (A) is lowered to reduce dynamic power dissipation. This block phase noise analysis has been reported by Homayuon et al. (2013) [11]. High switching of gates during multiplication and fictitious transitions of internal nodes resulted in high power dissipation [12]. CMOS process technology of this work has advantage against the fabrication process due to integrated circuits simplification and fast switching time.

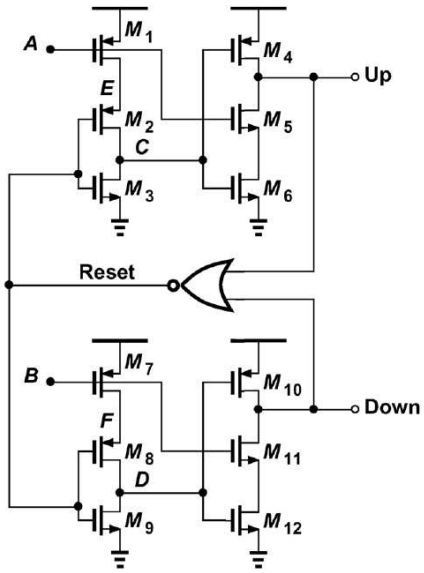

Figure 8: TSPC DFF PFD With NOR Gate [11]

3. METHODOLLOGY

Proposed pseudo-PMOS AND gate depicted in Figure 9 to replace the CMOS NOR gate and pseudo-NOR gate of the previous works into the dynamic PFD of this work. Pseudo-PMOS AND has less transistors to operate under low power and dissipates less power. This proposed Pseudo-PMOS AND gate is derived from Pseudo-NMOS NOR gate [8]. It built from 3 PMOS transistors to operate as AND gate. Pseudo-PMOS AND gate is identified as one of asynchronous dynamic circuit where the device bulk power is connected to the VDD thru N-well.

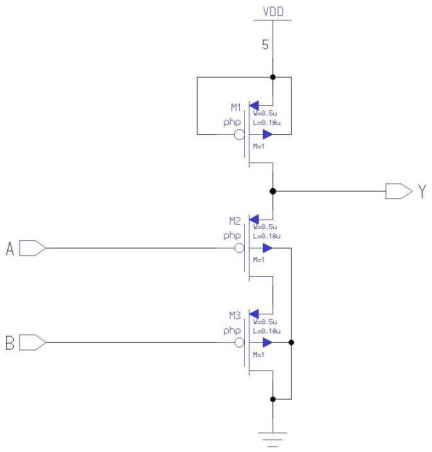

Figure 9: Modified Pseudo-PMOS AND

The proposed TSPC PFD utilized Homayuon et al. PFD which used for phase noise analysis depicts in Figure 10. The dynamic circuit (TSPC) is maintained while NOR gate is replaced with pseudo-PMOS AND of Figure 9.

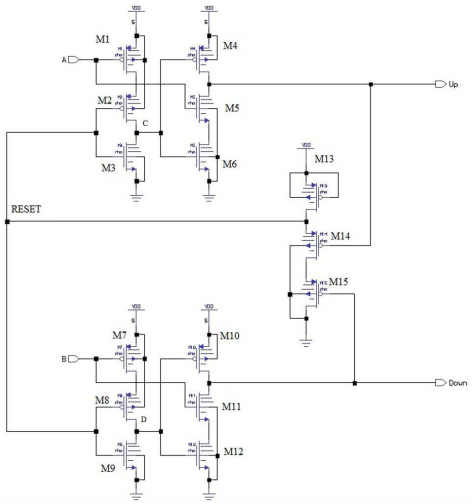

Figure 10: Proposed Dynamic PFD With Pseudo-PMOS AND Gate Schematic

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4. RESULT AND DISCUSSIONS

The proposed pseudo-PMOS AND gate element used in dynamic PFD schematic test-bench is shown in Figure 11. Input power supply is 1.8 V. The delay of input pulses for node A and B has been set to 1 to observe output wave response. Output waveform depicts in Figure 12 shown that the proposed module produced same output with typical AND gate. This proposed pseudo-PMOS AND dissipates only 13.997 pWatt power and it is suitable for high speed dynamic PFD used in DLL applications.

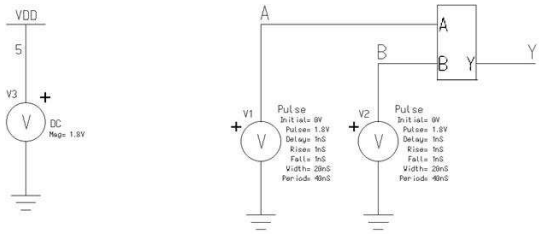

Figure 11: Pseudo-PMOS AND Test-Bench Schematic

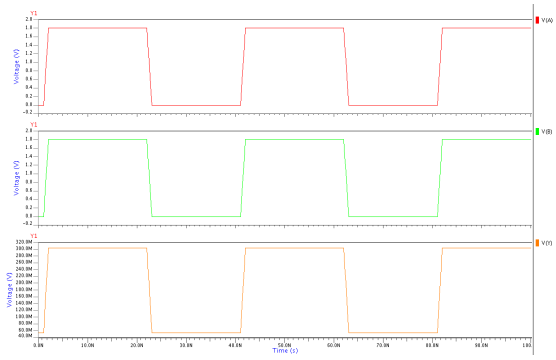

Figure 12: Pseudo-PMOS AND Output Waveform

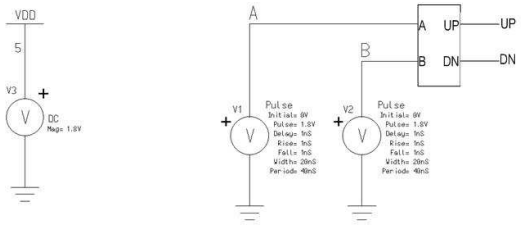

Figure 13: Proposed Dynamic PFD Test-Bench Schematic

Proposed TSPC PFD test-bench schematic consists of pseudo-PMOS AND illustrated in Figure 13. Noise transient is set to 1 GHz. Output wave form of matched inputs shown in Figure 14. The small current at the output UP/DOWN is 50 mV which is close to 0 V and formed approximately zero pulse width. This short pulse is due to the dynamic circuit behaviour and insignificant to the PFD and DLL circuit performance. Total power dissipation of this modified dynamic PFD achieved only 206 nWatt exhibiting the lowest among the rest of the designs implemented earlier. Figure 15 shows the noise transient of the dynamic PFD with pseudo-PMOS AND output UP/DOWN and input A/B waveforms. Noise transient pulses usually consist of a relatively short pulse. The source of these noise pulses is often channel interference. In this work, the noise transient of input A and B are unstable at the first 0.15 µs and affected output UP and DOWN directly. The unstable noise transient resolved quickly after 0.15 µs and give minimum impact to the PFD functionality.

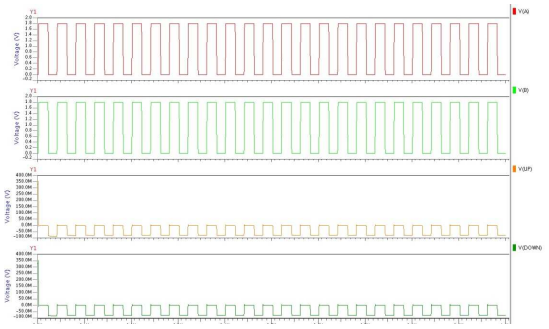

Figure 14: Proposed Dynamic PFD Output Waveform Matched Input

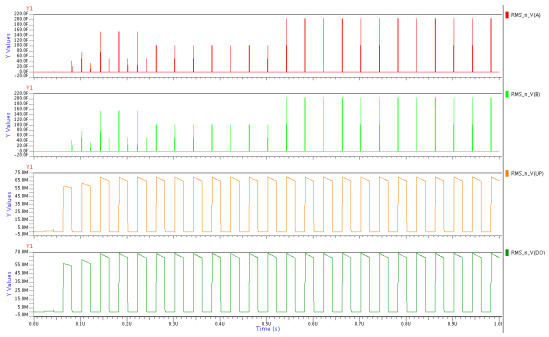

Figure 15: Proposed Dynamic PFD Noise Transient Output

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Figure 16 shows the respective layout mask design of proposed dynamic PFD drawn in 0.18 µm process technology. The highest metal used is Metal 3 in order to pull the input signals out and ready to connect at higher level signal routings. Parallel critical signals are spaced out more than its minimum spacing to avoid cross-talk, apposite ptaps and n-taps are placed to avoid massive latch-up between devices and practice short signal routings to minimize the RC effects.

In this work we found that the stability of the design in 0.18 µm process technology gives more flexibility for the researcher to design according to the application needs. Moreover, custom circuit design of the dynamic flip-flop has contributed to the low power operation and a compact active area. Conventional tri-state PFD has weaknesses of large power dissipations and delay variation due to current driving capabilities of the transistors frequently have issue to operate at low supply core voltage VDD. This problem has resolved in this high speed dynamic PFD as it satisfies the demand of digital circuit design and befitting a modern operating system running on a multi-gigahertz.

Table 1 shows circuit design performance comparison with previous works. This designed pseudo-PMOS dynamic PFD dissipates very low power and consume a very small layout design area compare to the reported works. This achieved mainly due to the less number of transistors utilized in the design. The PFD circuit functionalities are maintained with low input power supply voltage 1.8 V used in the simulated design.

This proposed pseudo-PMOS dynamic PFD that the circuit offered an alternative for any high speed and low power DLL applications. Design miniaturizations in downscaling CMOS process lead to circuit malfunction due to intrinsic effects and many other reasons. Hence further study of design performance in nanometer process technology is vital to ensure high PFD sensitivity in very low input power supply and maintain its functionality when operate in high speed DLL.

4. CONCLUSION

A low power, low noise and compact PFD design are continues challenge in the high speed analog and all-digital DLL systems and applications. A dynamic TSPC PFD with pseudo-PMOS AND gate is presented. The circuit design and simulation are done in 0.18 µm Silterra process technology environment. This proposed dynamic PFD design consists of 15 transistors and consumed 163.36 μm^2 layout area. In addition, the proposed dynamic PFD operates in 1G Hz frequency and retain all main functionality of conventional PFD. This proposed dynamic PFD exhibits 206 nWatt total power dissipation and suitable for high performance DLL application.

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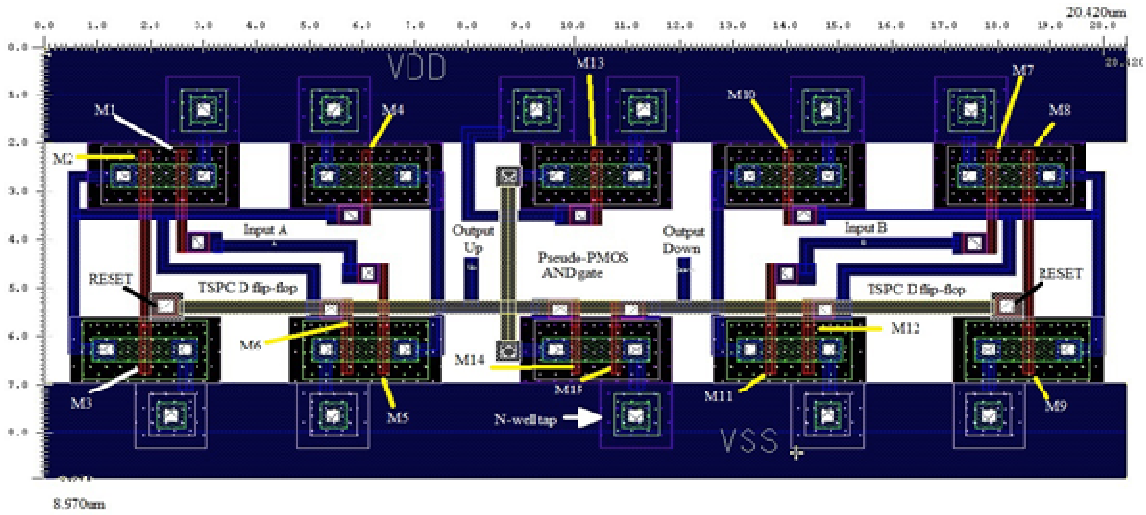

Figure 16: Proposed Dynamic Pfd With Pseudo-Pmos And Layout Design

Table 1: Performance Comparison

Type of PFD	This work	[19]	[20]	[11]	[11]	[21]	[22]
Process	0.18µm	0.18µm	0.13 µm	N/A	N/A	0.18µm	0.18µm
Voltage	1.8 V	1.8V	1.2V	N/A	N/A	1.8V	1.8 V
Area	163.36 μm^2	3.74 mm^2	N/A	N/A	N/A	N/A	N/A
No. of Transistors	15	150	26	32	16	N/A	24
Total Power Dissipation	206 nWatt	1.6 Watt	496 µWatt	0.24 mWatt	0.24 mWatt	2.24 mWatt	325 µWatt