Journal of Theoretical and Applied Information Technology
20th April 2015. Vol.74 No.2

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

DESIGN OF LOW POWER REDUCED WALLACE MULTIPLIER WITH COMPACT CARRY SELECT ADDER, HALF ADDER & FULL ADDER USING CMOS TECHNOLOGY

[1]P.RADHIKA, [2]Dr.T.VIGNESWARAN,
[1]Asst.Professor, Department of ECE, SRM University, Kattankulathur, Chennai, Tamilnadu, India.
[2]Professor, School of Electronics engineering, VIT University, Chennai, Tamilnadu, India.
Email: [1]radika.srm@gmail.com, [2]vigneswaran.t@vit.ac.in

ABSTRACT

The Wallace Multiplier is mainly used in the Arithmetic & Logic Unit (ALU) to perform the scientific computation in processors, controller etc... The existing multiplication technique like booth multiplier, array multiplier etc requires more time in multiplications. Hence Wallace Multiplier has been designed by using the parallel process to reduce the delay. The regular Wallace Multiplier requires more number of half adder and full adders in the reduction phase. So the chip size (Area) is high in the regular Wallace multiplier. The complexity reduced Wallace multiplier has been designed with less number of half adder and full adders. In this paper, the compact carry select adder, half adder and full adder are designed, which has been incorporated into the complexity reduced Wallace multiplier to reduce the area and delay than the existing reduced Wallace multiplier. The compact half adder and full adder are designed by using static CMOS technology with 6 transistors and 16 transistors instead of 12 transistors and 24 transistors. Also the compact carry select adder has been constructed based on compact half adder with 6 transistors, compact AND, OR and XOR gates with 4 transistors for each gate. So the proposed complexity reduced Wallace multiplier offers low power and less area than the existing Wallace multiplier. Simulation is performed by using Tanner Tool v14.1.

Key Words: *Static CMOS technology, Compact half adder & full adder, complexity reduced Wallace Multiplier, reduced carry select adder and Tanner Tool.*

1. INTRODUCTION

The optimization of power and area in digital circuits is very important to improve their performance. In Ripple Carry Adder (RCA), the sum for each bit position in basic adder is generated sequentially only after the preceding bit position has been summed & a carry propagates into the next location [7]. The regular CSLA contains two sets of Ripple carry adders for cin = 0 & cin = 1. The CSLA is used in many systems to reduce the propagation delay of carry by separately producing the multiple carries and then decide a carry to produce the sum [1].

The SQRT CSLA is used for various multiplier circuits in order to reduce the carry propagation delay. There are various combinations of CSLA available for achieving low area and low power. In two set of RCAs, One RCA can be replaced by either D-Latch or Binary to Excess1 code Converter (BEC) for providing efficient low computation and low area. In this paper, the design of SQRT CSLA is performed by using reduced half adder instead of full adders with optimized AND, OR and XOR gates. Hence, the area occupancy is reduced in proposed SQRT CSLA. Further to reduce power and area, this proposed SQRT CSLA (SQRT CSLA) and reduced full adder are incorporated into Wallace multiplier. The comparison of Wallace multiplier with conventional SQRT CSLA [5] and Wallace multiplier with proposed SQRT CSLA, full adder

Journal of Theoretical and Applied Information Technology
20th April 2015. Vol.74 No.2

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

using static CMOS logic are presented in this paper.

Result shows that Wallace multiplier with proposed SQRT Carry Select Adder and full adder occupies less area and consumes low power than the Wallace multiplier with the conventional SQRT CSLA.

The effective CSLA was proposed by using one RCA and D-Latch for providing partial sum and carry. The delay is reduced by D-Latch when compared to regular CSLA with Dual RCAs. In [3], D-latch in CSLA is replaced by Binary to Excess1 code Conversion (BEC) to provide partial sum and carry thereby it consumes less area, power and delay. This architecture is mostly used for FIR filter in order to reduce dynamic power consumption and meet the computational efficiency. The performance of above computation was done by CSLA with various combinations such as Dual RCA, One RCA & One D-Latch, One RCA and One BEC unit in [4]. The CSLA with One RCA and One BEC consumes lower area and delay when compared to other CSLA structures [4]. In [2], the AND-OR logic based CSLA is proposed to reduce the area and power utilization.

In this paper, the AND-OR logic based CSLA circuits is designed using static CMOS logic with less number transistors in AND gate OR gate, XOR gate, half adder for CSLA circuit. Also the optimized full adder circuit is designed based on static CMOS design with less number of transistors, which is incorporated into the Wallace Multiplier. The main objective of this work is to design a novel Wallace Multiplier with reduced CSLA and full adder based on static CMOS logic.

2. REDUCED CSLA USING STATIC CMOS LOGIC

In this paper, the design of reduced CSLA based on AND-OR logic is presented using static CMOS technology. Previously, several CMOS technique has been invented to reduce the number of transistors [8] such as GDI logic, Complementary logic, Minority logic, Majority Logic, Pass transistor logic, Ultra low power logic (combination of pass transistor logic and static CMOS logic) etc. But in this paper, only the static CMOS logic is used to design the CSLA [6].

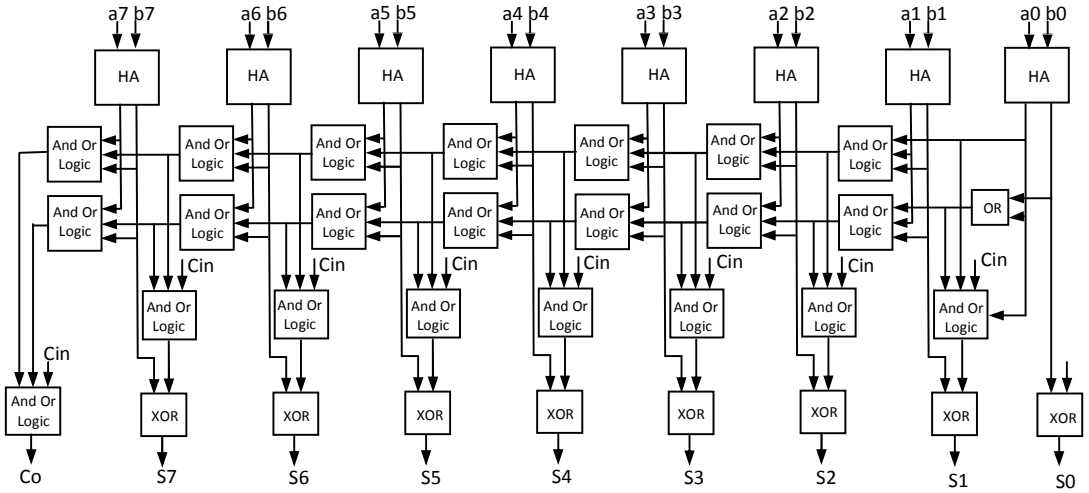

Fig.1 Block diagram of reduced CSLA based on AND-OR logic.

The block diagram of reduced CSLA is shown in fig.1. The reduced CSLA consists of half adder (HA), And Or logic and XOR circuits. The internal diagram of half adder, XOR gate, And Or logic is shown in Fig.2. The reduced AND gate is constructed using only 4 transistors instead of 6 transistors; OR gate is designed using 4 transistors instead of 6 transistors; And the reduced XOR gate is applied in the Reduced CSLA. The optimized half adder is constructed by using only 6 transistors based on static CMOS technology. All these gates and half adder are incorporated into reduced Carry select adder as shown in Fig.1 [10]. Comparison between reduced CSLA with regular AND, OR, XOR and half adder structure and proposed CSLA with optimized AND, OR, XOR and half adder structures is performed to analyze these working principle and power utilization.

Journal of Theoretical and Applied Information Technology
20th April 2015. Vol.74 No.2

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

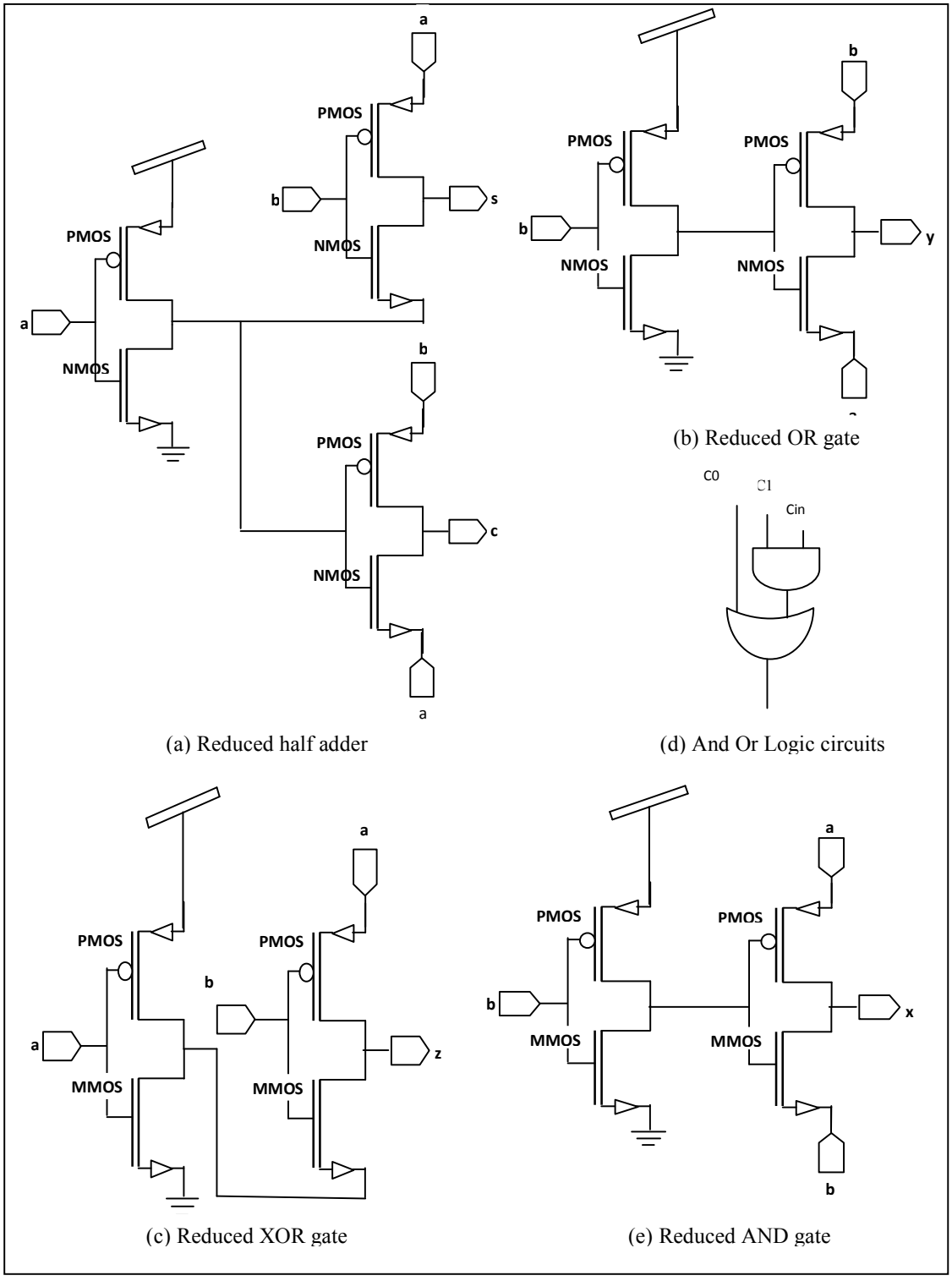

Fig.2 Circuit diagrams of reduced AND, OR, XOR gates, half adder and And Or Logic.

Journal of Theoretical and Applied Information Technology
20th April 2015. Vol.74 No.2

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

3. REDUCED FULL ADDER USING STATIC CMOS LOGIC

The reduced full adder structure is designed by using reduced half adder and XOR gate based on static CMOS logic. Till now there is no full adder design with 16 transistors based on static CMOS logic. In the static CMOS logic, the transistor reduction is very difficult when compared to the PTL (Pass Transistor logic), Complementary logic, GDI logic etc… The structure of reduced full adder is shown in fig.3. This reduced full adder is incorporated into the Wallace multiplier to generate the partial product in different stages. In the fig.3, inputs are a, b, c and the corresponding outputs are sum and carry. In Out ports are HS_1, HC1 and HC2.

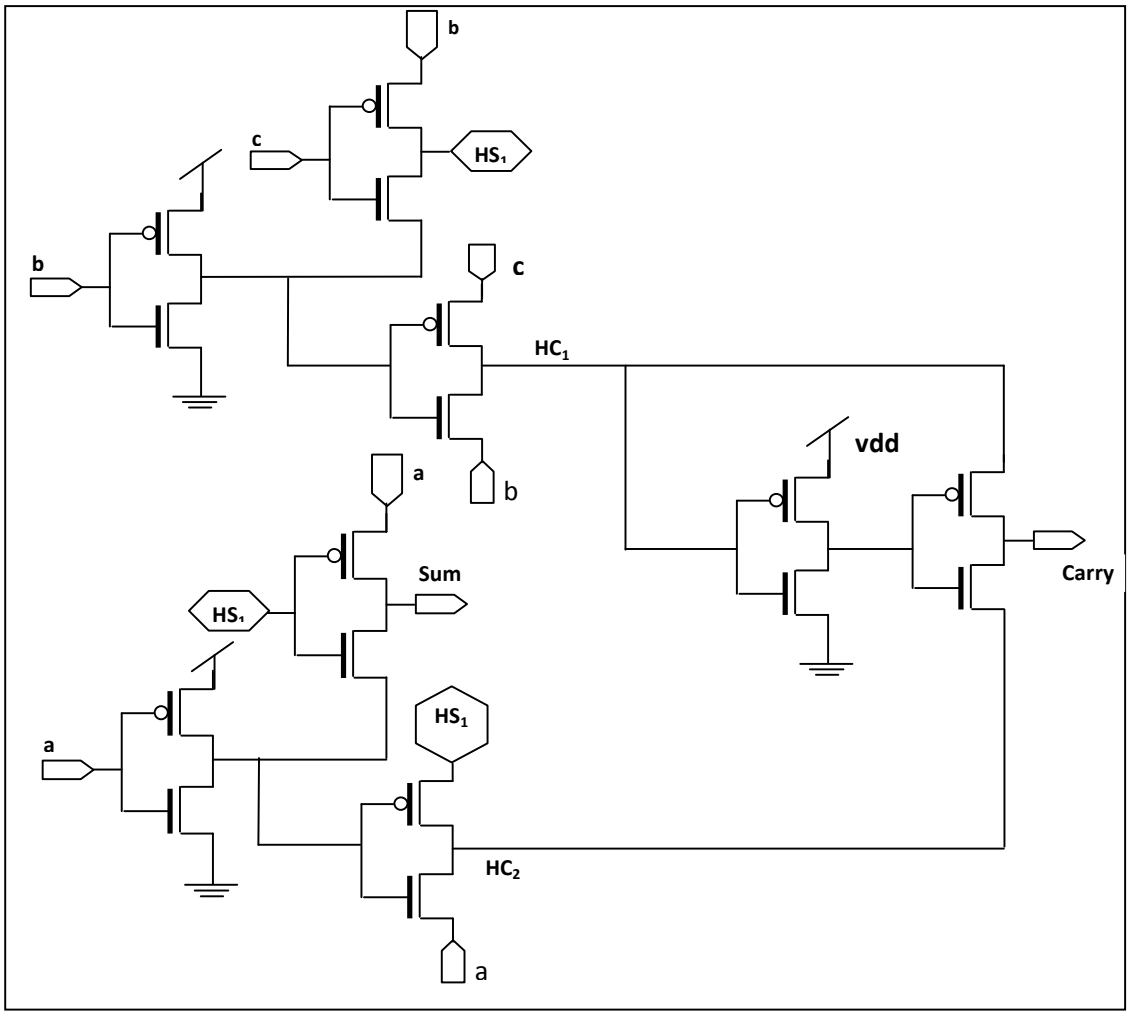

Fig.3 Structure of reduced full adder based on static CMOS logic.

4. WALLACE MULTIPLIER

A Wallace multiplier is a parallel multiplier which performs the array multiplication effectively [9]. Array multiplier has more number of gates to perform multiplication. Hence, it occupies large area for computation. In order to overcome this problem, Wallace multiplier with proposed SQRT CSLA is designed. The Wallace multiplier consists of of number of reduced half adders and full adders when compared to the conventional Wallace multiplier. In the modified circuit, N^2 AND gates form the partial products and they are arranged in an inverted triangle order. The matrix

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

is divided into three row groups in the reduced complexity Wallace multiplier.

1) Full adder is used for adding three bits.
2) Half adder is used for adding two bits
3) Single bit is moved to the next stage directly.

In the final stage of Wallace multiplier, proposed SQRT CSLA, reduced half adder and full adder are used instead of conventional SQRT CSLA, regular half adder and regular full adder for partial product generation & addition process. It reduces area as well as power by reducing the number of transistors.

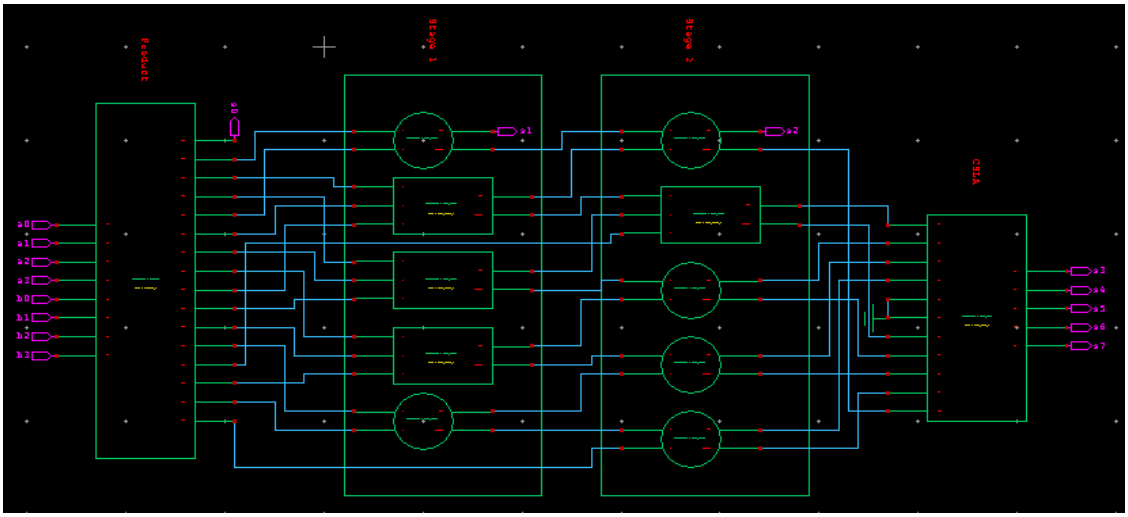

Fig. 4 Schematic Of 4x4 Wallace Multiplier Using Tanner.

Fig 4 shows Wallace multiplier structure. From the Fig.4, the multiplicands are a0, a1, a2, a3 & Multipliers are b0, b1, b2, b3. The corresponding outputs are s7, s6, s5, s4, s3, s2, s1, s0. Initially, 16 AND gates are used to generate the partial product. The first output s0 is generated directly during the partial product generation. Second output s1 is generated in the first stage and third output s2 is produced in the second stage. Similarly, the remaining outputs are generated in the final stages by applying the 5 –bit SQRT CSLA as shown in Fig.4.

5. RESULTS AND DISCUSSIONS

In this paper, the design of optimized Wallace multiplier with reduced SQRT CSLA and reduced full adder as well as half adder is presented to reduce the area and power utilization. Tanner Tool 14.11 is used to design the Wallace multiplier. Power consumption is calculated by using T-SPICE in Tanner. The area reduction is performed by calculating the number of NMOS and PMOS utilization. The comparison between existing and proposed design is shown in Table.1.

Table.1 Comparison Between Existing And Proposed Design For Area Utilization

Design	Number of PMOS		Number of NMOS		Total number of Transistors	
	Existing	Proposed	Existing	Proposed	Existing	Proposed
AND gate	3	2	3	2	6	4
OR gate	3	2	3	2	6	4
XOR gate	5	2	5	2	10	4
Half adder	8	3	8	3	16	6
Full adder	14	8	14	8	28	16
SQRT CSLA	239	130	239	130	478	260

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

4-bit Wallace Multiplier	419	228	419	228	838	456

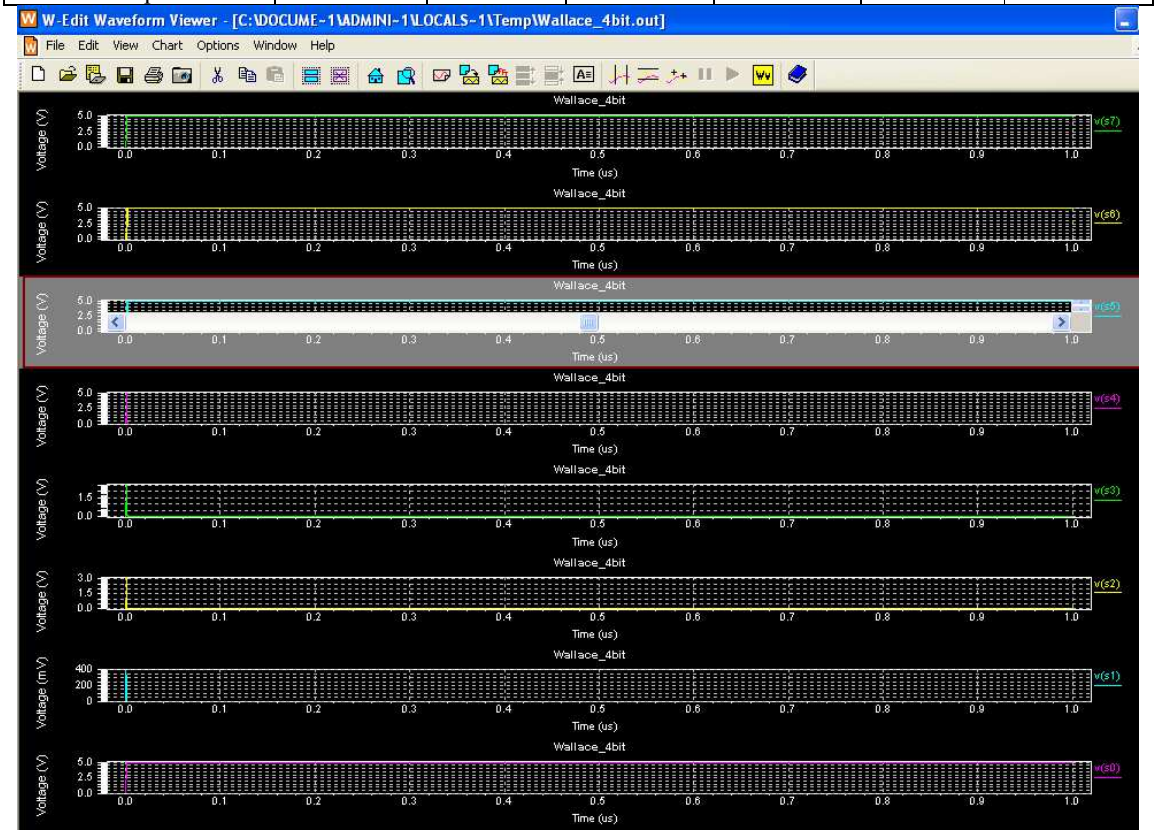

Fig.5 Simulation Output Of 4X4 Wallace Multiplier Using Tanner For A=1111 & B=1111.

From the Fig.5, the multiplicand a=1111 and Multiplier b=1111 is processed by Wallace multiplication technique to produce the exact output s=11100001. The functionality of the Wallace multiplier is proved using Tanner W-edit through waveforms. Also from the table.1, it is proved that the proposed Wallace multiplier provides 46% area reduction than the existing Wallace Multiplier.

Table.2 The Power Utilization Of 4X4 Wallace Multiplier

VDD (v)	Max Power (mw)	Min Power (uw)
2.5	25.3	30
2.0	16.9	19.8
1.5	11.9	12.7
1.0	10.6	8.29
0.5	10.5	4.165

From the Table.2, It is shows that the Wallace multiplier provides considerable reduction, when the VDD value reduces. The power reduction occurs from Mille watt to Micro watt. The optimum VDD level is 0.5. Because there is considerable reduction in 0.5 volt.

6. CONCLUSION

This paper presents the design of low area and low power Wallace multiplier using Tanner Tool v14.11 employing the transistor level optimization. The design established a novel approach to minimize silicon-area of Wallace Multiplier design by using a simplified SQRT CSLA, Full adder and half adder for low area and low power multiplication in order to reduce the power dissipation and chip size for the overall multiplier architecture. The proposed Wallace multiplier offers 46% area reduction and

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

mw to uw Power reduction, when compared to the conventional Wallace multiplier. The results point out that our design is suitable for best arithmetic and logical applications which need small chip size and low power consumption such as Digital communication, Digital Image Processing, DSP etc.

REFERENCES:

[1] He, Y., C. H. Chang, and J. Gu, "An area-efficient 64-bit square root carry-select adder for low power application", proceeding of IEEE Int. Symposium on Circuits System, vol. 4, 2005, pp. 4082–4085.

[2] Basant Kumar, M. and Sujit Kumar, P., "Area–Delay–Power Efficient Carry-Select Adder", IEEE Transactions on Circuits and Systems—II: Express Briefs, Vol. 61, No. 6, 2014.

[3] Wey, I.-C. C.-C. Ho, Y.-S. Lin, and C. C. Peng, "An area-efficient carry select adder design by sharing the common Boolean logic term", in Proc. IMECS, 2012, pp. 1–4.

[4] Ramkumar, B. and H. M. Kittur, "Low-power and area-efficient carry-select adder," IEEE Trans. On Very Large Scale Integr. (VLSI) Syst.", vol. 20, no. 2, 2012, pp. 371–375.

[5] Rajaram, S. and Mrs.K.Vanithamani, "Improvement of Wallace multipliers using Parallel prefix adders". Proceedings of 2011 International Conference on Signal Processing, Communication, Computing and Networking Technologies IEEE, 2011.

[6] Shuchi Verma and Sampath Kumar V.," Design & Analysis of Low Power, Area-Efficient Carry Select Adder" *ISSN: 2248-9622,* Vol. 4, Issue 3 (Version 1), March 2014, pp.53-55.

[7] Parhami, B., "Computer Arithmetic: Algorithms and Hardware Designs", 2nd ed. New York, NY, USA: Oxford Univ. Press, 2010.

[8] Parhi, K.K., "VLSI Digital Signal Processing''. New York, NY, USA: Wiley, 1998.

[9] Ron S., Waters and Earl E.Swartzlander "A Reduced Complexity Wallace multiplier reduction" IEEE transactions on Computers, 2010.

[10] Amit Kumar P., Ram Awadh M. and Rajendra Kumar N., "Performance Analysis of Novel Domino XNOR Gate in Sub 45nm CMOS Technology". WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS, Volume 12, Issue 2, February 2013.