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ERROR COMPENSATED FIXED WIDTH MODIFIED BOOTH MULTIPLIER FOR MULTIMEDIA APPLICATIONS

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ABSTRACT

Many multimedia and digital signal processing systems are desirable to maintain a fixed format and to allow little accuracy loss to output data. The objective of this paper is to design a fixed width modified booth multiplier with high error performance. And the need to derive an effective error compensation function that makes the error distribution more symmetric and centralized in the error equalized to zero. The compensation circuit is mainly composed of simplified sorting network and this can achieve a tiny mean and mean square error as compared to the other circuits. The odd even sorting networks used for error compensation are composed of appropriately connected comparators. The simplified form of sorting network consist of neither NAND, NOR, AND-OR INVERTER (AOI) and OR-AND-INVERTER (OAI). In fixed width modified Booth multiplication, to reduce the number of partial products by a factor of two, modified booth encoding is used. The software used for the simulation of this circuit is Altera-Quartus II. The RTL code is generated using the above software. The implementation of the circuit is done using DE1 board.

Keywords: *Booth Multiplier, mean square error, partial products.*

1. INTRODUCTION

Multipliers are always the fundamental arithmetic unit of all the multimedia applications and DSP systems for which high processing performance and low power dissipation are the most important objective. To achieve high performance, the modified Booth encoding [1]-[4] which reduces the number of partial products by a factor of two, through performing the multiplier recoding has been widely adopted. The n * n fixed width multipliers that generate only the n most significant product bits are utilized to maintain the fixed word size which allows a little accuracy loss to output data. By directly removing the adder cells the hardware complexity reduction and power saving can be achieved and computation of the n least significant bits of 2n –bit output product is also done. But in direct –truncated fixed width multiplier (DTFM) a huge truncation error will be introduced.

Various error compensation techniques are used to effectively reduce the truncation error, which add estimated compensation value to the carry input of the reserved adder cells, have been proposed. Two methods, constant scheme and adaptive scheme are used to produce the error compensation value. The truncation error of constant scheme is very large since it pre-computes the error compensation value and feeds them to the carry input of retained adder cells regardless of the current input data value. But in adaptive scheme [5] high accuracy is achieved by adaptively adjusting the compensation value according to the input data with little higher hardware complexity. However adaptive error compensation scheme are not applied for fixed width modified Booth multipliers directly since it is developed for fixed width array multipliers.

Hence several error compensation approaches [6] have been proposed to reduce the truncation error of fixed width modified Booth multipliers. By using statistical analysis and linear regression analysis the compensation value generated significantly reduces the mean error but the maximum absolute error and the mean square error are still large.

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The truncated parts of the product bit matrix of booth multiplication are divided into major group and a minor group depending on their effects on the truncation error. Booth encoded outputs are consumed to make the error compensation value. The fixed width modified Booth multiplier in [7] attains improved performance in terms of greatest absolute error and the mean square error. The smaller mean and mean square error represent that the error distribution is more symmetric to and centralized in the error equal to zero. In multimedia and DSP applications the final output are produced from accumulating a series of product rather than from a single multiplication operation hence truncation error is accumulated to produce a huge output error. To avoid this compensation value is computed which requires additional computations, the fixed-width multiplier with small mean and mean square error is largely expected to obtain more accurate output data.

In this paper high error compensated circuit for fixed width modified Booth is proposed. Therefore, the mean and mean square error can be reduced; hence the resultant fixed width multiplier is suitable for different applications. To achieve this goal, at first the partial product matrix of Booth multiplication is improved to decrease the partial product bits in the truncated portion of DTFM. Then the correlation among the Booth encoded outputs and the truncated product error of DTFM is examined and explored to derive an effective error compensation function, which can generate an approximation to the carry value generated by truncated portion of DTFM, to decrease the truncation error and make the error distribution as symmetric and centralized as possible. Finally a simple compensation circuit composed of simplified sorting network and some adder cells is developed according to the proposed error compensation function. Simulation and implementation results show that the proposed fixed width modified Booth multipliers achieves much higher accuracy.

2. BOOTH MULTIPLIER

2.1 Modified Booth Multiplier

Consider the multiplication of two n-bit signed number

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i \qquad (1)$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \qquad (2)$$

Table I
Modified Booth Encoding Table

b_{2i+1}	b_{2i}	b_{2i-1}	Operation	neg_i	two_i	one_i	$zero_i$	cor_i
0	0	0	+0	0	0	0	1	0
0	0	1	+A	0	0	1	0	0
0	1	0	+A	0	0	1	0	0
0	1	1	+2A	0	1	0	0	0
1	0	0	−2A	1	1	0	0	1
1	0	1	−A	1	0	1	0	1
1	1	0	−A	1	0	1	0	1
1	1	1	−0	1	0	0	1	0

By modified booth encoding which groups the bits of the multiplier into triplets, B can be expressed as

$$B = \sum_{i=0}^{n/2-1} M_i 2^{2i} = \sum_{i=0}^{n/2-1} (-2b_{2i+1} + b_{2i} + b_{2i-1}) 2^{2i} \qquad (3)$$

Where $b_{-1} = 0$ and $M_i \in \{-2, -1, 0, 1, 2\}$.

Based on the encoded results shown in table 1 the Booth encoder and the partial product generation circuit are adopted to choose one of multiple multiplicand -2A, -A, 0,A and 2A for generating each partial product row PPi where 0≤ i ≤ n/2-1 and aj bar is the complement of aj (0≤ j ≤ n-1). In *Table I.* Left shifting A by one bit achieves 2A. For negation, eac bit of A is inverted and an extra binary value '1' is added to the LSB of next partial product row. Adding '1' can be considered as a correlation bit Cori which indicates that partial product is PPi is positive if cori=0 or negative if cori=1. Further, the sign bit for partial product row must be extended upto (2n-1) bit position because each PPi row is represented in two's complementation.

Let us consider two 8 bit signed integers A=10101010; B=11100001. The two's complement of A is a=01010110, the two's complement of B is b=00011111. Let this b can be given as input to the booth encoder. Outputs of booth encoder are neg=0011, one=0001, two=0100, zero=1010, Cori=0010, the width of all these outputs is i=4 (0<=i<=3); where as i=n/2-1.

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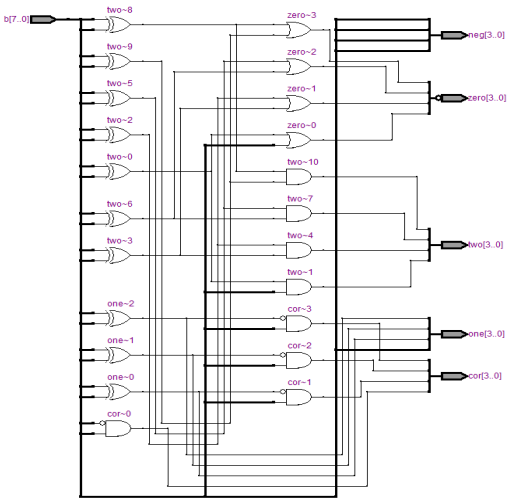

Figure 1: RTL View of Modified Booth Multiplier.

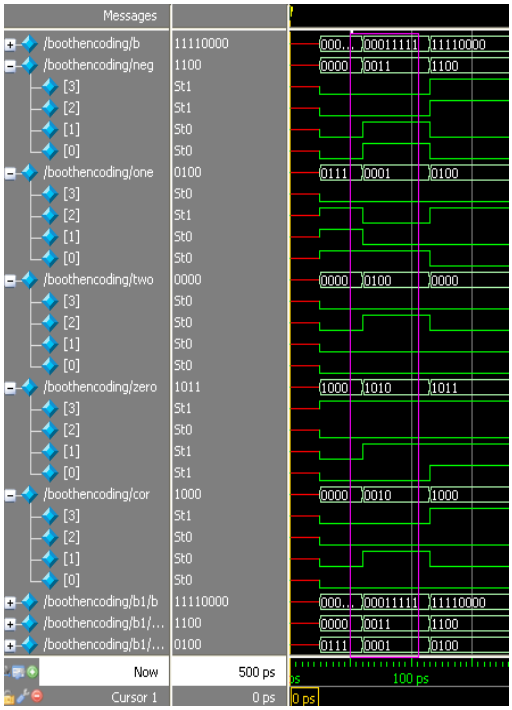

Figure 2: Simulation Output Waveform for Modified Booth Multiplier.

The two's complement of A i.e. a and abar=~a are given as inputs to partial product generation circuit. a=01010110; abar=10101001; here four registers are used namely, q, r, s, and t, to store the partial products generated from the circuit. No. Of partial products=i=4.

2.2 Partial Product Generation Circuit

The outputs i.e. q, r, s, and t are of 8-bits each with no sign extension bits. q=01010110; s0=0, ~s0=1 r=00000000; s1=0, ~s1=1; s=01010010; s2=0, ~s2=1; t=00000000; s3=0, ~s3=1;

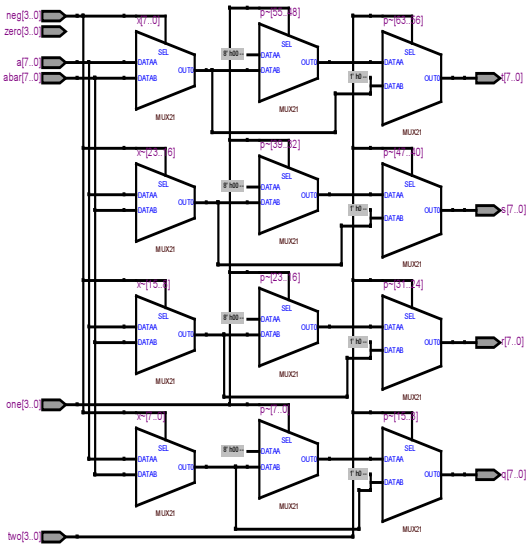

Figure 3: RTL View of Partial Product Generation Circuit.

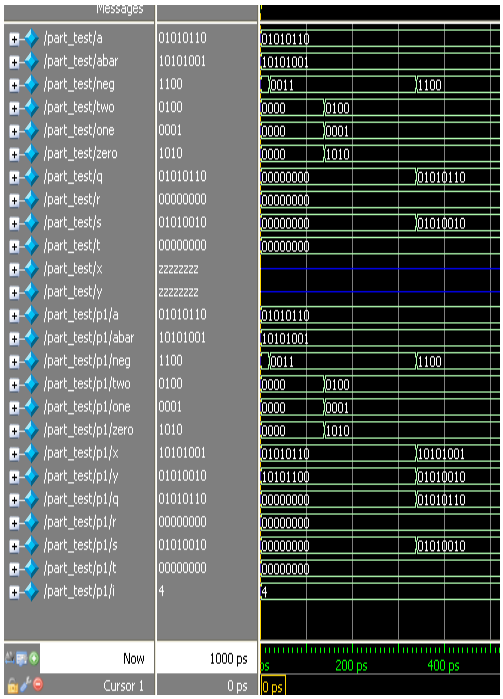

Figure 4: Simulation Output Waveform for Partial Product Generation Circuit.

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2.3 Partial Product Matrix For 8*8 Modified Booth Multiplication

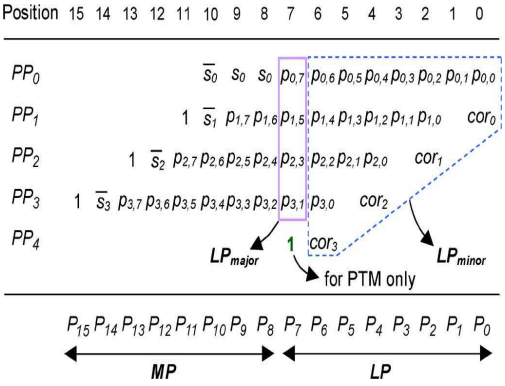

Figure 5: Partial Product Matrix for 8 × 8 Modified Booth Multiplication.

These additional sign bits affects the performance and power consumption of the multipliers. Hence Fig.5 illustrates the partial product matrix if 8×8 modified Booth multiplier with sign extension elimination technique to solve this problem. Here the partial product matrix can be divided into MP and LP, where LP is of two types namely, LP major and LP minor. According to DTFM, LP can be directly omitted but huge truncation error will be introduced. Hence in the propagated error compensated multiplier, only the partial product bits in LP minor are removed and carry value is propagated from LP minor to LP major, which is estimated by a simple circuit.

3. PROPOSED FIXED WIDTH MODIFIED BOOTH MULTIPLIER

3.1 Generation Of Error Compensation Function

Let sum (MP) and sum (LP) represent the sum of partial product bits in MP and LP then the output product P can be expressed as

$$P = A \times B = SUM(MP) + SUM(LP) \quad (4)$$

The sum (LP) can be obtained as

$$SUM(LP) = \delta \times 2^n \quad (5)$$

Where

$$\delta = \frac{1}{2}(p_{0,n-1} + \ldots + p_{n/2-1,1}) + \frac{1}{2^2}(p_{0,n-2} + \ldots + cor_{n/2-1}) + \ldots + \frac{1}{2^{n-1}}(p_{0,1}) + \frac{1}{2^n}(p_{0,0} + cor_0) \quad (6)$$

$$Let\ \theta_{major} = p_{0,n-1} + \ldots + p_{n/2-1,1} \quad (7)$$

Can be written as

$$\delta = \frac{1}{2}\theta_{major} + \theta_{minor} \quad (8)$$

Where

$$\theta_{minor} = \frac{1}{2^2}(p_{0,n-2} + \ldots + cor_{n/2-1}) + \frac{1}{2^n}(p_{0,0} + cor_0) \quad (9)$$

If partial products in LP are removed the most accurate error compensation value δ is the rounding value of δ that can be expressed as

$$\delta = \left[\frac{1}{2}\theta_{major} + \theta_{minor}\right]_r = \left[\frac{1}{2}(\theta_{major} + 1) + \theta_{minor}\right] \quad (10)$$

3.2 Post Truncuated Modified Booth Multiplier

Post-truncated modified Booth multiplier (PTM) can generate the most accurate error compensation value δ. By adding an extra '1' at the (n-1) th bit position of partial product matrix shown in fig 2 PTM can be achieved. Inspite of the advantages this results in hardware complexity and power consumption to standard modified Booth multiplier. Hence, a simple error compensation function whose output value approximates the most accurate error compensation value $\hat{\delta}$ is developed by the following steps. First, the partial product matrix of PTM shown in fig.2 is modified into a new matrix as shown in Figure 3.

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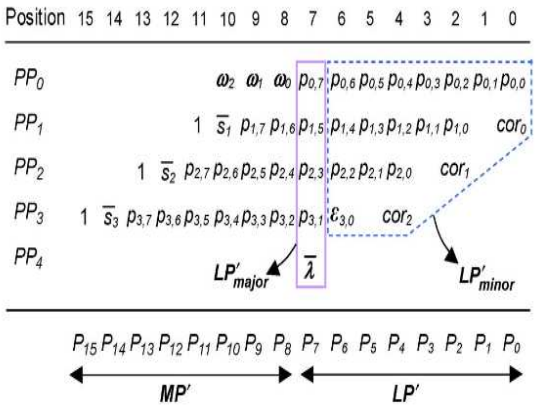

Figure 6: The Proposed 8 × 8 Modified Booth Partial Product Matrix.

Table II
Truth Table

b_{n-1}	b_{n-2}	b_{n-3}	$two_{n/2-1}$	$one_{n/2-1}$	$zero_{n/2-1}$	$cor_{n/2-1}$	$p_{n/2-1,0}$	$\varepsilon_{n/2-1,0}$	λ
0	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	a_0	a_0	0
0	1	0	0	1	0	0	a_0	a_0	0
0	1	1	1	0	0	0	0	0	0
1	0	0	1	0	0	1	1	0	1
1	0	1	0	1	0	1	$\overline{a_0}$	a_0	$\overline{a_0}$
1	1	0	0	1	0	1	$\overline{a_0}$	a_0	$\overline{a_0}$
1	1	1	0	0	1	0	0	0	0

The new matrix is obtained by adding the least significant bit Pn/2-1,0 of PPn/2-1 and cor n/2-1 in advance to generate a sum $\varepsilon_{n/2-1,0}$, carry λ at the (n-2) Th and (n-1) Th bit positions respectively. The expression for $\varepsilon_{n/2-1,0}$ and λ can be derived from the truth table shown in *Table II* as follows

$$\varepsilon_{n/2-1,0} = a_0 \wedge one_{n/2-1} \quad (11)$$

$$\lambda = \overline{(a_0 \wedge one_{n/2-1})} \wedge \overline{zero_{n/2-1}} \wedge b_{n-1} \quad (12)$$

Where $\wedge$ denotes AND operation. Since the weight of extra '1' located at the (n-1)th bit positioin of PTM is equal to the weight of λ,they can be added upto generated a sum $\overline{\lambda}$ and a carry λ which must be propagated to the nth bit position. Then the carry λ can be incorporated with the sign extension bits $\overline{s_0}\ s_0 s_0$ of PP_0 to produce the new partial product bits based on the *Table III*.

TRUTH TABLE FOR $\varepsilon_{n/2-1,0}$ AND λ

b_{n-1}	b_{n-2}	b_{n-3}	$two_{n/2-1}$	$one_{n/2-1}$	$zero_{n/2-1}$	$cor_{n/2-1}$	$p_{n/2-1,0}$	$\varepsilon_{n/2-1,0}$	λ
0	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	a_0	a_0	0
0	1	0	0	1	0	0	a_0	a_0	0
0	1	1	1	0	0	0	0	0	0
1	0	0	1	0	0	1	1	0	1
1	0	1	0	1	0	1	$\overline{a_0}$	a_0	$\overline{a_0}$
1	1	0	0	1	0	1	$\overline{a_0}$	a_0	$\overline{a_0}$
1	1	1	0	0	1	0	0	0	0

The expressions for carry $\overline{\lambda}$ and $\omega_2\omega_1\omega_0$ can be derived as

$$\overline{\lambda} = \overline{[(a_0 \wedge one_{n/2-1}) \wedge \overline{zero_{n/2-1}} \wedge b_{n-1}]} \quad (13)$$

$$\omega_2 = \overline{(s_0 \wedge \overline{\lambda})} \quad (14)$$

$$\omega_1 = \overline{\omega_2} \quad (15)$$

$$\omega_0 = \overline{[(s_0 \vee \overline{\lambda}) \wedge \omega_2]} \quad (16)$$

Where $\vee$ denotes the OR operation. Now generation off lbar (shown as $\overline{\lambda}$ in product matrix):

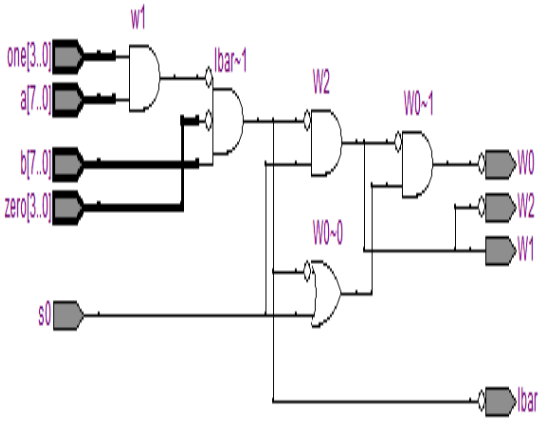

Figure 7: RTL View of Ibar Generation Circuit.

The inputs of this circuit are, since n=8; zero [3]=1; b [7]=0; one [3]=0; a0=0; s0=0; the outputs are lbar=1; W2=1; W1=0; W0=0; the error compensation function $\hat{\delta}$ can be defined as

$$\tilde{\delta} = \left[\frac{1}{2}[(\theta_{major} + \overline{\lambda}) + CA(LP')]\right] \quad (17)$$

$$= \left[\frac{1}{2}[\theta'_{major} + CA(LP'_{\min or})]\right] \quad (18)$$

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where $\theta'_{major} = \theta_{major} + \overline{\lambda}$ represents the approximate carry value propagated from LP' minor to LP' major. Sum (LP' minor) is the sum of partial product bits in LP' minor; $\sim C$ is substituted to obtain the expression as below

$$\tilde{S}(X) = \frac{1}{N(T_{AB}(X))} \sum_{(A;B)\in T_{AB}(X)} SUM(LP'_{\min or}) \quad (19)$$

where $N(T_{AB}(X)) = N(T_B(X))*2^n$ and $N(T_B(X))$ indicate the number of elements in $T_B(X)$. As $X = zbar_{n/2-1}*2^{n/2-1} + zbar_{n/2-2}*2^{n/2-2}+.....+ zbar_0*2^0$. $S(X)$ = floor function$(\sim S(X)/ 2^{n-1})$ = sum of (zbar[0], zbar[1], zbar[2], zbar[3]) Finally estimated carry = floor function $(\theta'_{major} + S(X))$.

3.3 Proposed Low Error Compensation Circuit

The SC-generator is the simple and efficient circuit for low error compensation. The input of SC generator is $zero_i$ for $0 \le i \le n/2 - 1$ and it will generate m output bits $\alpha_1, \alpha_2, ..., and\ \alpha_m$.

Φ	$s(\Phi)$				
	$n=8$	$n=10$	$n=12$	$n=14$	$n=16$
0	0	0	0	0	0
1	0	0	0	0	0
2	0	0	0	0	0
3	1	1	1	1	1
4	1	1	1	1	1
5	-	2	2	2	2
6	-	-	2	2	2
7	-	-	-	3	3
8	-	-	-	-	3

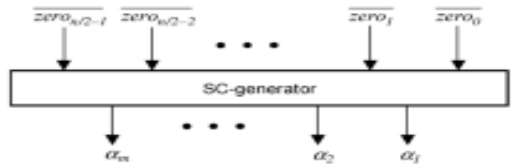

Figure 8: Block Diagram for Proposed Error Compensation Circuit.

SC-generator consists of odd even sorting network. After the estimation of carriers they are fed into LP`minor to produce the final fixed-width product. SC-generator works with the principle of odd even merge sorting algorithm. The network is given below

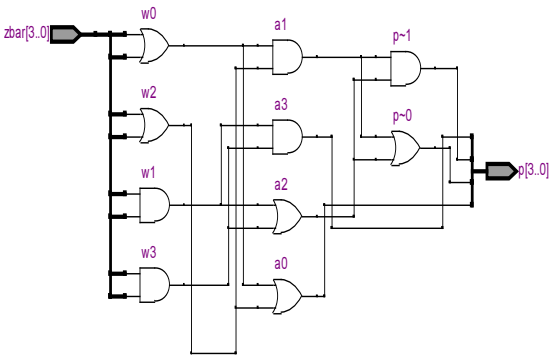

Figure 9: RTL view of Odd-Even Merge Sorting Network.

The inputs of SC generator are ~zero=zbar; zbar=0101, Here the larger weights are given MSB positions; in such a way they are sorted using the above circuit. The output is P =0011; to choose alpha value from p [0], p [1], p [2], p [3], the formula used is m=floor function of ((n/2-1)/2), m=floor function (1.5)=1, since n=8; alpha=p [m]=p [1]=1;

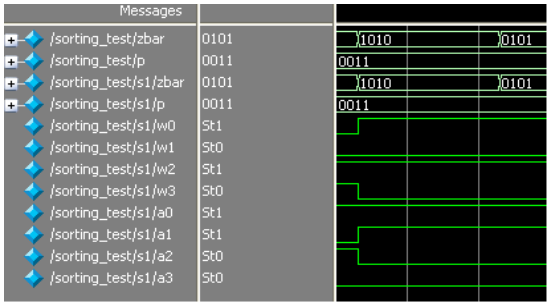

Figure 10: Simulation Waveform for Odd-Even Merge Sorting Network.

Now take four registers F, G, H, I of 16-bit length, frame all the required bits in that registers as per below partial product matrix, then accumulation is done using accumulator. The result obtained are as follows F=0000010001010110; G=0000110000000000; H=0011010100100000; I=11000000000000000.

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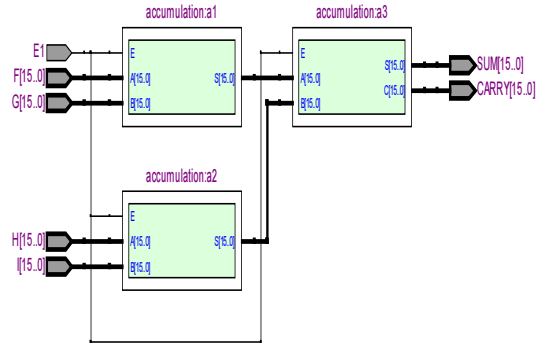

Figure 11: RTL View of Accumulator.

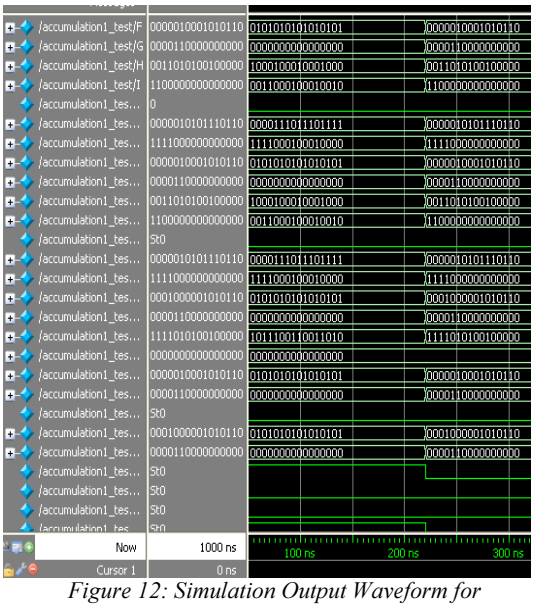

Figure 12: Simulation Output Waveform for Accumulation.

Now finally add lbar and alpha to the SUM[6], then truncate SUM[15:0] to SUM[15:7]. Finally making the widths of SUM, lbar, alpha same by appending zeros so that it will be very easy to add. Now as a result SUM=000001010(9bits); Lbar=000000001; P[2]=alpha=000000000. Now again add all three variables to get a 9bit output out of which most MSB 8 bits as final output. Thr RTL view of Adding Sum, lbar, alpha using Accumulator is shown below in Figure 13. The ouput is final(8bits)=11100110.

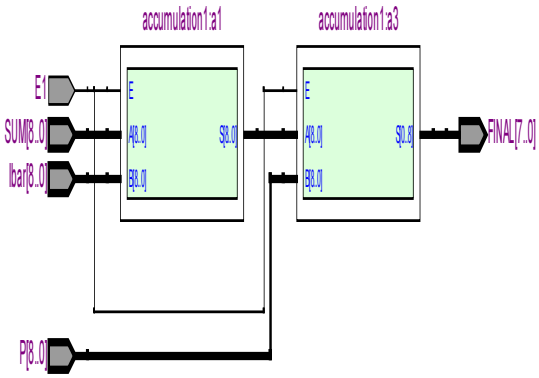

Figure 13: RTL View of Accumulator.

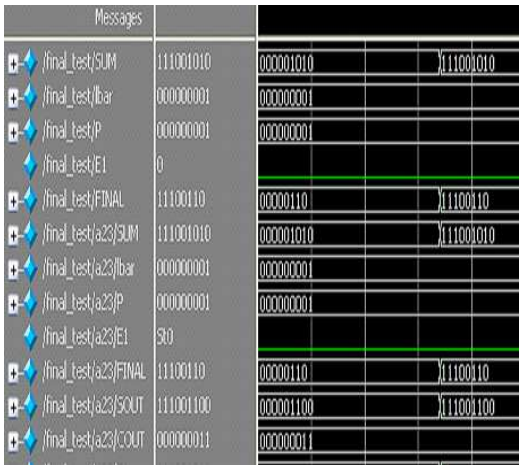

Figure 14: Simulation Output Waveform for Accumulation.

3.4 Power Analysis

The power analysis is done using Quartus simulator and optimum power is calculated. Power in a system is mainly composed of static and dynamic power. The dynamic power is due to the switching activity of the signals and the output capacitance in the circuitry. For **n=8** the experimental results are as follows;

PowerPlay Power Analyzer Status	Successful - Sun Nov 13 05:44:25 2011
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	booth
Top-level Entity Name	booth
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	348.23 mW
Core Dynamic Thermal Power Dissipation	2.98 mW
Core Static Thermal Power Dissipation	47.87 mW
I/O Thermal Power Dissipation	297.38 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

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PowerPlay Power Analyzer Status	Successful - Sun Nov 13 06:54:47 2011
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	lambda
Top-level Entity Name	lambda
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	75.86 mW
Core Dynamic Thermal Power Dissipation	0.11 mW
Core Static Thermal Power Dissipation	47.37 mW
I/O Thermal Power Dissipation	28.38 mW
Power Estimation Confidence	Medium: user provided moderately complete toggle rate data

PowerPlay Power Analyzer Status	Successful - Sun Nov 13 07:30:59 2011
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	sorting
Top-level Entity Name	sorting
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	69.14 mW
Core Dynamic Thermal Power Dissipation	0.03 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	21.76 mW
Power Estimation Confidence	Medium: user provided moderately complete toggle rate data

PowerPlay Power Analyzer Status	Successful - Sun Nov 13 08:02:16 2011
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	partial
Top-level Entity Name	partial
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	358.04 mW
Core Dynamic Thermal Power Dissipation	7.35 mW
Core Static Thermal Power Dissipation	47.88 mW
I/O Thermal Power Dissipation	302.81 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

PowerPlay Power Analyzer Status	Successful - Sun Nov 13 08:14:30 2011
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	accumulation
Top-level Entity Name	accumulation
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	494.52 mW
Core Dynamic Thermal Power Dissipation	12.62 mW
Core Static Thermal Power Dissipation	48.15 mW
I/O Thermal Power Dissipation	433.76 mW
Power Estimation Confidence	Medium: user provided moderately complete toggle rate data

PowerPlay Power Analyzer Status	Successful - Sun Nov 13 08:06:06 2011
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	finaladd
Top-level Entity Name	finaladd
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	293.07 mW
Core Dynamic Thermal Power Dissipation	3.02 mW
Core Static Thermal Power Dissipation	47.76 mW
I/O Thermal Power Dissipation	242.28 mW
Power Estimation Confidence	Medium: user provided moderately complete toggle rate data

4. CONCLUSION

In this paper error compensated fixed width modified Booth multiplier has been proposed. In the proposed paper, the partial product matrix of Booth multiplication was slightly modified and an effective error compensation function was derived. This compensation function makes the error low; leading the error compensated modified Booth multiplier with low error. In addition, a simplified sorting network has been designed to realize the compensation function.

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