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DESIGN OF HIGH SPEED VEDIC MULTIPLIER WITH PIPELINE TECHNOLOGY

Y. NARASIMHA RAO, DR. GSVP RAJU, PhD, Prof. PENMETSA V KRISHNA RAJA, PhD
Assistant Professor,Dept Of It, Gitam University, Visakhapatnam, Ap, India
Professor, Department Of Computer Science, Andhra University, Visakhapatnam, Ap, India
Aims College Of Engineering, Mummidivaram, Amalapuram , East Godavari Ap, India

ABSTRACT

In many digital computers multipliers plays vital role to improve the performance of the system. The speed of the processor greatly depends on high speed multipliers. On the other hand pipeline technology plays an important role in present parallel computers in improving the speed of the computer. In the present paper high speedVedic multiplier is designed and analysed by inserting a pipeline in the process of computation.The computation speed is considerably improved with pipeline when compared with conventional Vedic multiplier. The proposed pipelined Vedic multiplier was implemented in TSMC 65nm CMOS Technology consumes 57mWatts power when operated at 100MHz.

Keywords: *Pipeline, Vedic Multiplier, Throughput, High Speed,*

I. INTRODUCTION

The introduction part is divided into two sections. The first section discussed about the scope of multipliers and types of multipliers and in the second section discussed about pipeline concept. To achieve higher throughput in arithmetic operations is important to achieve the desired performance in many real-time applications [1]. In the recent days the multiplication circuit plays an important role in evaluating the performance of the computer. Along with this designing a fast multiplier is also a key constraint to the developers.But this is highly essential to develop fast multipliers with less time delay, power consumptionand high throughput [1, 2,5].

1.1 Multiplier

Multipliers are very important processing elements in many types of digital systems and computers. With effective multiplication the speed of the arithmetic operation can significantly improvewhich further saves the system time. Multipliers are used in many types of systems such calculator, microprocessors, mathematical co-processors, floating point unit, DSP processors, MAC, Digital filters, PID controllers and many other scientific devices.

Digital multiplication is a sequence of additions carried out on partial products. This partial product array is then summed by using a Carry Propagate Adder (CPA). Different arithmetic techniques are used to implement digital multipliers. Most techniques involve in computing partial products and summing all partial products. This is similar to conventional multiplication technique. A cumbersome process is done in evaluating the partial product, shifting and adding all partial products. There are some multiplication techniques which are actively involving to reduce the number of shift and additions in evaluating the final product. For instance in Booth multiplication shown in figure 2, the number of shifts and partial products computations are reduced. In booth algorithm a group of consecutive zeros in the multiplier requires no generation of newpartial product [14].

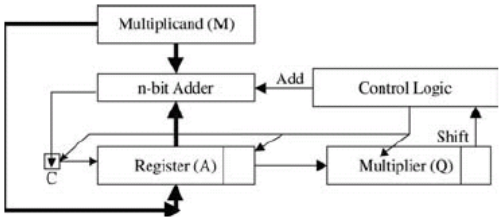

Figure 1: Conventional Shift-Add Multiplication

In this figure 1, the control logic is used to determinethe operation to be performed depending on the least significant bit in Q. An n-bitadder is used to add the contents of registers A and M.

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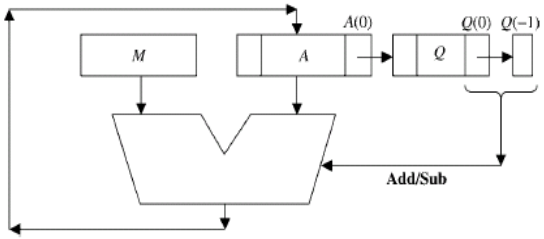

Figure 2: Hardware Structure For Booths Multiplication

The booth hardware shown in figure 2 consists of an ALU that can perform the add/sub operation depending on the two bits Q(0)Q(-1). A control circuitry is alsorequired to perform the Arithmetic shift Right (AQ) and to issue the appropriate signals needed tocontrol the number of cycles[14].

In the present work a Vedic multiplier is designed and analysed with Cadense tool. The conventional Vedic multiplier is compared with pipeline technology.In the present work the throughput is concentrated to improve the execution performance. In the present work, it is observed that the throughputof the traditional Vedic multiplier is less than the pipeline Vedic multiplier technique. This limitation of throughput can be overcome by inserting pipeline stages into Vedic multiplier at appropriate positions as shown in figure 8.In pipeline technology pipeline stages are inserted between individual Ladner Fischer adder (LFA) under Parallel Prefix Adder (PPA) structure.

In general multipliers are classified into three types [12].

a) Serial Multiplication: They are simple in structure as shown in figure 1. Both operands are entered in serial manner. However the speed is poor due to the operands entered sequentially. These multipliers are slow and small.

b) Parallel Multiplication: It is a high speed multiplier shown in figure 3 and incorporated with most advanced digital systems. Parallel multiplier is used in many algorithms [11].

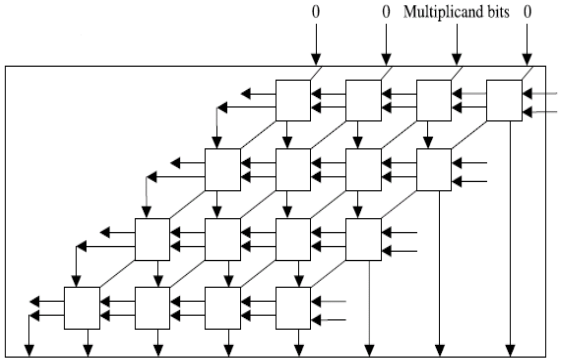

Figure 3: Parallel Multiplier Implementation

c) Serial-Parallel Multiplier: The entire multiplier input multiplied with one bit of the multiplicand in each step and results added with contents of Accumulator. It consumes less time and space. These multiplies are used when there is a demand for high speed and small area [15].

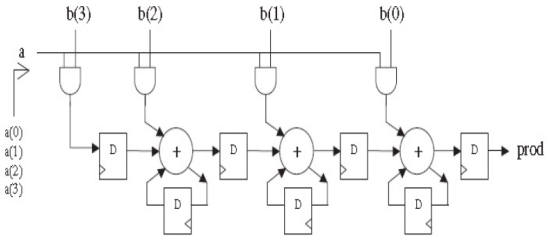

Figure 4: Serial-Parallel Multiplier

1.2 Pipeline

The execution performance is improved with pipeline when compared with sequential traditional execution. In a pipeline a task is divided into subtask and subtasks are executed simultaneously. In Vedic multiplier the multiplier and multiplicand are subdivided and applied at individual stages of pipeline. The parallel multiplier such as Vedic multiplier effectively solves a 4bit or 8bit multiplication on 8-bit processor. Sometimes lower word length microprocessor alone cannot compute higher bit multiplication. For large scale computation pipeline is the best solution to perform faster operation.In the enhanced method a pipeline is incorporated to carry the MSB of the operands. This is shown in the enhanced method of section 3. Generally basic pipeline consists of latches and stagesas shown in figure 5. The stages are the intermediate logic elements, where computations are performed. The results of these computation

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elements are feed forward to the next stages by latches. The operands which are left for computations in the next machine cycle are also feed forward through latches to next stages [9][10].

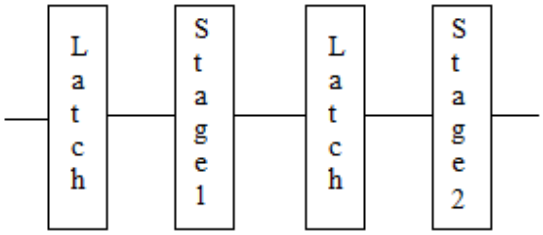

Figure 5: Basic Pipeline Diagram

2. EXISTING METHOD

In the present paper a parallel type Vedic multiplier is considered and studied its operation. Before discussing Vedic multipliers, let us have a brief introduction about parallel multipliers.

2.1 Different parallel multipliers

a) VEDIC Multiplier

In Vedic multiplier, the least significant bit of the product is produced by multiplying least significant bits of multiplier and multiplicand. Then, the LSB of the multiplicand multiplied with the next higher bit of the multiplierand the produced partial product is added with the product of LSB of multiplier and next higher bit of the multiplicand [16]. This is also called crosswise multiplication. The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position. Next, all the four bits are processed with crosswise multiplication and addition to give the sum and carry [6].

b) Column Bypass Multiplier

In this multiplier the operations in a column can be disabled if the corresponding bit in the multiplicand is zero. This means if the input bit coefficient is zero, corresponding column of adders need not be activated. The adders of this multiplier, however perform summation of the zero partial products and, as result, exhibit redundant signal switching. The increased activities of the internal nodes results in unnecessary power dissipation. To disable this adder columns we have to bypass the partial product of previous adder column to next adder column[12].

c) Multiplier using Different Compressors and Adders

For higher order multiplications, a huge number of adders or compressors are to be used to perform the partial product addition. We have reduced the number of adders by introducing special kind of adders that are capable to add five/six/seven bits per decade. These adders are called compressors. Binary counter property has been merged with the compressor property to develop high order compressors. Uses of these compressors permit the reduction of the vertical critical paths. These compressors make the multipliers faster [7].

1.3 Vedic Multiplier

Ancient Indian mathematicians have designed different serial and parallel multipliers. Out of which Vedic multiplier is fast parallel multiplier when compared with other multipliers.

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya Veda (book on civil engineering and architecture), which is a veda (supplement) of Atharva Veda. It describes various mathematical terms including arithmetic, geometry, trigonometry, quadratic equations, factorization and even calculus. His Holiness JagadguruShankaracharyaBharati Krishna Teerthaji Maharaja (swamiji) (1884- 1960) comprised and gave mathematical explanation while discussing it for various applications. Swamiji constructed 16 formulae and 16 sub formulae after extensive research in Atharva Veda [3][8].

A general block diagram of Vedic multiplier is shown in figure 6. In the diagram two 8-bit numbers A and B are taken into consideration and connected their LSB and MSB to individual 4-bit multipliers. Unlike traditional multiplier here all digits at different decimal places are taken for calculation and simultaneously generating partial products as shown in figure 6.

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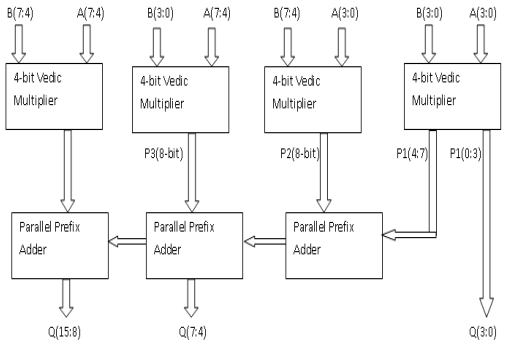

Figure 6: Block Diagram Of 8-Bit Vedic Multiplier

Vedic Multiplier is implemented with *vertical and cross wise* multiplication principal which is shown in figure 7. This is a fully parallel multiplier and the methodology is as shown below. The process used in vedic multiplier is shown below [13].

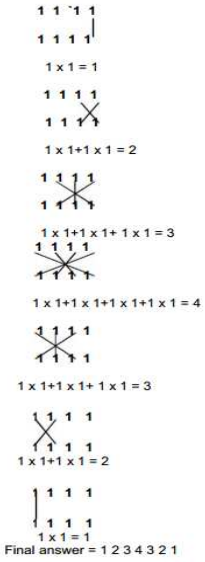

Figure 7: Vertical and Cross wise multiplication in Vedic multiplier

3. PROPOSED METHOD

From the above section its is concluded that all digits are simultaneously considered for product and so it is called parallel multiplier. Although vertical and cross wise multiplication is very fast, it may fail at large number multiplication. Because for example in figure 6 the third PPA (Parallel Prefix Adders) which is producing Q(15:8) has to wait for previous PPA results Q(7:4) and Q(3:0). Before it receives previous PPA results it has to accept the B(7:4), A(7:4) multiplier result. It may generate a faulty output. This can be avoided my proper clock synchronization at PPAs or by adding extra circuits between multipliers and PPAs. Selecting appropriate clock circuit at different PPA stages in large number multiplication is cumbersome. Instead of that in the present work we propose to add an extra circuit between multipliers and stages of PPAs. We have incorporated pipelines as extra circuit. These pipelines are used to solve two purposes. One is to minimize the waiting delay at higher PPA stages. The other advantage is, while computing one product at PPA the multipliers can fetch third and fourth number for next multiplication. This is greatly increasing the fetching rates of the input data, and performs multiple operations in few machine cycles. We are further developing this system to reduce the machine cycles. A proposed Vedic multiplier with pipeline is shown in figure 8.

In the present paper the performance of Vedic multiplier and Pipelined Vedic Multiplier is compared and analysed in various dimensions. In Vedic multiplier Parallel prefix adder is used as it supports good through put when compared with other fast adders [4].

4. RESULTS

The traditional Vedic multiplier with Pipelined Vedic multiplier is compared with the simulation tools such as Cadens Compiler v08.10-s108_1. The cell area, power consumption and propagation delay is analysed and presented in this section. The number of slices and power consumption at individual cell such as individual adder and multiplier is analysed. The individual cell analysis will help to evaluate the total performance of the Pipeline Vedic Multiplier easily. Not only it helps to evaluate the performance, but it also helps for future investigation to reduce power consumption and cell area. Some of the simulated output screen shots for Vedic and Pipelined Vedic Multiplier are presented in this section. An RTL Schematic generated in Cadense of Vedic Multiplier is shown in figure 9. Table 1is showing total cell areas which comprises of three parallel prefix adders a1, a2, a3and four multipliers v1,v2,v3,v4in a traditional 8X8 Vedic multiplier. For instance Table 1 is showing an ordinary Vedic

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multiplier require 348 cells and 1836nm. Table 1 describing the power consumption at individual cell and observe total power consumption by all cell area is 31.1 mW. The Vedic multiplier performance is further improved by proposed method by inserting pipeline and Schematic of the circuit is shown in the following figure 10. The throughput and speed of the Vedic multiplier is further improved with pipeline concept. After inserting the pipeline the total cell area obviously increases as shown in Table 1 and observed 415nm.Table 1 is showing power consumption in pipelined Vedic Multiplier is 57.3.Figure 11 is showing the simulated results of 8X8 Pipelined Vedic Multiplier output. Propagation delay of 10ns is observed through the proposed circuit, which proves a faster operation and through put when compared with traditional Vedic Multiplier. Figure 12 is showing a layout of the proposed circuit obtained from Cadense simulation tool.Figure 13 to Figure 14 are showing the simulation results generated after synthesis, and these results are consolidated in Table 1.

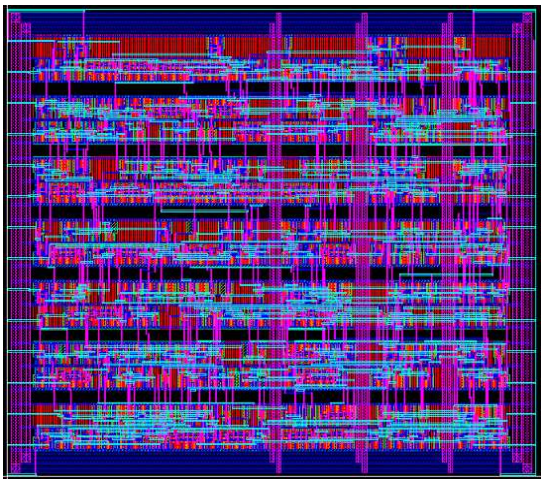

Figure 12: Pipelined Vedic Multiplier 8x8 Layout Diagram

5. CONCLUSION

High speed data rates are achieved in pipeline based Vedic multiplier. Higher throughput is observed in the proposed method when compared with Traditional Vedic Multiplier. Data for next multiplication are fetched while it is computing product for present numbers. Although the circuit design complexity increased here, it is more advantageous when compared with current technologies and trend requirements. By implementing advanced pipeline techniques in the circuit the data speed can be improved further. Further, power optimization techniques can be adopted to reduce the power consumption.By modifying the circuit at transistor level, the cell area can be reduced and this minimizes the power consumption.

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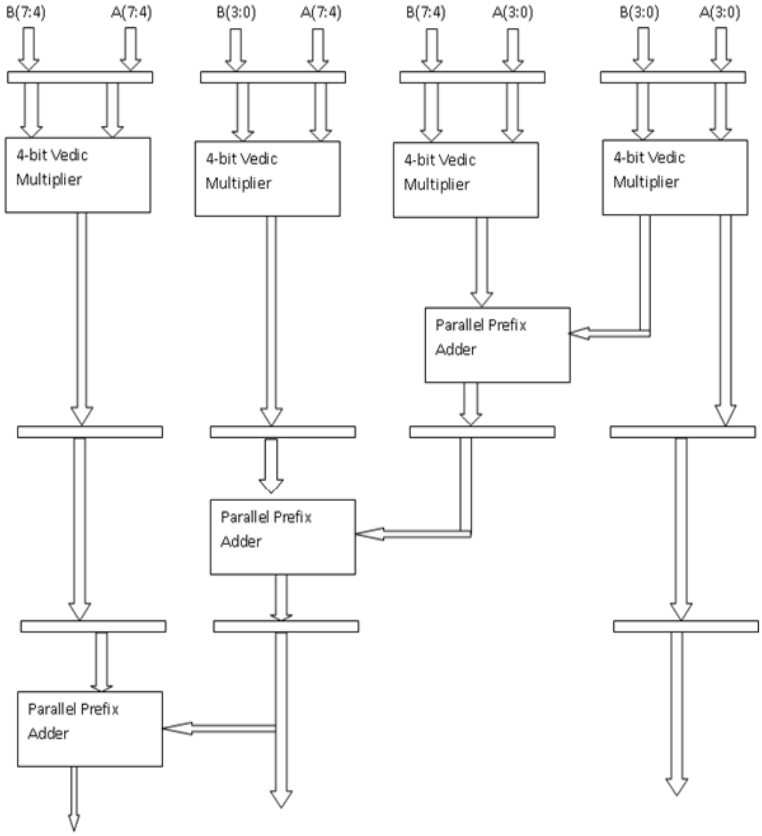

Figure 8: A Proposed High Speed Multiplier With Pipeline

Table 1: Comparative Readings Of Pipeline Vedic Multiplier With Traditional Vedic Multiplier

	Area	Power Consumption	Throughput
Regular Vedic Multiplier	348 Gates	31.1mW	15ns
Pipelined Vedic Multiplier	415 Gates	57.3mW	10ns

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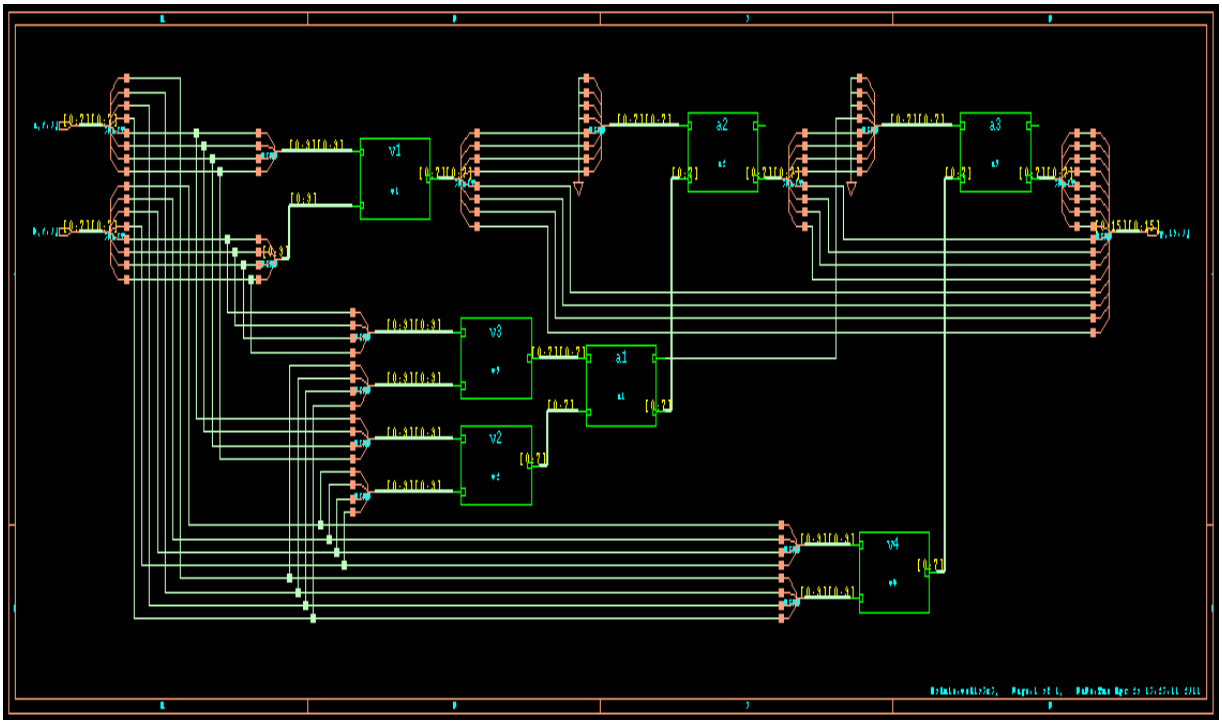

Figure 9: Schematic Of Traditional Vedic Multiplier

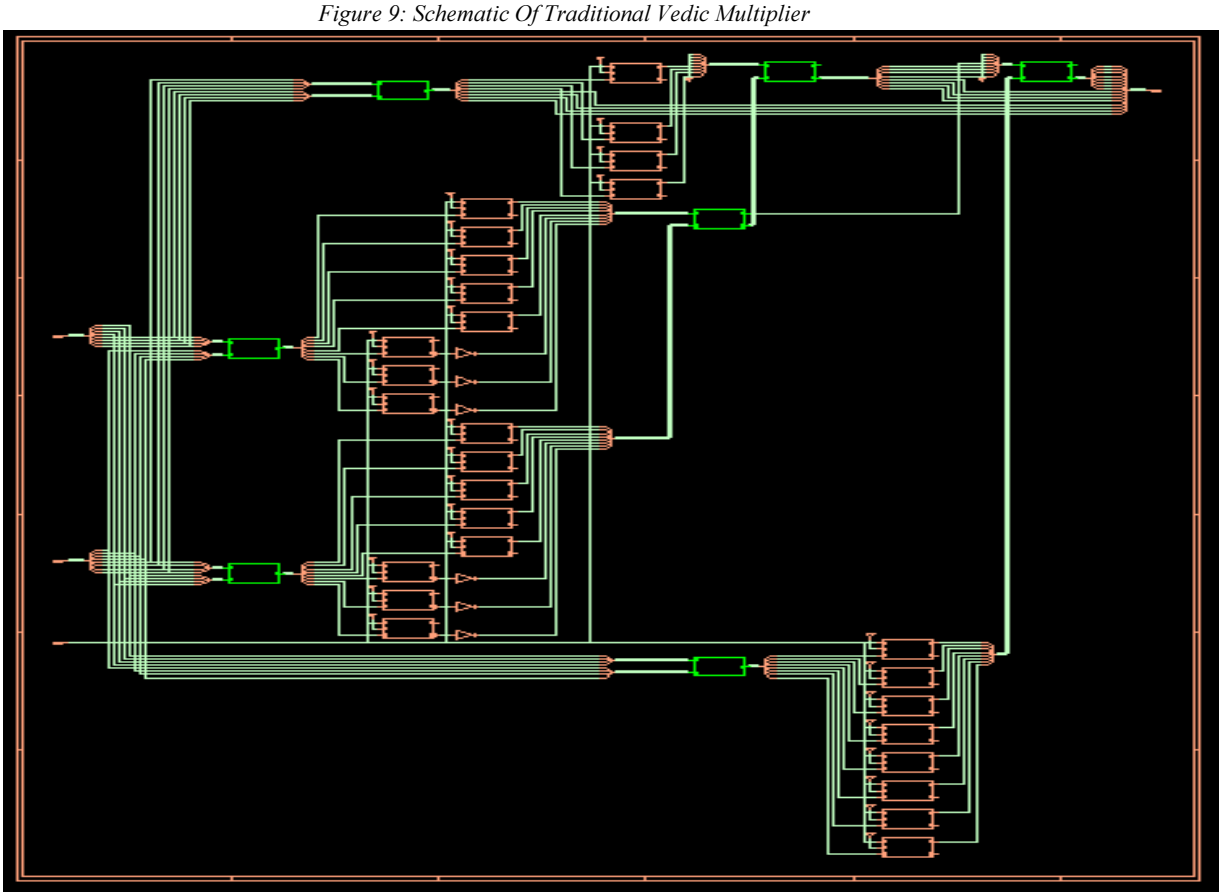

Figure 10: RTL Schematic of Pipelined Vedic Multiplier

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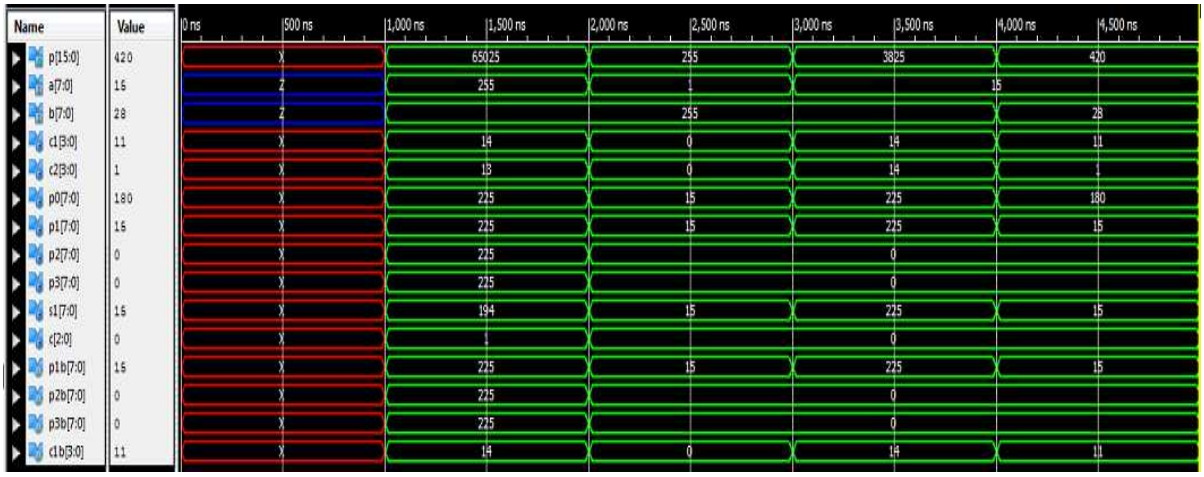

Figure 11: Simulation results of Pipelined Vedic Multiplier

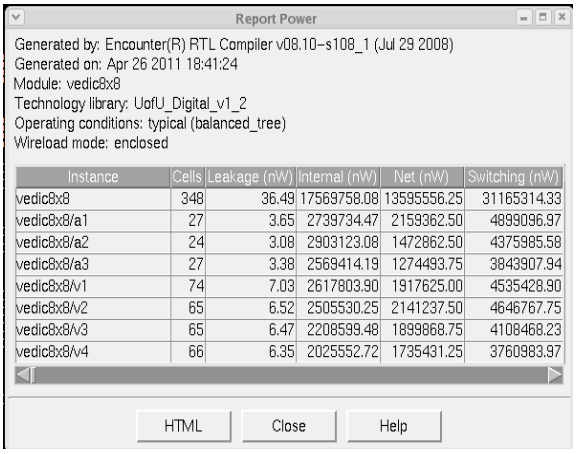

Figure 13: Showing power consumption at cost of individual cell

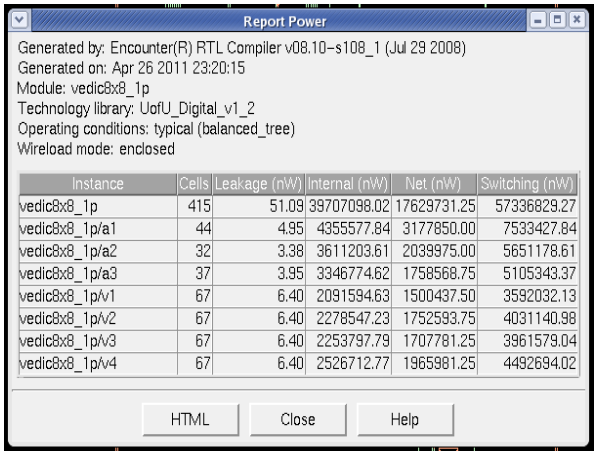

Figure 14: Showing power consumption at cost of individual cell in Pipelined Vedic Multiplier

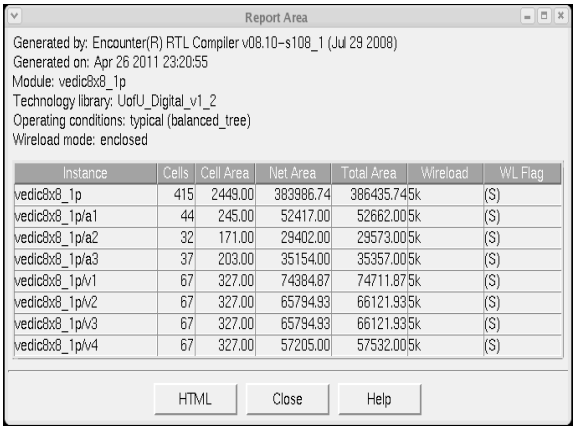

Figure 15: Individual Cell area Report of Pipelined Vedic Multiplier

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