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PROPAGATION DELAY BASED COMPARISON OF PARALLEL ADDERS

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ABSTRACT

An intelligent full adder circuit is simulated using Cadence Virtuoso Analog Design version 6.0. The complementary property between sum and carry for most of the input combination is considered for reducing the number of transistors in the full adder circuit. The parameters such as the Power consumption, Delay and Power Delay Product (PDP) are improved in the proposed CMOS full adder than the conventional CMOS full adder. The size of the chip and the number of transistors are greatly reduced with the proposed circuit. From the single bit full adder module, other parallel adder circuits such as Ripple carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Increment adder, Carry Skip Adder, Carry Select Adder and Carry By-pass Adder are simulated. The worst-case gate delay in each case is measured and compared with other adders.

Keywords: *Full Adder, CMOS, Gate Delay, PDP (Power Delay Product), Parallel Adders.*

1. INTRODUCTION

Adder is the fundamental logic block in the design of more complex logic circuits such as microprocessors, microcontrollers and DSP processors. The adder block is also responsible for other arithmetic operations such as multiplication and division. Hence the time consumed for addition greatly affects the performance and efficiency of the entire logic block by Abu Sharma (1996).

Kevin Navi (2008) designed a low power adder cell which can operate perfectly at very low range of power supply voltage. The author Vishal Sharma (2011) suggested that the proposed CMOS 1-bit full adder design consumes very less power, delay and PDP. Foroutan (2005) proposed a new dynamic full adder cell based on Majority Function. Saberi (2009) proposed a new structure of full adder using pass-transistor logic and branch-based logic. Banupriya and Udhaya kumar (2011) developed GDI and SERF based full adder cells. The merits of the full adder cells were said to be low power depletion, small delay, small power delay product and area. A low power multiplexer based single bit full adder circuit using 12 transistors was presented by Jiang et al (2004).

The truth table of full adder reveals a truth that the sum and carry outputs for six combinations other than 000 and 111 are complement of each other. This property has been used in the full adder circuit considered in this work. In the full adder circuit, the size is considerably reduced and achieved the performance parameters such as delay and Power Consumption.

Comparison of conventional dynamic logic and SRL based adders were carried out in terms of parasitic value, area and power dissipation by Uma (2011). Comparison of different low power fast adders were carried out by Uma (2012).The comparison was based on the number of transistors and maximum delay. It was concluded that the ripple carry adder, carry skip adder and carry bypass adder were suitable for low power applications.

Different types of full adders using transistors and transmission gates are developed and simulated by Saradindu (2012). Average power, average delay and power delay product are obtained for the adders developed and performance comparison was done between different adders by Ramkumar (2010). A low power adder suitable to build low power VLSI systems was constructed by jiang et al (2004). Hspice simulation of 5 different adders was performed and the results were compared. It was

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proved that the multiplexer based adder consumes less power.

Using the intelligent single bit full adder circuit, parallel adders such as Ripple carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Increment adder, Carry Skip Adder, Carry Select Adder and Carry By-pass Adder are simulated and the worst-case gate delay in each case is measured and compared with other adders.

The paper is organized as follows. Section II describes about the Architecture of the intelligent full adder. Section III is about the comparisons of various types of parallel adders. Section IV is about the results and discussion and finally conclusions are given.

2. Comparison of Full Adder

Initially, CMOS implementation of a complementary CMOS full adder circuit is constructed. (Using the property of the truth table of the full adder circuit, a size reduced (intelligent full adder) circuit is constructed.) The performance of both the full adders is compared.

2.1 Complementary CMOS Full Adder

The circuit comprises of conventional pull-up and pull-down transistor networks. Due to the series transistors in the output stage, the output voltage is very less.

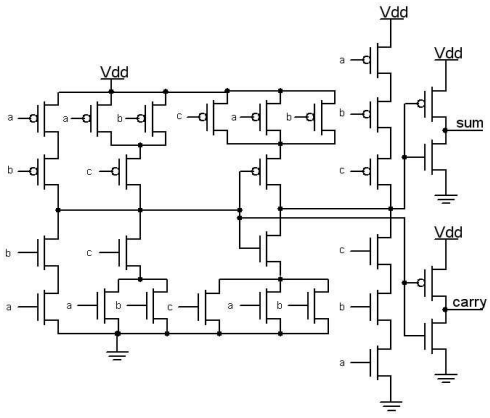

Figure 1: Complementary CMOS Full Adder

Stage. The main advantage of this circuit is that it is robust against voltage scaling and transistor scaling. The complementary CMOS full adder has a single static CMOS gate to generate $C_{out.}$ The complementary CMOS full adder is shown in figure 1.

2.1 Intelligent Full Adder

Figure 2 shows the intelligent full adder. It comprises a complementary majority function CMOS inverter and capacitors. The three input capacitors and inverter implement the complementary C_{out} function. The design is augmented by using high-V_T transistors which have a higher threshold voltage. Therefore the NMOS transistor working as a pull down network is turned ON only when $Vgs_n > Vth_n$ and the output becomes low only when the three inputs are high and vice-versa while all the inputs are low the PMOS is turned ON $Vgs_p < Vth_p$. In all the cases except 000 and 111 both pull-up and pull-down networks are switched OFF and the majority path creates the Sum output. The switched on PMOS pass-transistor is acting as a resistance, corrects the output voltage. The last CMOS inverter enhances the final voltage level and thus the Sum function is implemented.

The implementation of the above method has reduced the number of transistors to 9; hence the chip area is reduced. An additional advantage is

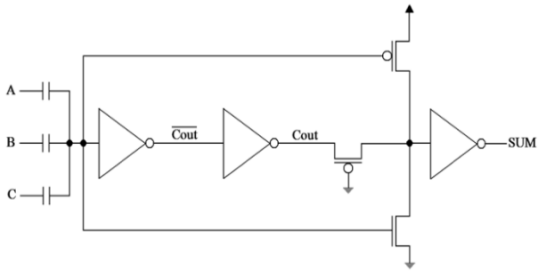

Figure 2: Intelligent full adder

that the intelligent full adder has low transistor count which gives to low switching capacitance and the ability to work at extremely low voltages which is crucial for the next generation ULSI chips. Reducing the number of transistors from V_{dd} to ground to two, the V_T loss problem is overcome and it makes a perfect choice for the low power design and implementation.

3. VARIOUS TYPES OF PARALLEL ADDERS

Different fast adder circuits are considered for comparison based on worst case gate delay.

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3.1 Ripple Carry Adder

The ripple carry adder is constructed by cascading full adder (FA) blocks as shown in the Figure 3. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspecting the full adder circuit. Each full adder requires three levels of logic. In a 32-bit [ripple carry] adder, there are 32 full adders, so the critical path (worst case) delay is 31 * 2(for carry propagation) + 3(for sum) = 65 gate delays.

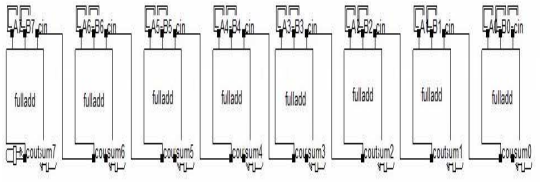

Figure 3: Ripple Carry Adder

3.2 Carry Look Ahead Adder

The carry-look-ahead-adder (CLA) solves the carry delay problem by calculating the carry signals in advance, based on the input signals. Carry look-ahead adder is designed to overcome the latency introduced by the rippling effect of the carry bits. The propagation delay occurred in the parallel adders can be eliminated by carry look ahead adder. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate. The carry Look Ahead adder is shown in figure.4.

3.3 Carry Save Adder

The carry-save adder reduces the addition of 3 numbers to the addition of 2 numbers.

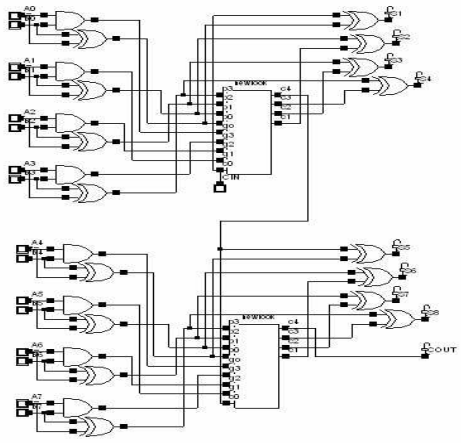

Figure.4: Carry look ahead adder

The propagation delay is 3 gates regardless of the number of bits. The carry save unit consists of n full adders, in which each unit computes a single sum and carries bit based solely on the corresponding bits of the three input numbers. The carry save adder is shown in figure.5.

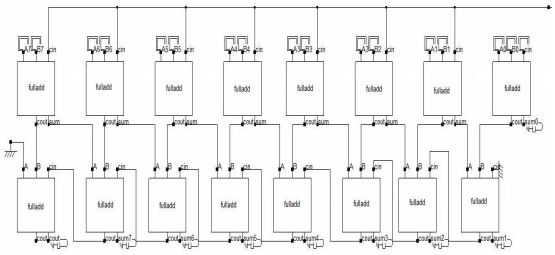

Figure 5: Carry save adder

3.4 Carry Increment Adder

An 8-bit increment adder includes two RCA (Ripple carry adder) of four bits each. The first ripple carry adder adds a desired number of first 4-bit inputs generating a plurality of partitioned sum and partitioned carry. Now the carry out of the first block RCA is given to C_{in} of the conditional increment block. Thus the first four bit sum is directly taken from the ripple carry output. The second RCA block regardless of the first RCA output will carry out the addition operation and will give out results which are fed to the conditional increment block. The input C_{in} to the first RCA block is given always low value. The conditional increment block consists of half adders. Based on the value of C_{out} of the 1st RCA block, the increment operation in second RCA will take place. Here the

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half adder in carry increment block performs the increment operation. Hence the output sum of the second RCA is taken through the carry increment block. The carry increment adder is shown in figure 6.

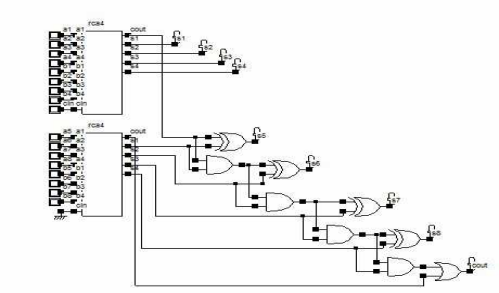

Figure 6: Carry increment adder

3.5 Carry By-Pass Adder

In a ripple-carry adder, every full adder cell has to wait for the incoming carry before an outgoing carry can be generated. This dependency can be eliminated by introducing an additional bypass (skip) to speed up the operation of the adder. An incoming carry C_i, either 0 or 1 propagates through complete adder chain and causes an outgoing carry C_{out}, under the conditions that all propagation signals are 1. This information can be used to speed up the operation of the adder. The carry by pass adder is shown in figure 7.

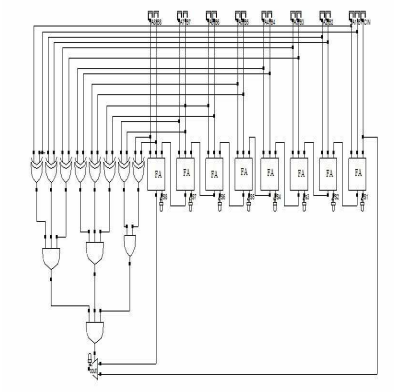

Figure.7: Carry by pass adder

3.6 Carry Skip Adder

A carry-skip adder consists of a simple ripple carry-adder with a special speed up carry chain called a skip chain. Carry skip adder is a fast adder compared to ripple carry adder when addition of large number of bits take place; carry skip adder has $0(\sqrt{n})$ delay provides a good compromise in terms of delay, along with a simple and regular layout This chain defines the distribution of ripple carry blocks, which compose the skip adder. A carry-skip adder is designed to speed up a wide adder by aiding the propagation of a carry bit around a portion of the entire adder. The carry-skip circuitry consists of two logic gates. The AND gate accepts the carry-in bit and compares it to the group propagate signal. The carry skip adder is shown in the figure 8.

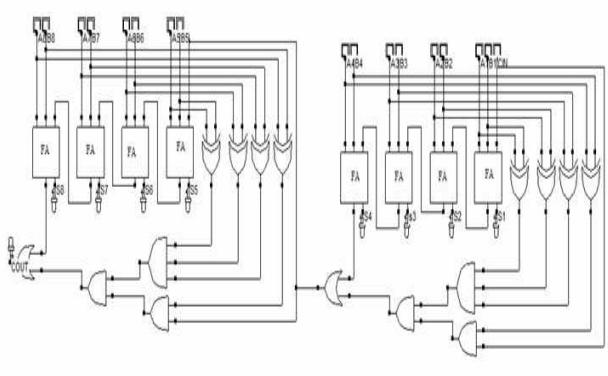

Figure 8: Carry skip adder

3.7 Carry Select Adder

A four bit carry select adder generally consists of two ripple carry adders and a multiplexer. The carry-select adder is simple but rather fast, having a gate level depth of O ($\sqrt{n}$). Adding two n-bit numbers with a carry select adder is done with two adders (two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one.

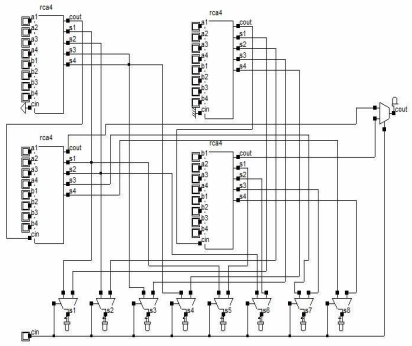

Figure.9: Carry select adder

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4. RESULTS AND DISCUSSION

Two single bit adder cells namely Complementary CMOS Full Adder and the proposed adder have been simulated by using Cadence software. The 0.18nm technology is used to simulate the full adder circuit. The schematic was drawn for each of the circuits. The test-bench waveform was created. This structure simulates the circuits like they do while in actual working conditions. The inputs are fed and the outputs are noted on the scope. The schematic, symbol, test-bench waveform and outputs of two adder designs are shown below. The performance of the full adder circuits in terms of worst–case delay, power consumption and power delay product at 100MHZ frequency is evaluated. The delay is calculated from 50% of voltage level of input to 50% of voltage level of resulting output for both rise and fall output transitions.

It is possible to reduce the delay of all adders without increasing the power consumption by optimizing the size of the full adder circuit.

4.1 Simulation of CCMOS Full adder

The schematic was drawn for CCMOS circuit as shown in figure.1 was drawn in cadence. The Schematic diagram of CCMOS circuit is shown in figure.10. The test bench of the CCMOS circuit is shown in figure.11.The output waveform is shown in figure.12.

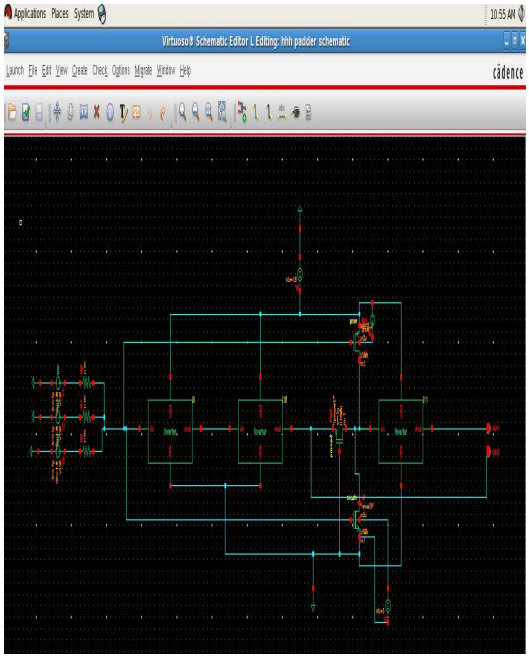

Figure 10: Schematic of Complementary CMOS Full Adder

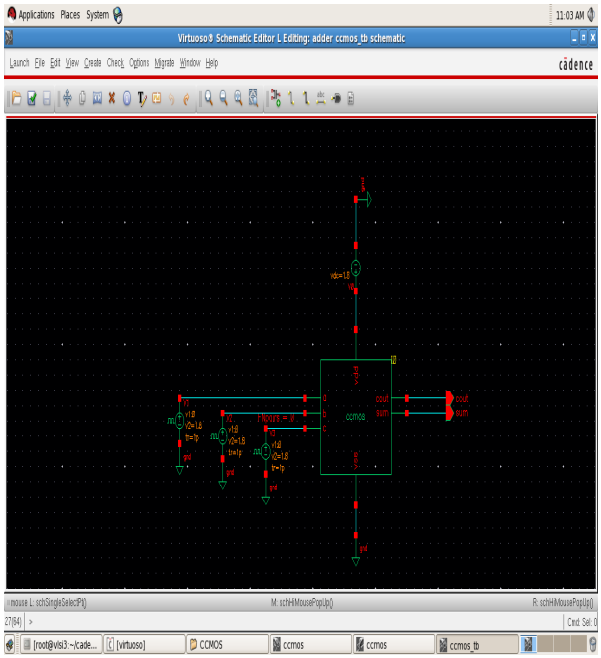

Figure11: Test-Bench of Complementary CMOS Full Adder

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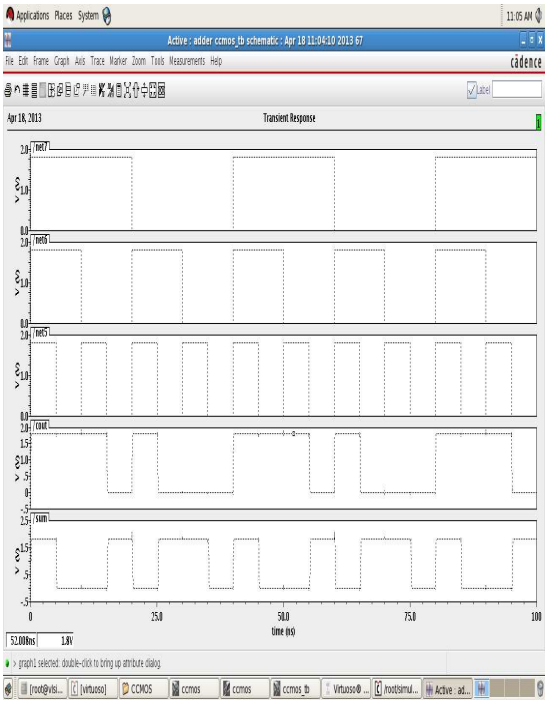

Figure12: Output Waveform of Complementary CMOS Full Adder

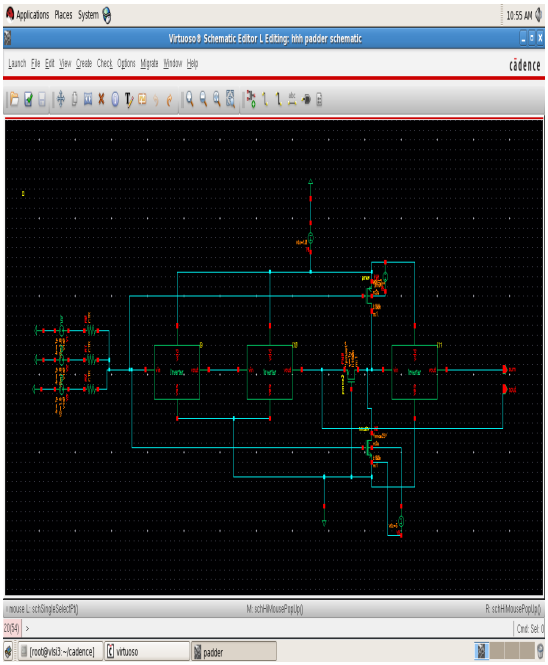

Figure 13: Schematic of intelligent Full Adder

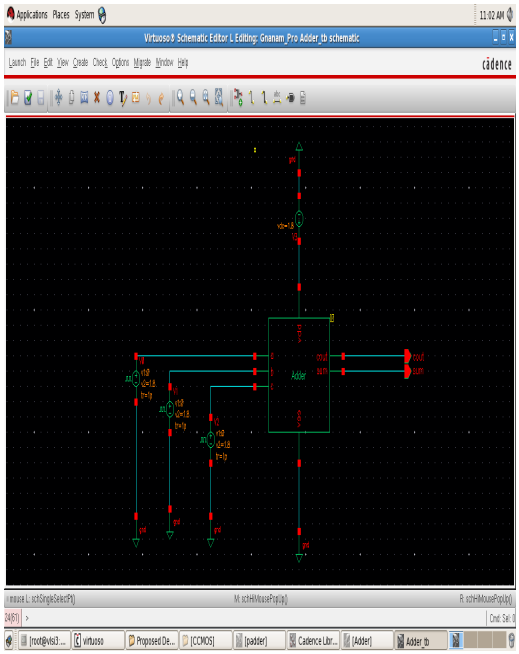

Figure14: Test bench of intelligent full adder

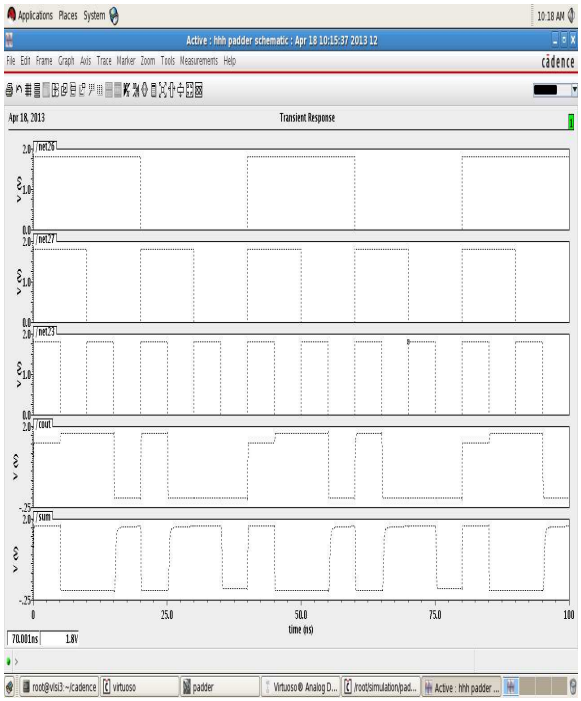

Figure 15: Output Waveform of the intelligent Full Adder

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Power dissipation and worst-case delay and power delay product are calculated for both the full adder circuits. The values obtained are listed in the Table 1.

Table 1 Comparison Of The Performance Of Full Adders

DESIGN	POWER DISSIPATION (µW)	DELAY (ns)	PDP (*10^-15)
CCMOS	0.887	0.673	0.596951
Proposed design	0.406	0.158	0.064148

It is understood from the comparison table that the intelligent full adder design encounters the minimum delay, less power consumption and it also has the lowest PDP.

5. SIMULATION RESULTS OF PARALLEL ADDERS

The intelligent full adder circuit is used to construct the different type of adders. The parallel adders are converted into symbols. The symbol created will look like an IC which is shown as testbench in this chapter. The minimum delay required for obtaining the sum is calculated. The schematic of ripple carry adder is shown in the figure 16.

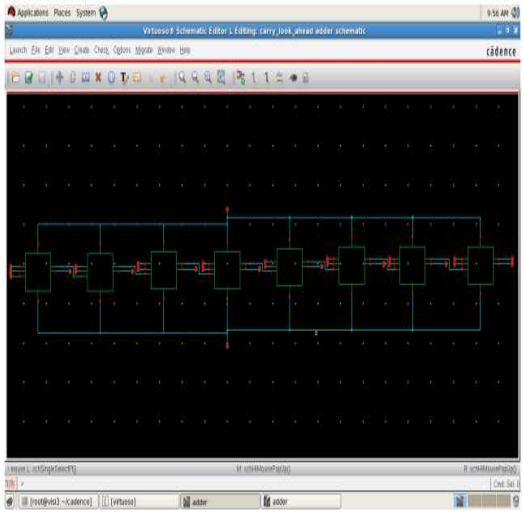

Figure 16: Schematic of Ripple Carry Adder

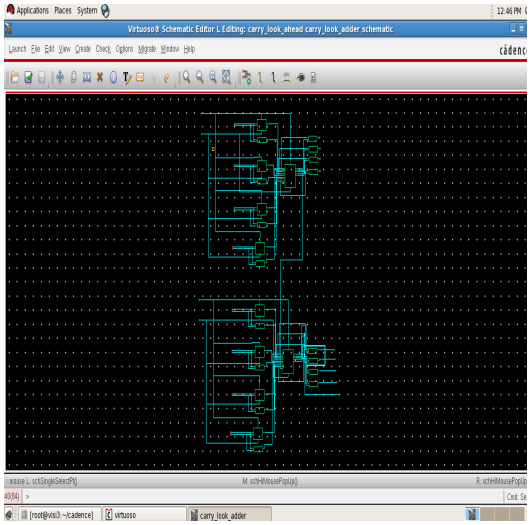

Figure17: Schematic of Carry Look Ahead Adder

The schematic and test bench of Carry look ahead adder are shown in figure.17 and figure 18 respectively.

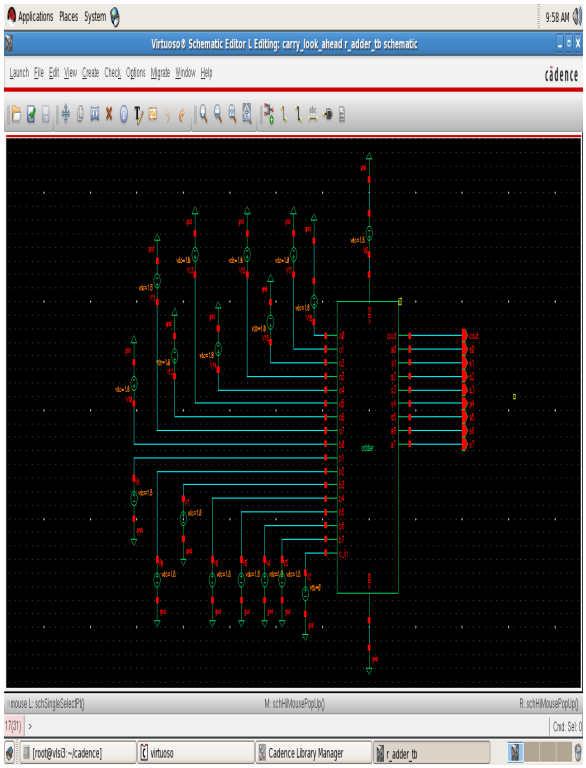

Figure 18: Test bench of Carry Look Ahead Adder

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The Schematic and test bench created for Carry save adder are shown in figures 19 and 20 respectively.

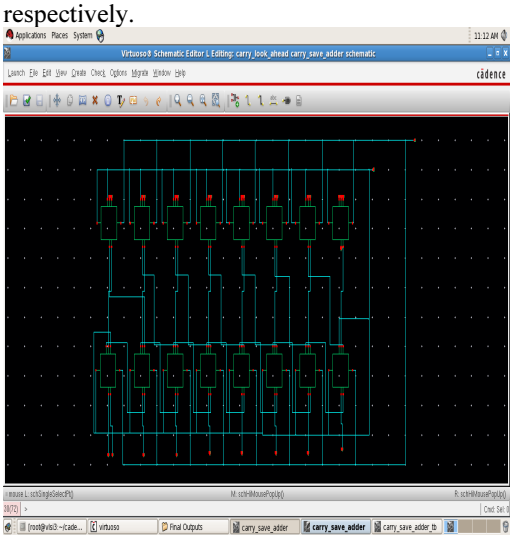

Figure 19: Schematic of Carry save Adder

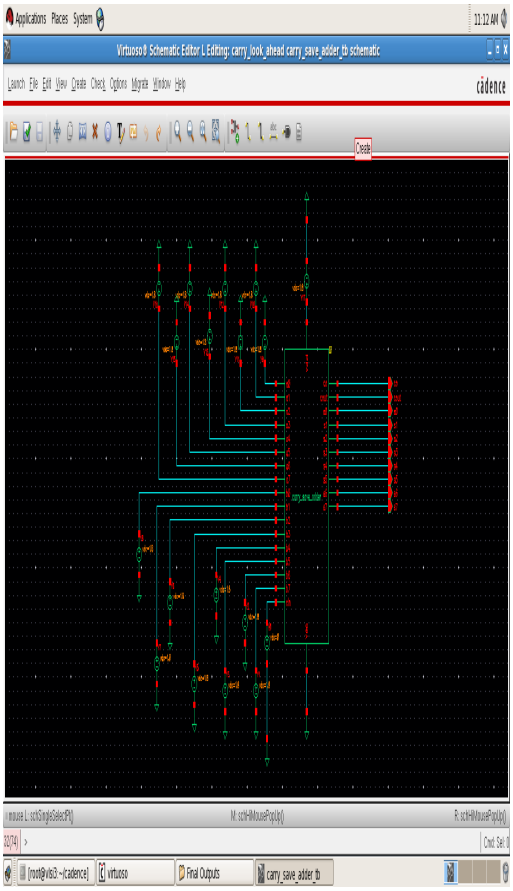

Figure 20: Test bench of Schematic of Carry save Adder

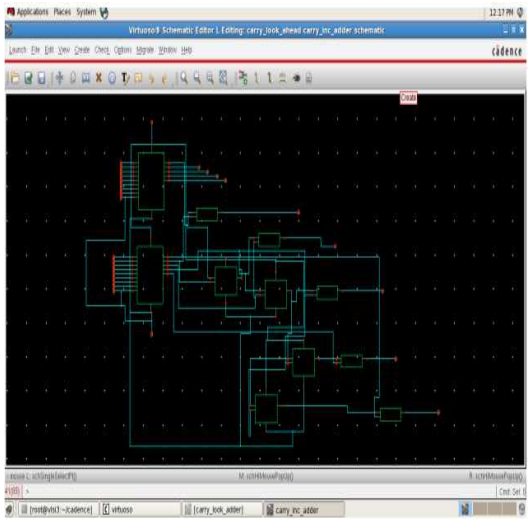

Figure 21: Schematic of Carry Increment Adder

The schematics of Carry Increment Adder carry by-pass adder and carry select Adder are shown in figures 21, 22 and 23 respectively. The testbench of carry select adder is shown in figure.24.

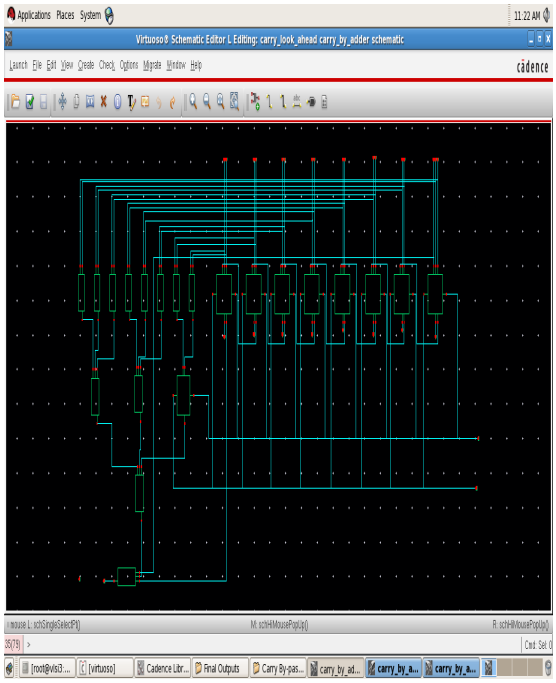

Figure 22: Schematic of Carry By-Pass Adder

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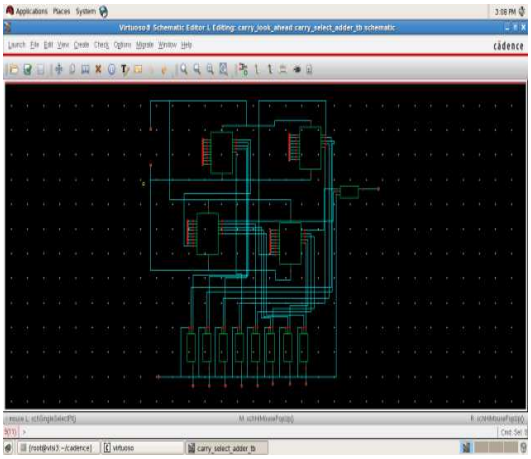

Figure23: Schematic of Carry Select Adder

The schematic of carry skip adder is shown in figure 25.

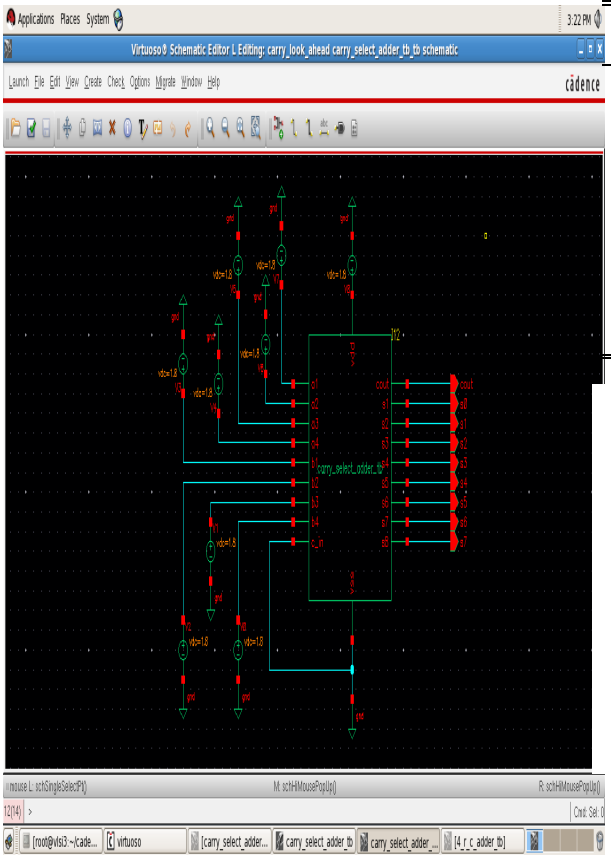

Figure 24: Testbench of Carry Select Adder

The Results of Propagation Delay of various parallel adders are shown in Table 2 and the comparisons are also shown in the figure 27.

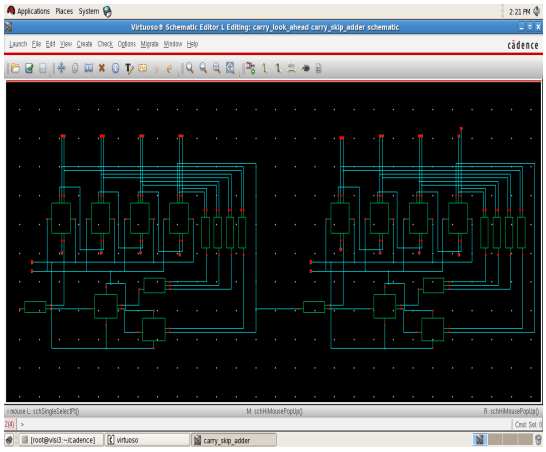

Figure 25: Schematic of Carry Skip Adder

Table 2: Propagation Delay Of Parallel Adder Designs

Adder	Delay(ns)
Ripple Carry Adder	4.208
Carry Save Adder	2.924
Carry Look-Ahead adder	2.742
Carry Increment Adder	3.04
Carry Skip Adder	3.022
Carry By-pass Adder	2.88

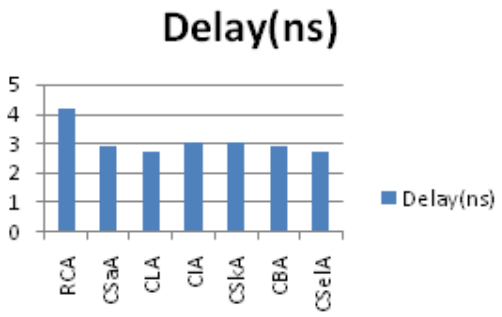

Figure 27: Propagation Delay Of parallel Adders

It is understood from this comparison, the best performance is displayed by Carry look-ahead adder and Carry Select adder.

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5. CONCLUSION

The novel high speed 1-bit Full Adder cell has been presented in this paper. Simulations have shown a significant improvement in terms of delay and reasonable improvement in terms of PDP in comparison with other conventional and currently used cells. The simulation results for the augmented adders are presented. Propagation delay for each of the adder is calculated and compared. Finally, it was justified from the result that the carry look ahead adder and Carry select adder are faster than the other adders.

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