METHOD OF IDENTIFICATION AND DIAGNOSTICS OF PULSED SYSTEMS USING DISCRETE SIGNAL CONVOLUTION

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ABSTRACT

The present paper is devoted to development of the method of pulsed systems identification and diagnostics using discrete signal processing. Authors consider types of synchronous logical convolution and elementary synchronous logical convolutions, namely: synchronous disjunctive convolution, synchronous conjunctive convolution, synchronous conjunctive convolution with delayed variable inversion, synchronous conjunctive convolution with input variable inversion as well as synchronous conjunctive modulo two. Creation of new technical means on the basis of described logical convolution of PZ-signal indicates the possibility of developing new principles of logical and discrete signal processing, and devices.

Keywords: *Logical Signal Convolution Operator, Synchronous Pulsed PZ-Signal, PZ-Series.*

1. INTRODUCTION

The modern equipment of automated technological systems is produced by many manufacturers. If any module breaks down, a line idle can reach several months. A method allowing the synthesis of a scheme with given functional features on programmable logic is introduced in order to reduce economic costs. This method is based on:

1) conversion of time diagrams into synchronous PZ-row;
2) creation of convolution procedures based on pulsed PZ-row.

To eliminate word duality, basic descriptive definitions are introduced.

Synchronous pulsed PZ-signal (P-prima, Z-zero) is a synchronous sequence of units in which the information value is represented in the form of P-row (P-prima) or Z-row (Z-zero). Information parameter is the length (N_P) of P-row and the length (N_z) of Z-row.

Synchronous logical convolution (SLC) is a logical function that determines the logical operation with input PZ-row, both delayed and undelayed. The total number of SLC is determined as $M=2^N$.

Synchronous logical function (SLF) is a logical operation on R and Z-row.

Logical convolution operator (LCO) is a device made of logical and delaying units that implements an elementary SLC.

SLS procedure is a consequent set of actions performed by LCO to achieve the desired result [1].

In logic the obtained results allow the analysis and synthesis of the automats with synchronous delay elements. The general model of such devices can be represented as a synchronous shift register (a single delay unit with traps). The delay element in this case is considered as a demultiplexer performing a shift in the input signals' queue. For convenience of the analysis, the general model is divided into separate functional logical blocks [2], [3].

A lot of scientists study the problems of signal convolution based on synchronous PZ-signal. Among them there are D.A. Pospelov, G.R. Greiner, V.P. Il'yashenko, V.P. May, N.N. Pervushin, L.I. Tokmakov, J. Smith, C. Rothamong and others. A range of their papers focus on the ways of graphical representation of binary variables as functions of time.

Such operators are referred to as 'delay', 'the

first time', 'the second time', 'income', 'state', 'still', etc. They are more or less similar to the function of logical convolution operator of signal the signal operator's logical convolution. The paper introduces a synthesis of the control logical devices using the operators of algebra of states. Delay elements are asynchronous and implemented on the RC-chains [4]. There are examples of constructing control systems on logical elements with delays. There are also descriptions of schemes performing the functions of logical convolution operators. These functions are extension, compression and separation of the front of input PZ-signal, and a description of them is provided in the form of Boolean function of the second kind recursion [5].

The papers listed above were relevant in the 1970s and 1980s; however the implementation of the described principles of creating logical delay systems thereafter experienced a lack of development in its element base, and therefore did not receive an essential level of distribution.

Programmable logical circuits of CPLD-type allow implementing management systems and information processing systems based on configured modules with dynamic management. These modules act as the elements of digital technology for the logical convolution operators [6].

This approach allows the creation of a system-on-chip solution. It provides an opportunity to switch restricted management systems and information processing systems to the state of modern electronics, ignoring embeddings in imported electronic devices. Minimisation of the number of elements required for building systems is supposed to lower the energy consumption and will raise their reliability.

Using the formalised method of synthesis for synchronous logical circuits will simplify systems and will lower their development by transferring the timing charts into PZ-row, a compilation of PZ-row convolution procedures and circuit synthesis of convolution procedures.

Unconditional logic of the device will increase the stability of the performance in case of proper debugging; the probability of software failures will thereby decrease. When compared to FPGA, systems based on microcontrollers tend to 'hang up'. It negatively affects the operation of any system.

2. TYPES OF SYNCHRONOUS LOGICAL CONVOLUTION

There is a great variety in the functions of the logical convolution. However the main classes of functionally complete sets of elementary logical functions are:

$$
\begin{aligned}
C_\delta(p) &= A(p) \vee B(p), \\
C_\kappa(p) &= A(p) \wedge B(p), \\
C_\varphi(p) &= A(p) \wedge \overline{B(p)}, \\
C_S(p) &= \overline{A(p)} \wedge B(p), \\
C_\mu(p) &= A(p) \oplus B(p),
\end{aligned}
\tag{1}
$$

where C_δ is disjunctive, C_k is conjunctive of the structure, C_φ is conjunctive with delayed variable inversion, C_s is conjunctive with input variable inversion, C_μ is modulo two addition of input and delayed variables, $B(p)$ is delay polynomial, and $A(p)$ is input consequence.

To implement logical signal processing operations with synchronous logic should be reduced to the convolution operations with polynomials and similar terms under the rules of logical addition, multiplication and modulo two addition.

The result of the logical convolution on the input signal is the output row, determined by the form of the input signal and the form of convolution.

Using a functionally complete set of convolution operators, any convolution procedure can be implemented.

3. ELEMENTARY SYNCHRONOUS LOGICAL CONVOLUTIONS

In accordance with the definition of SLF, any SLS can be represented as a set of elementary single level schemes. The following schemes are the most common ones.

3.1. Synchronous Disjunctive Convolution

1. A logical action described by the following logical function is to be called a synchronous disjunctive convolution (SDC):

$$
C_\delta(p) = A(p) \vee B(p).
\tag{2}
$$

2. A device that performs such convolution is to be called δ operator, the P-row elongation.

3. A repeating exposure of δ operators to the input row $A(p)$ is to be called the procedure $C_\delta \leftarrow \{A \circ i\delta\}$, where C_δ is output row, i is the number

of consequently connected δ operators.

4. The result of the procedure {A∘iδ} is P-row elongation by i elements.

SDC scheme is a consistent (cascade) scheme, where each cell (cascade) delays the signal for one position in the row.

$$C(p) = A(p) + B(p) = p^0 + p^1 + p^2 + p^3 + p^4. \quad (3)$$

Reduction of similar terms shall be implemented according to the rules of logical addition.

$$1 + 0 = 1; \quad 1 + 1 = 1$$
$$p + 0 = p. \quad p + p = p. \quad (4)$$

Disjunction $C(p) = A(p)^\vee B(p)$, $B(p) = A(p) \cdot p^1$ with one delay unit (fig. 1a) is described by equation from the table 1. P-row of input row is elongated by one element.

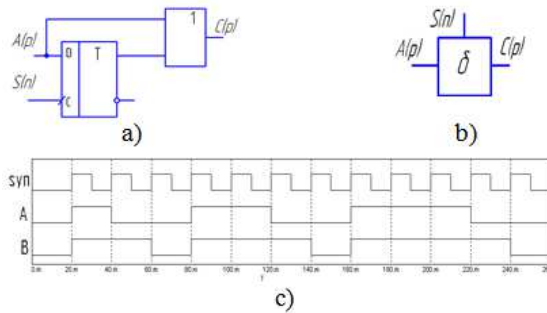*Table 1: SDC Logical Function*

Figure 1: Scheme of a Synchronous Disjunctive Convolution (a), Pictorial Symbol (b) and Time Diagrams of the SDC Operator (c)

In this particular case P-row can be regarded as a sequence of pulses, and then:

- pulses of the input sequence shear lengthen by $t_C = i\tau$, where i is the number of consequent operators δ;

- length of pauses between pulses is $t_A \leq k\tau$, where k is the number of delay units that are discriminated – filled with elementary intervals. Consequently, their frequency falls.

- if $t_A \leq t_3 = k\tau$, then the length of output pulse t_C remains unchanged, but pulse p^k is added to the k position between pulses.

Based on the description above, the total delay in synchronous systems may be replaced by one element with the synchronization period $T_c = k\tau$. In this scheme the delay length can be adjusted by synchronisation frequency.

Thus, SDC is a device that generates a reference signal of duration $t = \tau (1 + i)$ from the strobe, where i is the length of convolution.

3.2. Synchronous Conjunctive Convolution

1. A logical action described by the following logical function will be called as a synchronous conjunctive convolution (SCC):

$$C_\kappa(p) = A(p) \wedge B(p). \quad (5)$$

2. A device that performs such convolution will be called κ operator, the P-row compression (length decrease of the P-row by one unit).

3. A repeated exposure of κ operators to the input row A(p) will be called the procedure Cκ←{A∘jκ}, where Cκ is output row, j is the number of consequently connected κ operators.

The result of the procedure {A∘ jκ} is P-row length decrease by Nx-j. If the length of Z-row does not exceed 1, Z-row will be discriminated.

4. General view of the scheme that performs conjunctive convolution is shown in fig. 2a.

SCC is a consistent (cascade) scheme, where each cell (cascade) delays the signal for one position in the row. Reduction of similar terms in conjunctive convolution shall be implemented according to the rules of logical multiplication:

$$1 \circ 0 = 0; \qquad 1 \circ 1 = 1;$$
$$p \circ 0 = 0; \qquad p \circ p = p$$
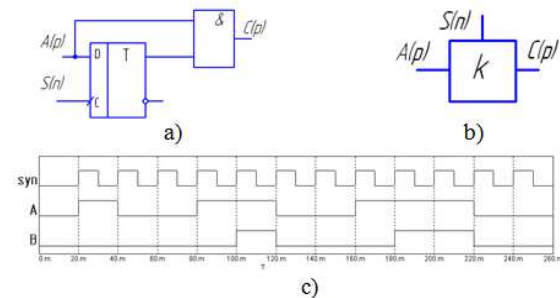$$p_i \circ p_j = 0 \text{ if } i \neq j. \quad (6)$$

Figure 2: Scheme of a Synchronous Conjunctive Convolution (a), Pictorial Symbol (b) and Time Diagrams of the SCC Operator (c)

Conjunctive convolution can be used for PZ-signal combinations identification, allocation of zero or a single strobe; step identification, error fragments identification, and synchronised values selection.

Let us consider some special cases of conjunctive convolution described by the equations presented in table 2.

In the particular case P-row can be regarded as a sequence of pulses, then:

- pulses of the input sequence are front-shortened by $t_3 = \kappa\tau$, where κ is the number of delay units;

- pulses of $t_u \leq \kappa\tau$ length are not omitted (they are discriminated, table 2.1);

- if length of pause is $t_3 > \kappa\tau$, the output pulse will be front-delayed $t_3 = \kappa\tau, t = t_u - \kappa\tau$.

Conclusion: conjunctive convolution has selective properties and can be used for comparing the length of the P-row with a constant.

Table 2: Logical Functions of SCC

	A(p)				C(p)				Logical function interpretation
1									$C(p) = p^0 \wedge p^1 = 0$
2									$C(p) = (p^0 + p^1) \wedge p^1 = p^1$
3									$C(p) = (p^0 + p^1 + p^2) \wedge (p^1 + p^2 + p^3) = p^1 + p^2$
4									$C(p) = (p^0 + p^2) \wedge (p^1 + p^3) = 0$
5									$C(p) = (p^0 + p^3) \wedge (p^1 + p^2) = 0$
	0	1	2	3	4	0	1	2	3	4	Discrete scale

Conjunctive convolution performs filtering functions (pulse discrimination), as in table 2.1, as well as front-delaying pulses as in table 2.2-3, length limitation and length rejection, as in table 2.4-5.

3.3. Synchronous Conjunctive Convolution with Delayed Variable Inversion

1. A logical action described by the following logical function will be called a synchronous conjunctive convolution with delayed variable inversion (SFC – synchronous front convolution):

$$C_\varphi(p) = A(p) \wedge \overline{B(p)} \cdot \qquad (7)$$

2. A device that performs such convolution will be called front allocation operator φ.

3. A repeated exposure of φ operators to the input row A(P) will be called the procedure Cs ←{A∘nφ}, where C is output row, *n* is the number of consequently connected φ operators.

4. The result of the procedure {A∘nφ} is newly formed single P-strobe after the end of input P-row.

Timing diagrams can illustrate the essence of the transformation as well as the corresponding logical functions listed in table 3. Operator φ (fig. 3) has the features, which can be used in different converting devices.

Operator φ is a ZP(01) step identifier and may be used to form:

1) strobes at the pulse front;
2) duration integrity of signal intervals indicator.

Table 3: SFC Logical Functions

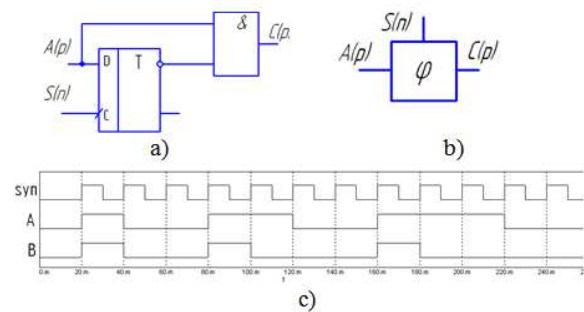|	A(p)				C(p)				Logical function interpretation
1									$C(p) = p^0 \wedge \overline{p^1} = p^0$
2									$C(p) = (p^0 + p^1) \wedge \overline{p^1 + p^2} = p^0$
3									$C(p) = (p^0 + p^1 + p^2) \wedge \overline{p^1 + p^2 + p^3} = p^0$
4									$C(p) = (p^0 + p^2) \wedge \overline{p^1} = p^0 + p^2$
5									$C(p) = (p^0 + p^3) \wedge \overline{p^1} = p^0 + p^3$
	0	1	2	3	4	0	1	2	3	4	Discrete scale

Figure 3: Scheme of a Front Allocation Operator (a), Pictorial Symbol (b) and Time Diagrams of the SFC Operator (c)

3.4. Synchronous Conjunctive Convolution with Input Variable Inversion

1. A logical action described by the following logical function will be called a synchronous conjunctive convolution with input variable inversion (SCC – synchronous convolution cut-off)

$$C_S(p) = \overline{A(p)} \wedge B(p) \cdot \qquad (8)$$

2. A device that performs such convolution will

be called an s shear operator.

3. A repeated exposure of s operators to the input row A(P) will be called the procedure $C_s \leftarrow \{A \circ ls\}$, where C is output row, l is the number of consequently connected s operators.

4. The result of the procedure $\{A \circ ls\}$ is a newly formed single P-strobe after the end of input P-row.

The essence of the transformation can be illustrated by timing diagrams and the corresponding logical functions listed in table 4. 'Shear' operation is a PZ-signal step identifier. It forms P-strobe that coincides with the first element of Z-row.

In the particular case the following elements can be used for formation:

1) strobes at the pulse shear;
2) indicators of Z-row continuity.

Table 4: SSC (Shear Operator) Logical Functions

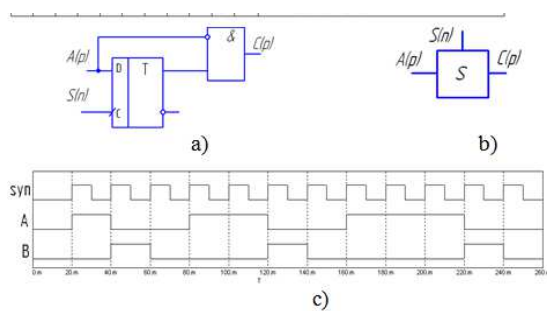|	A(p)	C(p)	Logical function interpretation
1			$C(p) = p^0 \wedge p^1 = p^1$
2			$C(p) = (\overline{p^0 + p^1}) \wedge (p^1 + p^2) = p^2$
3			$C(p) = (\overline{p^0 + p^1 + p^2}) \wedge (p^1 + p^2 + p^3) = p^3$
4			$C(p) = (\overline{p^0 + p^2}) \wedge (p^1 + p^3) = p^1 + p^3$
5			$C(p) = (\overline{p^0 + p^3}) \wedge (p^1 + p^3) = p^1 + p^4$
	0 1 2 3 4	0 1 2 3 4	Discrete scale

Figure 4: Scheme of a Shear Operator (a), Pictorial Symbol (b) and Time Diagrams of the SSC Operator (c)

3.5. Synchronous Conjunctive Modulo Two

1. A logical action described by the following logical function will be called a synchronous convolution modulo two (SMC)

$$C_\mu(p) = A(p) \oplus B(p) \cdot \qquad (9)$$

2. A device that performs such convolution will be called µ operator that performs marking function (begin and end marking) of the P-row.

3. A repeated exposure of µ operators to the input row A(P) will be called the procedure Cµ $\leftarrow \{A \circ g\mu\}$, where C is output row, n is the number of consequently connected **µ** operators.

4. The result of the procedure is newly formed front strobe and P-row shear.

The reduction of similar terms will be implemented according to the rules of modulo two addition:

$$1 \oplus 0 = 1; \quad 1 \oplus 1 = 0;$$
$$p \oplus 0 = p \cdot \quad p \oplus p = 0 \cdot \qquad (10)$$

Such schemes are the basis of the cyclic coding devices. Modulo two convolution is the main operation of analog-to-digital conversion of PZ-signal into code.

Convolution modulo two has the properties, based on which a large number of different reducers can be performed. In a particular case the convolution can be used for construction of pulse converters. Consider the following functions:

- indicator of PZ-signal changes (leaps) produces a pulse, coinciding with the first intervals of steps ZP (01), PZ (10) (the front pulse and the shear of pulse);

- if input pulse length is $t_i = k\tau$, then output length is $t_i = 2k\tau$;

- if $t_i = t_n = \tau$, then z-row will be discriminated and therefore convolution modulo two can be considered a frequency detector;

- if $t_i = t_n = 2\tau$, then output frequency is doubled.

Feedback and the corresponding logical functions are shown in table 5. The following rules can be formulated based on the information contained therein.

Table 5: SMC (Modulo two Convolution) Logical Functions

	A(p)	C(p)	Logical function interpretation
1			$C(p) = p^0 \oplus p^1 = p^0 + p^1$
2			$C(p) = (p^0 + p^1) \oplus (p^1 + p^2) = p^0 + p^2$
3			$C(p) = (p^0 + p^1 + p^2) \oplus (p^1 + p^2 + p^3) = p^0 + p^3$
4			$C(p) = (p^0 + p^2) \oplus (p^1 + p^3) = p^0 + p^1 + p^2 + p^3$
5			$C(p) = (p^0 + p^3) \oplus (p^1 + p^4) = p^0 + p^1 + p^3 + p^4$
	0 1 2 3 4	0 1 2 3 4	Discrete scale

Modulo two convolution:

1)   lengthens single pulses (table 5.1);
2)   filters (aggregates pauses) table 5.2);
3)   doubles row frequency (table 5.3);
4)   aggregates single pauses (table 5.4);
5)   prolongs row without changing frequency (table 5.5).

The following devices of system identification based on the logical convolution operators can be developed:

1)   length-sensitive detectors;
2)   phase-shift discriminator;
3)   phase advance or delay converters;
4)   PZ-series converters; frequency and latitudinal descriptors;
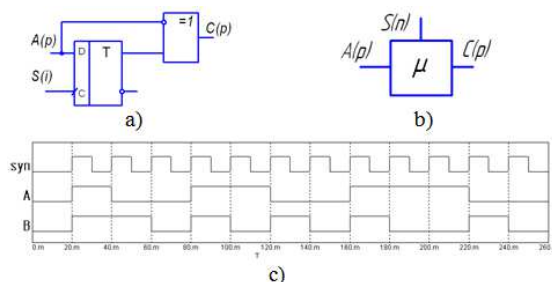5)   latitude-shift and phase-shift modulators and demodulators.

Figure 5: Scheme of SMC (a), Pictorial Symbol (b) and Time Diagrams of the SMC Operator (c)

FPGA-based systems underlined the advantages of the logical convolution operators compared to the implementation of systems based on microcontrollers, Verilog HDL and VHDL programming languages.

The comparative analysis was performed on latitude-shift and phase-shift modulators and assembly logical identifiers. We can see the implementation of these devices in table 6.

Table 6: Implementation of the Systems Based on Microcontrollers and FPGA

Programming language	Hardware implementation
Logical convolution operators	Altera FPGA
Assembler	Atmel Microcontroller
Verilog HDL	Altera FPGA

Circuit implementation of the software file through the logical convolution operators simplifies visual perception and takes fewer FPGA logical elements than a similar implementation in Verilog HDL.

When compared with the microcontroller implementation, the logical convolution operators allow parallelising and pipelining data-handling procedure and the methods of management systems construction.

Development of a universal convolution module, capable of implementing the whole range of convolution procedures, will allow for flexible solutions with minimal FPGA logical elements expenditure.

Unlike the microcontroller, FPGA has many more custom outputs with the opportunity of 'flashing on the go'.

At high frequencies FPGA have gain in performance speed compared to microcontrollers. That is due to the limited value of the clock frequency of the latter.

4.   CONCLUSION

The proposed FPGA set allows upgrading the method of logical scheme synthesis in the sphere of pulse devices development, identification and diagnostics. The upgraded method allows creating control and identifying devices based on programmable logic. Schemes synthesis using timing diagrams will reduce man-hours and in some cases surpass the modern means of classical digital signal processing.

In accordance with the proposed classification of reducers based on the principle of synchronous unitarity, transformative procedures are introduced to perform PZ-synchronous signal transformations.

Logical models of synchronous delay units were created, allowing the application of logical analysis, synthesis of synchronous devices and the development of a formal methodology for the analysis and synthesis of pulsed devices with delay units.

To describe the converting procedures, logical convolution operations were introduced and the full set of logical operators of convolution was determined.

SLF systematisation was carried out. Of all the diverse functions of the SLF, the major class of elementary logical functions was marked out. It determines the complete set of logical operations on delayed and undelayed variables.

Using five LCO greatly simplifies recording and

perception of conversion procedures and, most importantly, allows vector and matrix representation of the conversion procedures.

$$\{\overline{x \circ \varphi}\} = \{x \circ s\}; \quad x \wedge \overline{\{x \circ \varphi\}} = \{x \circ \kappa\}; \quad x \vee \overline{\{x \circ \varphi\}} = \{x \circ \delta\}; \quad \overline{\{x \circ \varphi\}} \vee \{x \circ \varphi\} = \{x \circ \mu\}$$

$$x \wedge \{x \circ \mu\} = \{x \circ \varphi\}; \quad \overline{x} \wedge \{x \circ \mu\} = \{x \circ s\}; \quad \overline{x} \vee \{x \circ \mu\} = \{x \circ \delta\}; \quad \overline{x} \wedge \overline{\{x \circ \mu\}} = \{x \circ \kappa\}$$

$$x \wedge \overline{\{x \circ \kappa\}} = \{x \circ \varphi\}; \quad \overline{\{x \circ \kappa\}} = \{x \circ \delta\}; \quad \overline{x} \wedge \overline{\{x \circ \kappa\}} = \{x \circ s\}; \quad \overline{\{x \circ \kappa\}} \wedge \overline{\{x \circ \kappa\}} = \{x \circ \mu\}$$

$$\{x \circ \delta\} \wedge x = \{x \circ \varphi\}; \quad \{x \circ \delta\} \wedge \overline{x} = \{x \circ s\}; \quad (x \wedge \{x \circ \delta\}) \vee (\{x \circ \delta\}) \wedge \overline{x} = \{x \circ \mu\}; \quad x \wedge \overline{\{x \circ \delta\}} = \{x \circ \kappa\}$$

$$\overline{\{x \circ s\}} = \{x \circ \varphi\}; \quad \{x \circ s\} \wedge x = \{x \circ \delta\}; \quad x \wedge \overline{\{x \circ \kappa\}} = \{x \circ k\}; \quad \overline{\{x \circ s\}} \vee \{x \circ s\} = \{x \circ \mu\}$$

Basic conversion features of convolution blocks were analysed: front shortening, shear elongation, doubling, merging of adjacent rows, combination identification, and row length selection.

Based on the results of the study the following conclusions were made and proved:

- a synchronised pulse signal can be represented by a set of P-rows;

- any consequent convolution scheme can be reduced to the equivalent of a convolution scheme consisting of a delay and a logical unit by transformation of the delay units to the input;

- to perform logical operations on PZ-signals the transformed sequence of pulses must be demultiplexed (dimensionally open) by delay units, and then perform the inverse problem – multiplex (close) using logical output devices.

Thus, it can be stated that the creation of new technical means on the basis of logical convolution of PZ-signal indicates the possibility of developing new principles of logical and discrete signal processing, and devices such as digital filters on programmable logic, discrete-time nonlinear systems. [7], [8].

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Any convolution row can be represented by a set of convolution operators: