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SYNCHRONOUS SEQUENTIAL CIRCUIT BASED CASCADED MULTILEVEL INVERTER

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ABSTRACT

This paper is focused on the practical and designing aspects of a cascaded multilevel inverter using synchronous sequential circuits. The performance of the inverter has been improved by using a digital logic algorithm for required pulse width modulation. The digital logic algorithm has been exposed to give the superior performance in load voltage and total harmonic distortion. The synchronous sequential circuit based multilevel inverter offer several advantages like simple structure, easy to identify the fault, cost-effective, improved functional performance and low power consumption. The output voltage performance of proposed strategy has been confirmed through simulation and hardware investigations.

Keywords: *Digital Logic Control (DLC), Synchronous Sequential Circuits (SSC), Total Harmonic Distortion (THD), Cascaded Multilevel Inverter (CMLI), Pulse width modulation (PWM).*

1. INTRODUCTION

The multilevel inverters were introduced since 1975. They are popular due to their high-power, high voltage capacity, low switching losses and low cost. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as solar, wind, fuel cells and MHD can be easily interfaced to a multilevel converter system for a high power application [1–4]. The concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple DC voltage sources.

The multilevel inverter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses and produce smaller Common-mode voltage [5]. Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Unfortunately, multilevel converters do have some drawbacks. One particular drawback is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. The various topologies of multilevel inverters are cascaded, diode clamped and flying capacitors multilevel inverters [6-9]. The modulation techniques developed for multilevel converters are sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), etc.

The proposed system is focused on the synchronous sequential circuit control of the seven-level cascaded multilevel inverter for standalone system. The clocked sequential circuit is a digital system which contains digital logic devices. This digital logic device produces the PWM pulses to control the seven-level inverter. The proposed system is investigated through simulation and portable hardware model.

2. CASCADED MULTILEVEL INVERTER

The general function of this multilevel inverter is the same as that of two level inverters. The cascaded multilevel inverter synthesizes a desired

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AC voltage from several independent sources of DC voltage, which may be obtained from batteries, MHD, fuel cells, or solar cells, etc. The cascaded multilevel inverter configuration recently becomes very popular in AC power supply and adjustable speed drive applications. This inverter can avoid extra clamping diodes and voltage balancing capacitors. A seven-level cascaded multilevel inverter configuration is shown in figure1. Each DC source is associated with a single-phase full-bridge inverter. The DC terminal voltage of single-phase full-bridge inverters are connected in series with different combination of switching function (S1-S4), each single-phase full-bridge inverter can generate three different voltage outputs such as +Vdc, -Vdc, and zero.

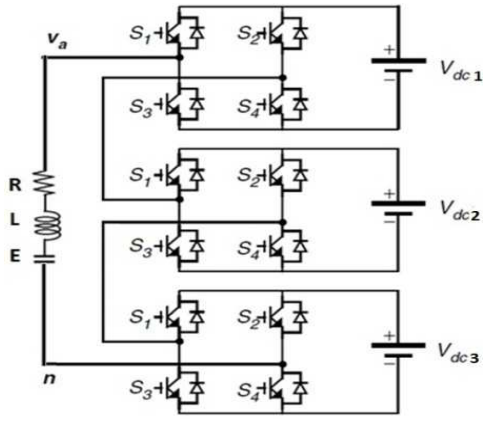

Figure 1: Cascaded Multilevel Inverter

In this topology, the phase voltage levels are defined by m = 2s+1, where 'm' is the number of levels and's' is the number of DC sources. The proposed method has been designed for a seven-level cascaded multilevel inverter, which has three single-phase full bridge Inverter connected in series; it produces the desired seven-level phase voltage.

For seven-level cascaded multilevel inverter (including 0) per half phase output phase voltage is

$$V_o = V_{dc1} + V_{dc2} + V_{dc3} \quad (1)$$

The Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_n [\cos(n\theta_1) + \cos(n\theta_1) + \ldots + \cos(n\theta s)]X\frac{\sin(n\omega t)}{n} \quad (2)$$

Where n =1,3,5,7,…..

The magnitudes of the Fourier coefficients when normalized with respect to Vdc are as follows

$$H(n) = \frac{4}{n\pi}\sum_n [\cos(n\theta_1) + \cos(n\theta_1) + \ldots + \cos(n\theta s)]$$

Where n =1,3,5,7,….. (3)

3. DIGITAL MODULATION SCHEME

Almost all power electronic converters are operated in the switched mode. This means the switches within the multilevel inverter are always in either one of the states turned OFF or turned ON. To control the flow of power in the multilevel inverter, the switches alternate between these two states. The switched component is attenuated and the desired DC or low frequency AC component is retained. This process is called Pulse Width Modulation (PWM). The required switching pulses are developed by using a clocked sequential circuit. The seven level cascaded multilevel inverter voltage levels works as desired by manipulating the switching pulses (PWM) produced by the clocked sequential circuit.

The clocked sequential circuits based multilevel inverters offers several advantages like simplicity of control at circuitry-level, ease of building the multilevel voltage source inverter, etc. The following are steps involved in the designing procedure of clocked sequential circuits [10]

- Assumption of the number of levels (n) of the multilevel inverter.
- The 'n' level phase voltages are converted to binary number and binary to decimal numbers.
- Draw the state diagram from binary number.
- Obtain state table from the state diagram information.
- Assign binary values to each state in the state table.
- Determine the number of flip flop needed and assign a letter
- Choose the type of flip flop to be used.
- Using the K-map derives the circuit output and flip flop functions.
- Draw the logic diagram.

The paper focuses on seven-level cascaded multilevel, the seven-level phase voltages are converted into the equivalent binary number as shown in figure.2. The positive or negative waveforms are considered for designing, because sinusoidal waveform is a symmetrical waveform. The equivalent decimal numbers of phase voltages are 0, 12, 14, 15, 6 and 4. P1, P2 and P3 are the switching pulses for the inverter and AP is the auxiliary switching pulse.

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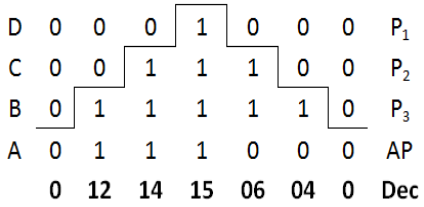

Figure. 2: Equivalent Binary Number of Phase Voltage

The equivalent binary numbers of the seven-levels of voltages are converted into their equivalent decimal numbers. The State diagram of the equivalent decimal numbers is drawn as shown in figure 2. State diagrams provide another useful tool that is normally used when the state of the entities in the system will change in response to events. The next state of the state variables is assigned as the order of equivalent binary number of phase voltage as per figure 2.The state diagram acts as a ring counter.

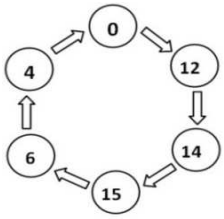

Figure 3: State Diagram

The state table is obtained from the state diagram and the binary values are assigned to each of the states in the state table. The state table of clocked sequential circuit is shown in table 1. Present state and next state of state table 1 are derived from the state diagram as shown in figure 3. The JK flip flop is taken for designing the clocked sequential circuits. The JK flip flop of state table 1 is derived from the present state and the next state using the excitation table of JK flip flop. The table 2 shows the excitation table of JK flips flop.

Table 1: State Table

	Present state				Next state				Flip Flop							
Dec	Q_A	Q_B	Q_C	Q_D	Q_A	Q_B	Q_C	Q_D	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	1	1	0	0	1	X	1	X	0	X	0	X
1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
2	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
3	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
4	0	1	0	0	0	0	0	0	X	X	X	1	0	X	0	X
5	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
6	0	1	1	0	0	1	0	0	X	X	X	0	X	1	0	X
7	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X
8	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
9	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
10	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
12	1	1	0	0	1	1	1	0	X	0	X	0	1	X	0	X
13	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	0	X	0	X	0	1	X
15	1	1	1	1	0	1	1	0	X	1	X	0	X	0	X	1

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Table 2: Excitation Table of JK Flip Flop

Q n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

The Boolean function of clocked sequential circuit is determined from the state table 1. Symbol 'X' is denoted as don't care condition. The K-map method has been implemented for simply determining the Boolean function of clocked sequential circuit. K-maps plotted from the state table 1 has four state variables, they are A,B,C and D. Looking at the table 1, notice that the terms which are having output 1 has the corresponding cells marked with 1s and other cells are marked by zeros and don't care condition. The sum of the product form of Boolean expression can be plotted from the K-map. Derivations of K-map are shown in Table 3.

TABLE 3: Derivations OF K-MAP

	C'D'	C'D	CD	CD'
A'B	1	X	X	X
A'B	X	X	X	X
AB	X	X	X	X
AB'	X	X	X	X
$J_A = A'B'C'D'$				

	C'D'	C'D	CD	CD'
A'B	X	X	X	X
A'B	X	X	X	X
AB	0	X	1	0
AB'	X	X	X	X
$K_A = ABC'D$				

	C'D'	C'D	CD	CD'
A'B'	1	X	X	X
A'B	X	X	X	X
AB	X	X	X	X
AB'	X	X	X	X
$J_B = A'B'C'D'$				

	C'D'	C'D	CD	CD'
A'B'	X	X	X	X
A'B	1	X	X	0
AB	0	X	0	0
AB'	X	X	X	X
$K_B = A'BC'D'$				

	C'D'	C'D	CD	CD'
A'B'	0	X	X	X
A'B	0	X	X	X
AB	1	X	X	X
AB'	X	X	X	X
$J_C = ABC'D'$				

	C'D'	C'D	CD	CD'
A'B'	X	X	X	X
A'B	X	X	X	1
AB	0	X	0	0
AB'	X	X	X	X
$K_C = A'BCD'$				

	C'D'	C'D	CD	CD'
A'B'	0	X	X	X
A'B	0	X	X	X
AB	0	X	X	1
AB'	X	X	X	X
$J_D = ABCD'$				

	C'D'	C'D	CD	CD'
A'B'	X	X	X	X
A'B	X	X	X	X
AB	X	X	1	X
AB'	X	X	X	X
$K_D = ABCD$				

The logic circuits of the clocked sequential circuit are designed from the derivations of the k-map. The digital modulation circuit produces the sequence of switching pulses, these sequence of pulses are used for both the half cycles. Positive and negative half cycle switching pulses are separated by using auxiliary flip flop and NAND gates. The logic circuit of the clocked sequential circuit is shown in figure 4. The sequences of positive and negative pulses are given to the seven-level multilevel inverter semiconductor switching devices (IGBT, MOSFET).

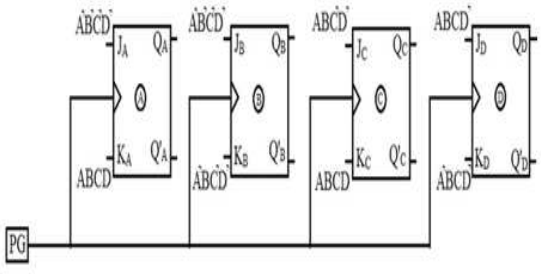

Figure 4: Logic Circuits of Clocked Sequential Circuit

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4. SIMULATION MODEL OF CASCADED MULTILEVEL INVERTER

In order to verify the proposed PWM method, extensive system of simulations is carried out through MATLAB/SIMULINK software. The simulation model of Clocked Sequential Circuit based seven level cascaded multilevel inverter is shown in figure 5. It contains digital logic devices like JK flip flop, AND gate, NOT gate, NAND gate and three single-phase full-bridge Inverter connected in series and sequence of switching pulses of clocked sequential circuits is separated by auxiliary flip flop and NAND gate devices and separated switching pulse fed seven-level cascaded multilevel.

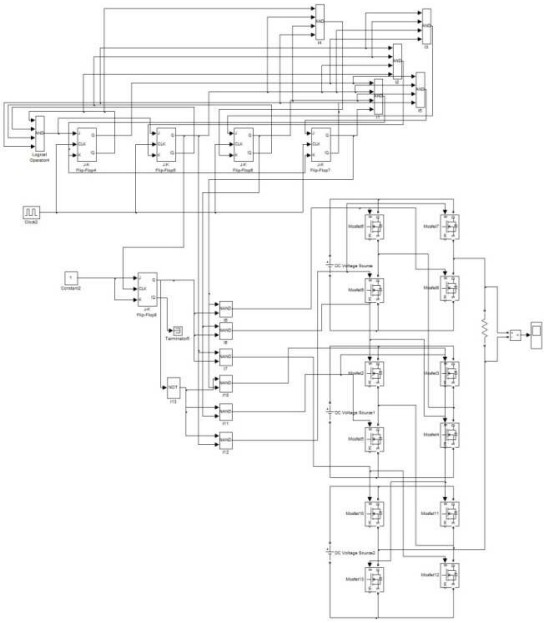

Figure 5: Simulation Model of Seven-level CMLI

5. RESULT AND DISCUSSION OF CMLI

In the simulation package the inverter is supplying an AC voltage to R load. The systems parameters chosen are Vdc = 0.2 kV, Load parameters: resistance of 100Ω. The clock pulse generator frequency is chosen as 650 Hz while the system frequency is 50 Hz. The inverter devices are assumed to be nearly ideal in this simulation. The digital modulating pulses are generated by the clocked sequential circuits. The simulation output result of the clocked sequential circuits is shown in figure 6. The sequence of switching pulses are separated by auxiliary flip flop and NAND gate devices, the separated switching pulse is shown in figure 7.

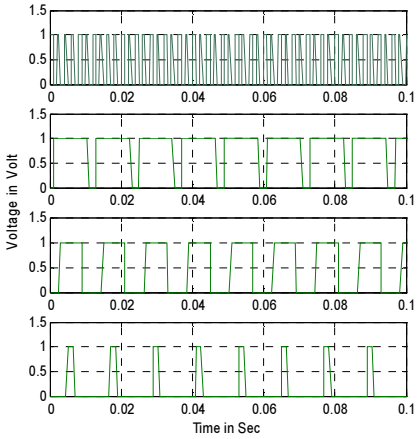

Figure 6. Output of Clocked Sequential Circuit

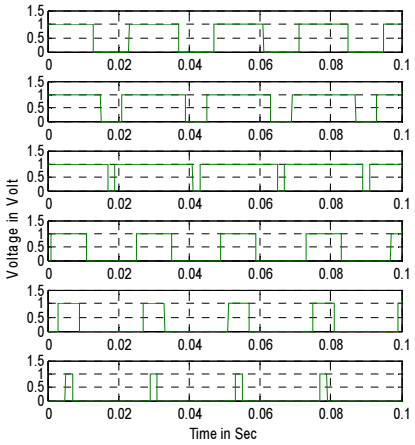

Figure 7: Switch Pulses of CMLI

These separated switching pulses are fed to the seven-level cascaded multilevel inverter. The single inverter output voltage and load current of seven-level cascaded multilevel inverter is shown in figure 8, and figure 9. The performance of the digital modulation algorithm proposed above is evident when considering voltage and load current.

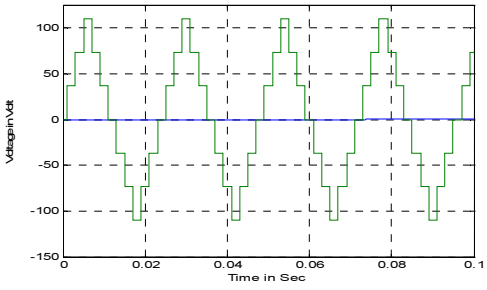

Figure 8: Output Voltage of CMLI

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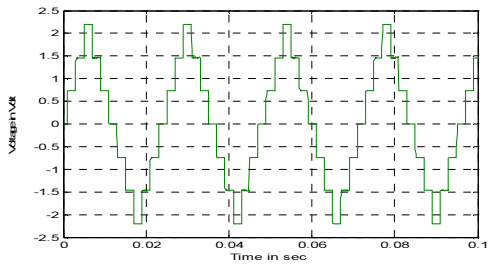


Figure 9: Load Current

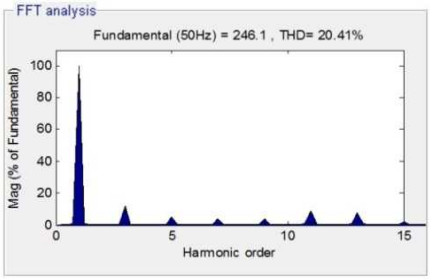
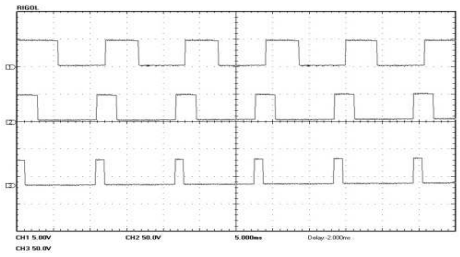


Figure10: Total Harmonic Distortion of voltage

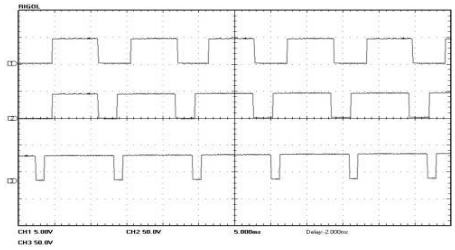
The effect of change in voltage on output power quality is shown in the plots of phase voltage spectra. The phase voltage spectrum is shown in figure 10. The total harmonic distortion of the cascaded multilevel inverter is 20.41%. Cascaded multilevel inverter output is fed to the resistive load for verifying the basic performance parameters of the inverter like voltage fluctuation, power frequency variations; because any variation present in the inverter means that the load current will be affected. The investigations of simulation result are shown in Figure. 8 to 10 from the simulation results it is shown that the inverter behavior is elegant. Using this digital modulation algorithm, the inverter power frequency can also change from minimum to the required frequency level by changing the clock pulse of the clocked sequential circuits.

6. HARDWARE RESULTS OF CMLI

The Seven-level cascaded multilevel inverter hardware results are illustrated. The synchronous sequential circuit generates sequential switching pulses which are separated every half cycle and applied to cascaded multilevel inverter H-Bridge switching devices, the H-Bridge inverter upper and lower switches operate as complementary functions. Note that S1 and S3 should not be closed at the same time, nor should S2 and S4, otherwise a short circuit would exist across the DC source. The clocked sequential circuit switching pulses are shown in figure11 (a) and (b) respectively.



(a)



(b)

Figure 11: Gate Voltages of Switching Device

The clocked sequential circuit based seven-level cascaded multilevel inverter output phase voltage is shown in figure 12. The seven-level cascaded multilevel inverter output phase voltage has lower harmonics. The phase voltage of the seven-level cascaded multilevel inverter is 192 volt, 50Hz. From the hardware investigation there is no voltage fluctuation and no power frequency variation in the clocked sequential circuit based seven-level cascaded multilevel inverter. This synchronous sequential circuit based seven-level cascaded multilevel Inverter attained 19.7% THD as shown in figure 13.

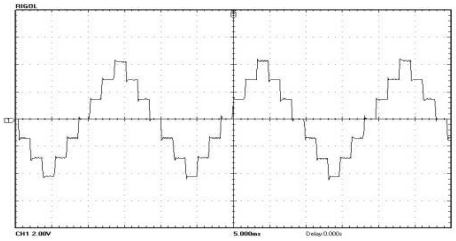


Figure.12: Output Phase Voltage of CMLI

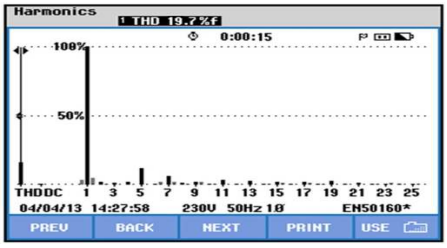


Figure 13: Total Harmonic Distortion of CMLI

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7. CONCLUSION

In the proposed method, seven-level cascaded multilevel inverter provides sinusoidal waveform using digital logic algorithm. The basic concepts and operational features of inverter and clocked sequential circuits based digital logic algorithms have been explored. The performance of the inverter and digital modulation algorithm has been improved when considering the voltage and load current. This method, ie; the cascaded multilevel inverter has the following features, they are- simplicity of control at circuitry level, the multilevel voltage source inverter can be built easily and implemented at a low cost, reduce the area of inverter circuits, adjustable frequency, ease of fault identification and low power consumption. The digital logic algorithm can be implemented for different topology of inverter and n level of inverter can be easily designed. The future scope of this digital logic algorithm based multilevel inverter is its implementation in a single chip using VLSI technology.

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