Journal of Theoretical and Applied Information Technology
31st July 2014. Vol. 65 No.3

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

DESIGN AND IMPLEMENTATION OF FACE DETECTION USING ADABOOST ALGORITHM

[1]SENTHILSINGH C, [2] M.MANIKANDAN

[1] Research Scholar, Department of Electronics, MIT,Anna University,Chennai, India
[2]Associate Professor,Department of Electronics,MIT,Anna University,Chennai, India
E-mail : [1] senthilsingh@gmail.com , [2] maniiz@annauniv.edu

ABSTRACT

Face recognition system is an application for identifying someone from image or videos. Face recognition is classified into three stages ie)Face detection,Feature Extraction ,Face Recognition. Face detection method is a difficult task in image analysis. Face detection is an application for detecting object, analyzing the face, understanding the localization of the face and face recognition.It is used in many application for new communication interface, security etc.Face Detection is employed for detecting faces from image or from videos. The main goal of face detection is to detect human faces from different images or videos.The face detection algorithm converts the input images from a camera to binary pattern and therefore the face location candidates using the AdaBoost Algorithm. The proposed system explains regarding the face detection based system on AdaBoost Algorithm . AdaBoost Algorithm selects the best set of Haar features and implement in cascade to decrease the detection time .The proposed System for face detection is intended by using Verilog and ModelSim,and also implemented in FPGA.

Keywords- *Adaboost, Face Detection, FPGA, Haar Classifier, Image Processing, Real-Time.*

1. INTRODUCTION

Face Detection System is to detect the face from image or videos. To detect the face from video or image is gigantic. In face recognition system the face detection is the primary stage. Figure 1 shows the various stages of face recognition system ie face detection, feature extraction and recognition. Now Face Detection is in vital progress in the real world

Guo proposed a two stage hybrid face detection system composed of the probability based face mask pre-filtering and pixel based[6]. Froba and Ernst[7] proposed a face detector consist of 4 phase cascade structure based on MCT-transformed images using the Adaboost learning algorithm. Knowledge-based methods use facial features, such as two eyes, a nose and a mouth [8]. Sung proposed the feature invariant methods based on facial features such as invariant to pose, lighting condition [9]. The matching methods of the template are calculated by the correlation between a test image and pre-selected facial templates [10]. Appearance-based, adopts machine learning techniques to extract features from a pre-labeled training set. The Eigenface method [11] is the most fundamental method for finding the features.The applications.Face Detection Technology is terribly vital in many fields like security services[1,2]. Several different sorts of techniques are there, among these for training the weak classifier Adaboost algorithm is employed by Vinola and Jones[3,4]. Lienhart proposed the rotated Haar like features to reinforce the detection performance of rotated faces [5]. face detection algorithms such as support vector machines [12], neural networks [13], statistical classifiers [14,15] and AdaBoost-based face detection [16] also used for detecting the face.

McCready [17] proposed a face detection method and implemented using nine FPGA boards for the Transmogrifier-2 configurable hardware system. Sadri et al. [18] proposed neural network primarily based face detection on the Virtex-II Pro FPGA. This face detection uses skin color filtering and edge detection to cut back the processing time. Wei et al. [19] proposed, face detection using FPGA for scaling input pictures and mounted-point expressions. The image size is simply too small (120×120 pixels) solely some parts of classifier cascade are literally implemented. Yang et al. [20] proposed low-price detection system using

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Cyclone II FPGA . Viola and Jones [21] explains regarding the face detection and applicable in some applications like digital cameras etc. The problems in viola jones are missing elements of faces and false detection. The main goal of my system is to solve the above mentioned problems.The proposed face detection system achieves a better detection and a lower false positive rather than the traditional adaboost algorithms.

The rest of the paper is organized as follows. Section II gives an overview of the Proposed System. Section III describes Face Detection Architecture. In Section IV, Simulation Result is introduced. Section V describes the Experimental Results. Conclusions are given in Section VI.

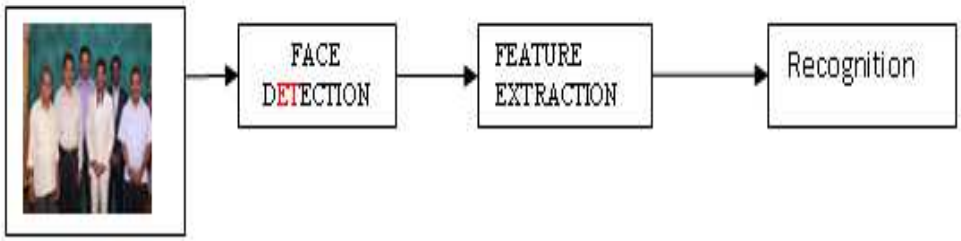


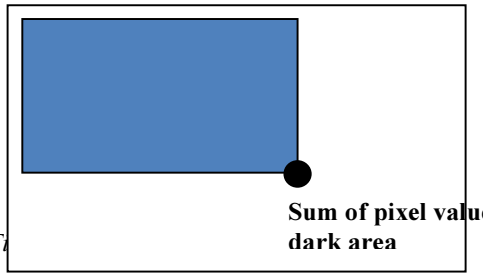
Figure 1: Stages of Face Recognition System

2. PROPOSED SYSTEM

Face detection is done using the viola jones method which consists of adaboost algorithm integrated with Haar features. It's the widely used method for real time detection. In this proposed system the detection is very fast. This algorithm only detects the face, but recognition is impossible. If anyone of the face features(eye, mouse, nose) is found, the algorithm permits the next step of detection. By using the rectangular section the face is detected .The oblong section is also known as sub-window. The rectangular size sub-windows have a fixed size (typically 24×24 pixels). This sub-window is scaled to get different size faces. The algorithm scans the entire image with this window and detects the face.

2.1 Integral Image

The summation of the pixel values of the first image is integral image.Each location value(x,y) of integral image is calculated as sum of the image's pixels left and above of location (x, y). Figure 2 illustrates the integral image generation. Figure 3a,Figure 3b explains the integral image generation.



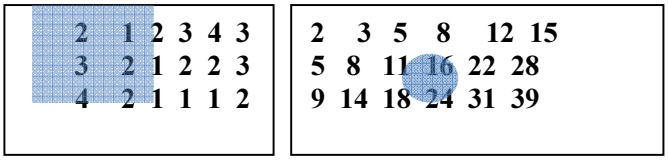


Figure 3:a)Normal Iimage Figure 3:b)Integral Image

2.2. Haar Features

Haar features are composed of either two or three rectangles. Face candidates searched the Haar features of the present stage. The weight and size of each feature are generated using a machine learning algorithm from AdaBoost. There are four basic types of haar features. These features will be used to evaluate the set of pixel intensity. The summation of the pixels in the white portion of the feature is deducted from the luminance summation of the pixels within the remaining black section. The representation of the image known as the integral image makes feature extraction faster. The commonly used haar features are specified in

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different sub-window as shown in the figure 4a, figure 4b.

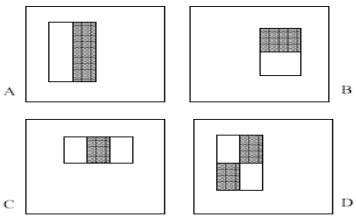

Figure 4:a) Sub Window

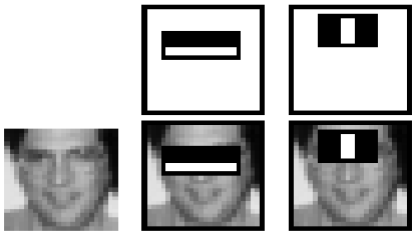

Figure 4: b) Examples of Haar Features

2.3 Adaboost Learning

The algorithm uses an image to process Haar features of a face in constant time. This algorithm uses different cascade stages to eliminate the non-face candidates. Each different stage consists of many different Haar features. The different feature is classified by a Haar feature classifier. Haar feature classifiers generate an output that can be given to the stage comparator. The stage comparator sums the outputs of the Haar feature classifiers and compares this value with a stage threshold to determine if the stage should be passed. Face candidate is concluded to be a face, if all stages are passed.Figure 5 explains about the cascade of stages, using the face feature each classifier can identify the face or non-face(F). If it is not a face then it directs to next classifier(T).

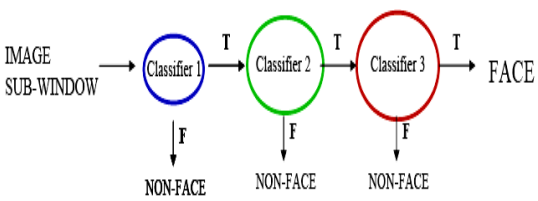

Figure 5: Cascade of Stages

3. FACE DETECTION SYSTEM ARCHITECTURE

Figure 6 explains the Face Detection Architecture. An image is extracted from digital camera or video. Primarily based upon the Haar features the feature is extracted. By using the Cascade classifiers, identify the image is having non-face or face. After identifying the face, only the face is extracted and recognized.

Given the example images (x1,y1),……..,(xn,yn) where yi=0,1 for –ve& +ve examples respectively.From the training examples, initialize weights w1,i=1/2m, 1/2l for yi=0,1 respectively

Then for t=1,……,T, Normalize the weights

$$\text{Wt,i«-}\ \frac{Wt,i}{\sum_{j=1}^{n} Wt,j}$$

So that Wt is the probability distribution.For each feature, j, train a classifier hj and the error is evaluated with respect to Wt.

$$\text{ie, } \varepsilon j=\sum_i Wi\,|hj(xi)-yi|$$

Then choose the best classifier.ie, choose the classifier ht, with the lowest error rate.Update the weights:

$$\text{Wt+1,i= Wt,i}\beta^{1-ei}$$

$$\text{Where}\ \beta t=\frac{et}{1-et}$$

ei= 0 if example xi is classified correctly,
ei= 1 otherwise.
Final classifier is the combination of the weak ones, weighted according to the error they had.

$$\text{h(x)=}\begin{cases} 1 & \sum_{t=1}^{T} \alpha t\ ht(x) \geq 1/2 \sum_{t=1}^{T} \alpha t \\ 0 & otherwise \end{cases}$$

$$\text{Where } \alpha t = \log \frac{1}{\beta}$$

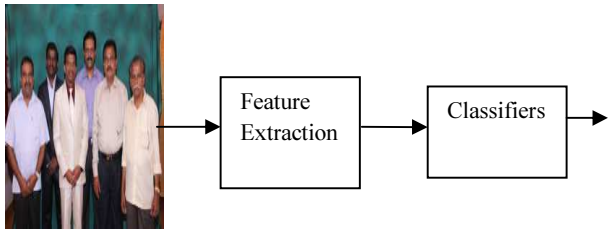

Figure 6: Face Detection Architecture

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4.SIMULATION RESULTS

The proposed system is designed using verilog and simulated within the Xilinx ISE 9.2i based Model Sim 6.3g environment.The Figure 7 shows the Simulation results for detecting face using Adaboost.

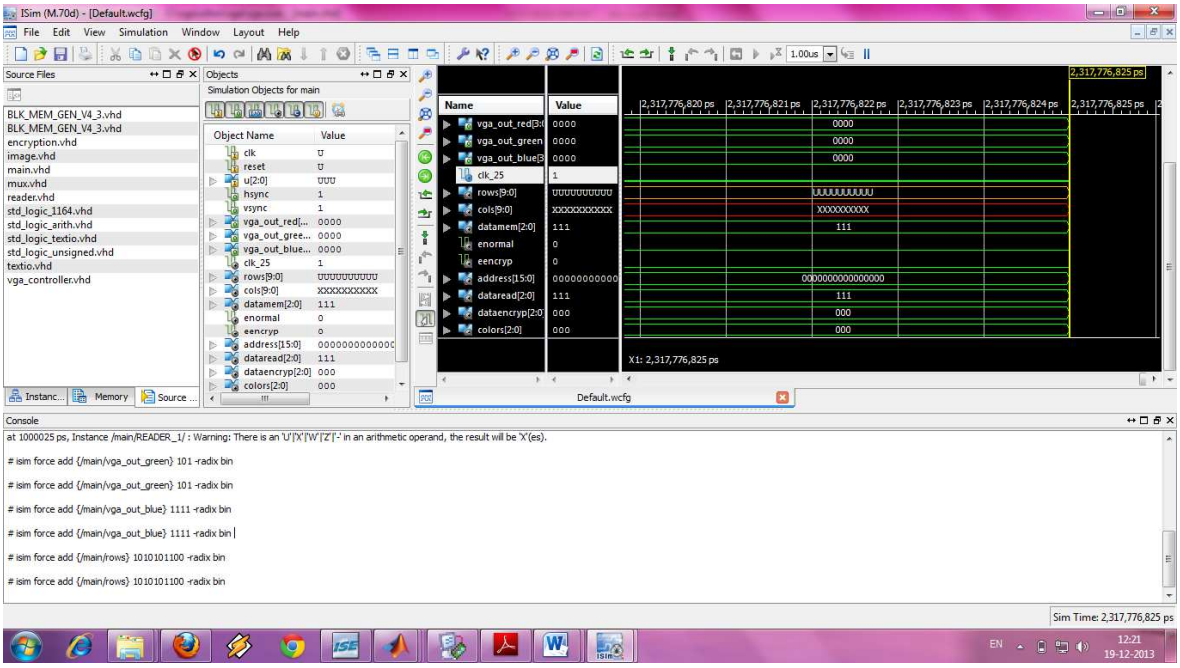

Figure 7: Simulation Results For Face Detection

4.1 Fpga Implementation

The proposed system is synthesized within the Xilinx ISE 9.2i based Model Sim 6.3g software tool and it is programmed to the targeted Xilinx Spartan 3E family of FPGA Device. The various levels of implementation such as Synthesis report, RTL View, Place and Route Report and Device Programming is given below.

4.2 SYNTHESIS REPORT

The Table 1 shows the synthesis report. Table 1shows the total gates, Macro Statistics and total memory usage is 264900 kilobytes. The table tells the information about the target FPGA device utilization.

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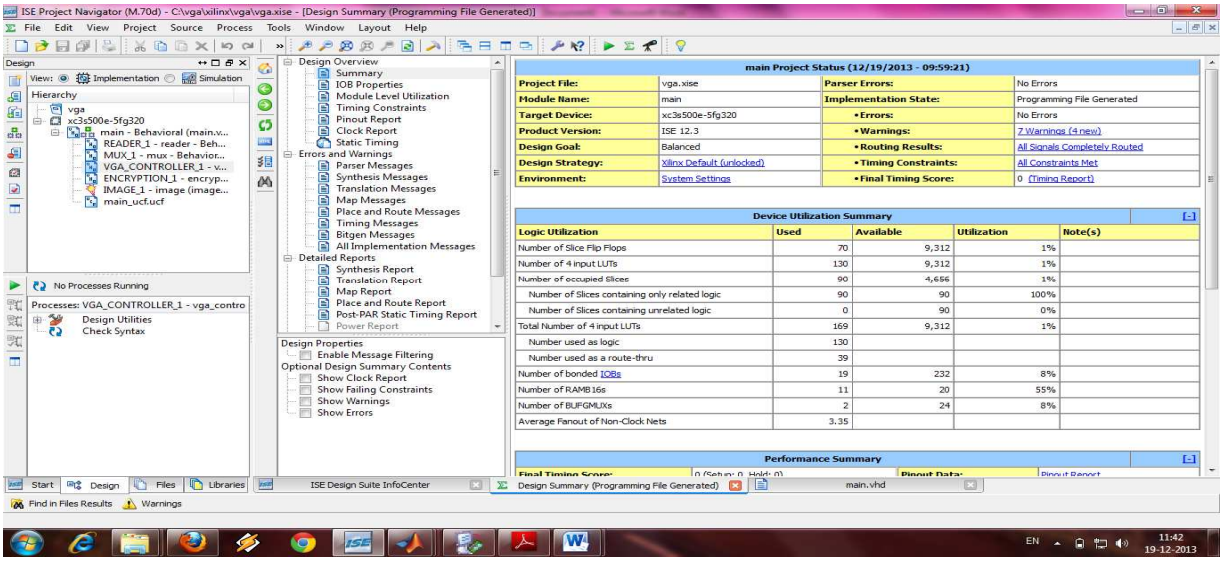

Table 1: Synthesis Summary

4.3. RTL View

Figure 8 gives the visualization of Register Transistor Logic (RTL) views in the form of schematic diagrams. This figure gives the RTL schematic diagram .

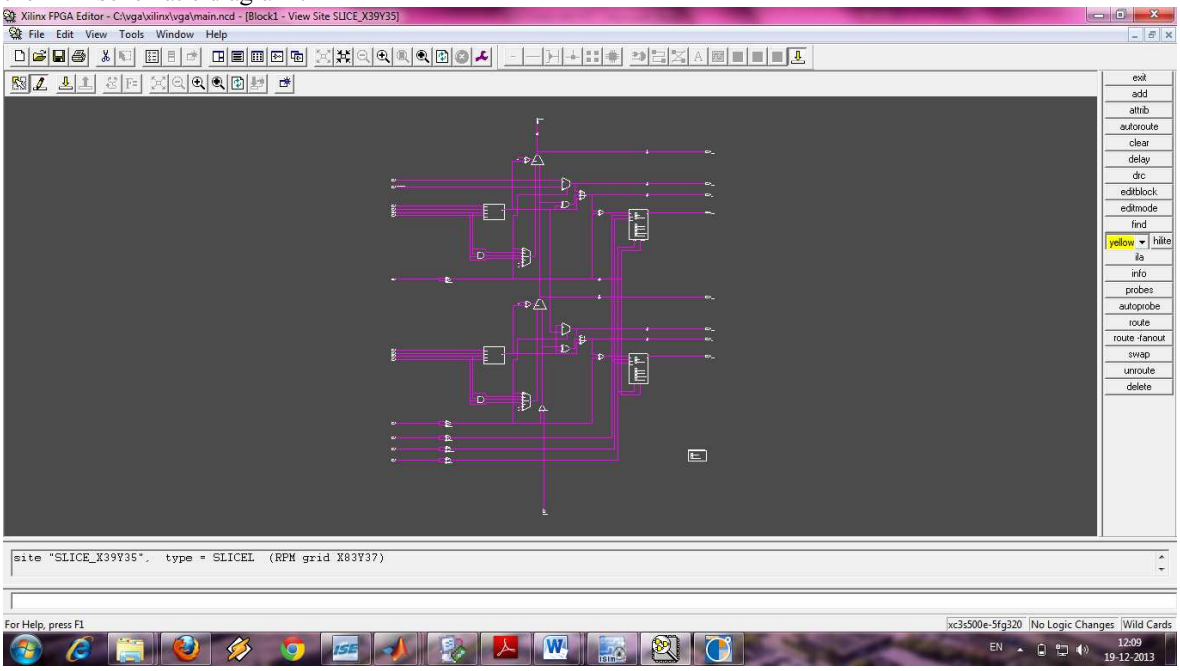

Figure 8: RTL Schematic diagram

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4.4. Place And Route Report

This section gives FPGA device utilization summary which gives the information for proper layout in the form of Place and Route report. The timing synchronization of CPU are given below with the REAL time environment .

4.4.1. device utilization summary

Number of Slices: 91 out of 4656 1%
Number of Slice Flip Flops: 70 out of 9312 0%
Number of 4 input LUTs: 169 out of 9312 1%
Number of IOs: 19
Number of bonded IOBs: 19 out of 232 8%
Number of BRAMs: 11 out of 20 55%
Number of GCLKs: 2 out of 24 8%
Minimum period: 6.073ns (Maximum Frequency: 164.673MHz)
Minimum input arrival time before clock: 3.639ns
Maximum output required time after clock: 4.040ns
Maximum combinational path delay: No path found

4.5. Device Programming

After successful process of synthesis the Target Selected Device 3s500efg320-5of Spartan 3E is connected to the system through USB port. The pin assignment is specified in the User Constraint File (UCF). The functional verification is carried out by using a pattern generator.

5. EXPERIMENTS/RESULTS

A high frame processing rate and low latency are important in many applications. The performance of the proposed system for the face detection system has low latency and fast detection. Face detection system when it is applied to a camera or video, which produces images consisting of 240×120 pixels at 60 frames per second. The detected face is in 12*12 pixels. The figure 9 a,figure 9 b explains how the face is detected from the image and extracted each face from the image and displayed in separate window in 12*12 pixels. These extracted faces are recognized by different methods. Figure 10 shows the realsetup of face detection using FPGA.

Figure 9:a) Face Detection

Figure 9:B)Face Extracting From The Image in 12 x 12

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Figure 10: Real Setup using FPGA for Face Detection

6. CONCLUSION

The proposed system explains about the Face Detection System using Ada Boost Algorithm. Face detection is an crucial step in many applications related to computer vision and image processing. The proposed System improves the fast detection , the power consumption , decrease the computation time. This paper presents a set of experiments for detecting and extracting the face. The result's that the detector is efficient in terms of detection rate notwithstanding a non negligible number of false alarms.The computation of the classifier is very fast as a result of the utilization of straightforward rectangular features which are easily computed with the integral image.The learning algorithm AdaBoost selects the best set of Haar-like threshold. Then the implementation in cascade which permits to decrease the detection time while increasing the detection rates.

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ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

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