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OPTIMIZED DIGITAL FILTER ARCHITECTURES FOR MULTI-STANDARD RF TRANSCEIVERS

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ABSTRACT

This paper addresses on two different architectures of digital decimation filter design of a multi-standard Radio Frequency (RF) transceivers. Instead of using single stage decimation filter network, the filters are implemented in multiple stages using FPGA to optimize the area and power. The proposed two types of decimation filter architectures reflect the considerable reduction in area & power consumption without degradation of performance. The filter coefficients are derived from MATLAB and the filter architectures are implemented and tested using Xilinx SPARTAN FPGA .The Xilinx ISE 9.2i tool is used for logic synthesis and the Xpower analysis tool is used for estimating the power consumption. First, the types of decimation filter architectures are tested and implemented using conventional binary number system. Then the two different encoding schemes namely i.e. Canonic Signed Digit (CSD) and Minimum Signed Digit (MSD) are used for filter coefficients and then the architecture performances are tested .The results of CSD and MSD based architectures show a considerable reduction in the area & power against the conventional number system based filter design implementation.

Keywords: Digital Transceiver, Multi-rate Digital Filter, Multistage Decimation Filter, FPGA, Area Reduction, Low Power Design.

1. INTRODUCTION

RF communication transceivers emphasizes both higher integration to meet consumer demand of low-cost, low-power, less area personal communication devices and the ability to adapt to Multiple Communication Standards. Higher integration can be achieved by using receiver architectures and circuit techniques that eliminate the need for external components. Receiver architecture that performs channel select filtering based on-chip at baseband allows for the programmability necessary to adapt to Multiple Communication Standards[3]. In audio applications of wireless transceivers, the use of oversampled Sigma Delta Analog to Digital ($\sum \Delta$ -ADC) converter has become popular because of its high resolution, improved performances and flexibility in selection of sampling rates. Consider an analog input signal with maximum frequency of f_x , which is sampled by the oversampling Sigma Delta Analog to Digital converter[4]. The $\sum \Delta$ -ADC

converter samples the input signal with rate much greater than Nyquist rate 2f_x. The oversampling ratio of the $\Sigma\Delta$ -ADC is defined as M =f_s/2f_x, where f_s is the sampling rate of $\sum \Delta$ -ADC converter and 2f_x is the Nyquist rate. Typical audio application consists of an oversampled $\sum \Delta$ -ADC followed by a decimation filter. The digital decimation filter is used to perform filtering operation and sampling rate down conversion so as to extract the original signal band or the band of interest from the oversampled $\sum \Delta$ -ADC. A programmable low-pass digital decimation filter of a RF transceiver can select a desired channel in the presence of both strong adjacent channel interference and quantization noise from the digitizing process.

Several literatures deal with the design issues of decimation filters for wireless communication transceivers. In this paper, a cascade CIC–HB.FIR filter implementation of the decimation filter using Conventional, CSD and MSD based multipliers are addressed in detail. This paper is organized as



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follows: Section 2 describes the digital receiver architecture suitable for multi-standard operation. Section 3 deals with the concepts of decimation process. Section 4 presents the two different multistage decimation filter architectures and types of filters used for implementation of each stage. In Section 5 Canonic Signed Digit (CSD) and Minimum Signed Digit (MSD) representation are explained in detail[8]. Section 6 provides the simulation results of the various types of decimation filter architectures. Finally Section 7 describes the conclusion and future work.

2. DIGITAL RECEIVER ARCHITECTURE

This section deals with the digital receiver architecture, which emphasizes high integration and multi-standard capability. High integration can be achieved by utilizing a receiver architecture that performs base band channel select filtering on-chip. This enhances the programmability to different dynamic range, linearity and signal bandwidth so as to meet the requirements of multiple RF standards. Typical block diagram of a digital transceiver is shown in Figure 1. An overview of a digital receiver will readily confirm that its main task is to take a signal sampled at a high rate, down convert it and filter it-through low-pass filter and then decimate it and finally format it into one or more of several forms. After demodulation, this signal is converted back to analog form and then applied to power amplifier and loudspeaker.



Figure 1: Architecture Of Digital Transceiver

The input analog signal is converted to digital form with the aid of the A/D converter. A wide band, high dynamic range sigma-delta modulator can be used to digitize both the desired signal and potentially stronger adjacent channel interferences. Next, this signal compromising of ones and zeros is applied to a digital Mixer, just as in the case of analog receiver. Only at this time, the signal is applied to two Mixers driven by digital In-phase (I) and Quadrature (Q) components of a local oscillator signal which in turn is provided by a digital frequency synthesizer. In essence, the input signal is multiplied with the sine and also with the cosine output of the local oscillator. Just as in the case of the analog receiver, the output of the Mixer consists of sum and difference frequencies extending the way up in the sampled data spectrum. To remove the higher order components and to recover only the baseband signal, the signal is passed through a decimating low pass filter. This digital filter has the property of reducing the sample rate of the input signal by some factor(decimation factor), which can be programmed to be as low as 1 or as high as 16,384.The filter output signal is formatted and this is made available in one or more of several forms. As far as the demodulator function is concerned, it is best performed digitally in a DSP processor outside the digital receiver chip. Demodulator is followed by a D/A converter and speaker to complete the analogy between the analog and digital receivers.

3. DECIMATION PROCESS

To reconstruct a signal from its sample values, a band-limited signal only need to be sampled at a rate in excess of the Nyquist rate. Speech or low bandwidth signals may be sampled well above their Nyquist rate to bypass problems associated with the low rate analog to digital conversion. This is achieved using Sigma Delta A/D converter($\Sigma\Delta$ -ADCs) in the digital receivers. One of the key features of Sigma Delta A/D converter is that the modulator is over sampled compared to the

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expected output sample rate. Decimation is an important component of over sampled analog to digital conversion ($\Sigma\Delta$ - ADCs). A higher order decimation filter is used to convert the over sampled signal into usable baseband signal. The decimation process simply reduces the output sample rate while retaining the necessary information. It transforms the digitally modulated signal from short words occurring at high sampling rate to longer words at Nyquist rate. To extract the signal information, the signal must be first down-converted to base band. A multi-stage decimation filter is used to perform this function.

As far as initial stage of decimation is concerned, the word rate decreases to about four times the Nyquist rate. In all these cases, high decimation rates are required to reduce the output bandwidth which can be processed with conventional hardware. Due to over sampled $\Sigma\Delta$ - ADCs , only small fraction of the total noise power falls in the frequency band of interest. The noise power outside the signal band can be greatly attenuated with a digital low pass decimation filter following the $\Sigma\Delta$ -ADC. Decimation is often performed in several stages instead of a single stage. This leads to higher decimation factor in the first filter stage as compared with decimation filters of similar input and output data word lengths in the consecutive stages. However, the word length differs between the consecutive stages. This is especially important for $\Sigma\Delta$ ADCs, as the input to the decimator may be only one bit while the output precision can be, say, 16 bits or more. Multistage decimation filter architecture reduces the overall complexity in terms of area and power at each stage of filter design[10].

4. MULTISTAGE DECIMATION FILTER

The sampling rate is down converted from the oversampled rate of sigma-delta modulator to a data rate that can be conveniently processed by existing DSP processors using decimation filters. This minimizes the power consumption of DSP processors for demodulation and equalization. The purpose of decimation filter is to remove all the out-of-band signals and noise and to reduce the sampling rate from oversampled frequency of the $\Sigma\Delta$ - ADC to Nyquist rate of the channel [7]. The decimation filter consists of a low-pass filter and a down-sampler. It is possible to perform noise removal and down conversion with a single FIR filter stage. The filter order N of FIR low-pass filter is given by eqn. (1), where D_{∞} is a function of the required ripples δp and δs in the pass-band and stop-band respectively, Fs is the sampling frequency and Δf is the width of transition band.

$$N \approx D_{\infty}(\delta p, \delta s) (F_{S}/\Delta f)$$
(1)

As the $\Sigma\Delta$ - ADCs are oversampled, the transition band is small relative to the sampling frequency leading to excessively large filter orders and this leads to a lot of multiplication operations. The power consumption of the filter depends on the number of taps as well as the rate at which it operates. So computational complexity is high for single stage implementation of decimation filter and consumes more power. Implementing decimation filter in several stages reduces the total number of filter coefficients. Subsequently, the hardware complexity and computational effort are reduced in multistage approach. This will result in less area and low power consumption. A multistage decimation filter system consists of a cascaded structure of several single stage decimation filter systems. The 'ith' stage of multistage system performs decimation by a factor of 'R_i' such that the overall decimation factor 'R' is given by the eqn. (2)

$$P R= \Pi Ri, (2)$$

$$i=1$$

Where 'P' is the total number of stages of multistage decimation filters. The individual filter of each stage is designed within the frequency band of interest in order to prevent aliasing in the overall decimation process. The performance of a decimation filter depends on the filter architecture and the order of each stage of a multistage decimator. FIR filters are widely used in decimators because of its linear phase characteristics. Multiple contributions are proposed in previous works for multi-standard multi stage digital filters for decimation and channel selection. Multistage decimation reduces the overall complexity of system by decomposing the decimation factor into several sub factors. Thus, each stage requires lower order filters. Moreover, after four to five stages, the filter complexity is not further reduced. Therefore, a trade off between the number of stages and complexity must be achieved.

FIR filter are used in down converters because some modulation schemes requires linear phase. In wireless communication devices, the battery life must be maximized. Therefore, high performance blocks with low power consumption and small area are required [1]. The implementation of decimation filter for multiple standards on a single device is very demanding in terms of area and power. With

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an efficient decomposition of decimation factor considering common blocks between different communication standards, it is possible to have an efficient design. Thus, few different blocks could be implemented in a configurable fashion.Two different filter architectures used in this paper are described in the following sections in detail.

4.1. Architecture I:

Decimation Filter with Conventional MAC Unit

In this architecture, decimation filter is implemented using two filter stages with a overall decimation factor of 32. The decimation filter architecture consists of first stage representing High Order Decimation Filter (HDF) and second stage representing Corrector Finite Impulse Response (FIR) filter and implemented using conventional binary number system with conventional MAC unit as shown in figure 2.



Figure 2: Two Stage Decimation Filter With Conventional MAC Unit

4.1.1. Cascaded Integrator Comb (CIC) Filter

The first filter section is called the HDF and it is normally optimized to perform decimation by large factors. It implements a low pass filter function using only adders and delay elements instead of a large number of multiplier/accumulators that would be required using a standard FIR filter. An efficient architecture of HDF stage belongs to a class of multi-rate multiplier-less systems referred to as Cascade of Integrators-Comb (CIC) filters[6]. In fact, in its recursive form, the CIC filter is multiplier less and presents low complexity properties. The fifth order CIC filter structure is shown in figure 3. It is constructed using only integrators and differentiators. Blocks R represents the decimator .The CIC filter design approach consists of 5 stages of Integrator section followed by a 5 stages of differentiators. The cascaded structure of integrators and combs provides a better solution for low power CIC filters as shown by figure 3.



Figure 3: Fifth Order Cic Filter Structure

The integrator and the comb filter operations are performed using registers and adders only. Figure 4 shows the equivalent digital circuit representation of the integrator stages. Each accumulator is implemented as an adder followed by a register in the feed forward path. The integrator is clocked by the sample clock, CK_IN. The output of the Integrator section is latched on to the decimation register by CK_DEC. The output of the decimation register is passed to the Comb Filter Section. The Comb section consists of five cascaded comb filters. Each Comb filter section calculates the difference between the current and previous integrator output. Each comb filter consists of a register which is clocked by CK_DEC followed by an subtracter where the subtracter calculates the difference between the input and output of the register. Figure 5 describes the equivalent digital circuit representation of the 5- stage comb filter.



Figure 4: Digital Circuit Implementation Of 5-Stage Integrator



Figure 5: Digital Circuit Implementation Of 5-Stage Comb Filter Section

4.1.2. Characteristics of CIC filter

The integrator section of CIC filter consists of N ideal digital integrator stages operating at high sampling rate, f_s . Each stage is implemented as a one-pole filter with a unity feedback coefficient. The system function for a single integrator is given by eqn. (3).

$$H_{I}(z) = 1/(1-z^{-1})$$
 (3)

The comb section operates at the low sampling rate f_s/R , where R is the integer rate change factor. This section consists of N comb stages with a differential delay of M samples per stage. The differential delay is a filter design parameter used to control the filter's frequency response. In practice, the differential delay is usually held at M = 1 or 2. The system function for a single comb stage referenced to high sampling rate is denoted by eqn. (4).

$$H_{\rm C}(z) = (1 - z^{-\rm RM})$$
 (4)

Where R - Decimation ratio M - Differential delay

N - No. of stages

It follows from eqn. 3and eqn. 4 that the system function for the composite Nth order CIC filter referenced to the high sampling rate, fs is denoted by eqn. 5 as

$$H(z) = H_{I}^{N}(z) * H_{C}^{N}(z) = (1 - z^{-RM})^{N} / (1 - z^{-1})^{N}$$

= $[\sum z^{-k}]^{N}$ (5)

where k ranges from 0 to RM-1

It is implicit from the last form of the system function that the CIC -HDF filter is functionally equivalent to a cascade of N uniform FIR filter stages[9].

4.1.3. Corrector FIR Filter

The second filter stage in the top level block diagram of architecture I is a corrector Finite Impulse Response (FIR) filter which performs the final shaping of the signal spectrum and suppresses the aliasing components in the transition band of the HDF. This enables the Decimation filter to implement filters with narrow pass bands and sharp transition bands. The Corrector FIR filter structure used for architecture I is shown in figure 6.The FIR is implemented in a transversal structure using a single multiplier/accumulator (MAC) and RAM for

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storage of data and filter coefficients. The corrector FIR is designed with the decimation factor of two[2]. The 16-bit output of the HDF output register is written into the data RAM on the rising

edge of CK_DEC. The Coefficient RAM stores the coefficients for the current FIR filter being implemented. The coefficients are loaded into the Coefficient RAM over the control bus.



Figure 6: Corrector FIR Filter Using MAC Unit

4.2. Architecture II Cascaded Multistage Decimation Chain

The decimation filter is a block that reduces the data rate from IF to base band domain. Different communication standards require large factor of decimation resulting in large orders of filter networks. Multistage decimation reduces the overall complexity of system, by decomposing the decimation factor in to several sub factors. Thus, each stage requires lower order filters. However, the use of several stages will increase hardware complexity. FIR filter are used in down converters because some modulation schemes requires linear phase[12]. In wireless communication transceivers, the battery life must be maximized. Therefore, high performance blocks with low power consumption and small area are required. The implementation of decimation filter for each standard on a single device is very demanding in terms of overall area and power dissipation. However, with an efficient decomposition of decimation factor and considering

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common blocks between different communication standards, it is possible to have an efficient design of multi-standard transceivers. Thus, few different blocks could be implemented in a configurable fashion to meet the multi-standard filter circuits requirement.

4.2.1. Decimation Chain Structure

Figure 7 shows the Cascaded Multistage Decimation Chain architecture for two different standards with the decimation factors of 8 and 32. The aim of this architecture is to reduce multiplication operations. To reach this goal,

multiplier-less comb filters are used for the first stage similar to architecture I. On simulations, the last two stages of each standard cannot be comb filters, because they don't remove the inband noise level sufficiently. That's why, it was decided to use half band filters for the two last stages. They exhibited good results and excellent out-of-band signal attenuation. The proposed architecture II supports three comb filter stages and 4 stages of half band filters to meet multi-standard requirements. Since the first comb filter stage is used commonly for both the standards, this architecture considerably reduces the area and power of the multi-standard transceiver.



Figure 7: Cascaded Multistage Decimation Chain Architecture

4.2.2. CIC Filter Structure

The fifth order CIC filter structure resembles as that of architecture I but the implementation of CIC filter integrators and differentiators stages of architecture II differs from architecture I. Figure 8 shows the basic integrator stage of CIC filter used in this architecture- its Z transform and its equivalent digital circuit in HDL. Thus the single accumulator (Integrator) unit is implemented in HDL using 14-bit adder and a register by avoiding complex multiplexer stages ,when compared with architecture I. In a similar fashion, the differentiator (Comb filter) stage of CIC filter in Z domain and its digital equivalent circuit are represented as shown in figure 9. Thus the comb stage is designed in HDL using a subtractor and a register networks. This architecture results in a considerable reduction in area and power ,when compared to the first architecture. Simulation environment states that further reduction in area and power can be achieved by changing the encoding scheme of filter coefficients from conventional binary number system to Canonic Signed Digit (CSD) and Minimum Signed Digit (MSD) Number systems.



Figure 8: Accumulator In Z-Transform And Its Digital Circuit Implementation



Figure 9: Differentiator In Z-Transform And Its Digital Circuit Implementation

4.2.3. Half Band Filter

The CIC filter is followed by an half band FIR filter for further down-sampling .The half band FIR filter is used instead of another CIC due to the fact that the pass band of CIC consists of distortions and the half band FIR can be designed in such a way that its frequency response compensates for the distortions created by CIC stages. Since the down-sampling rate of half band filter is chosen to be 2,

special type of symmetric coefficients type FIR filter can be used for the architecture II- meaning that the coefficients of an odd N tap (N-1 order) half band FIR can be represented by *Ceil* [(N-1)/4] +1 numbers[11]. The half band filter significantly reduces the hardware resources needed. The half band filter structure is shown in figure 10.The order of the half band filter used in this design is 14(15 taps) with the filter coefficients quantized for 8-bit precision.



Figure 10: Structure Of Half Band Filter

5. CO-EFFICIENT REALIZATION USING CSD AND MSD REPRESENTATIONS

The CSD representation is a radix-2 signed digit system with the digit set (1,0, _1). For any binary number, the CSD representation is unique and it satisfies the following two properties: first property is that the number of non zero digits are minimal and the second property is that adjacent two digits can never be nonzero digits i.e. the product of adjacent two digits will always be zero. This representation is widely used in multiplier less implementations of filter design with respect to filter coefficients because it reduces the hardware requirements due to the minimum number of nonzero digits. Any N digit number in CSD format has at most (N+1)/2 non-zero digits thus requiring only that much number of adders/ subtractors. On an average, the number of non-zero digits in CSD is reduced by 33%, when compared with the conventional binary number system. To obtain the CSD representation of a number, start processing its binary representation from the least significant digit to the most significant digit and replace repeatedly all the sequences found as 01...1 by a sequence 10...01 with same number of digits[5]. The conversion table shown in Table 1 is used to obtain the CSD number of a given binary number. 20th July 2014. Vol. 65 No.2

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Table 1. Csd Conversion Table

	Inputs	Outputs				
State	b _{i+1}	b _i	ci	Next State		
0	0	0	0	0		
0	0	1	1	0		
0	1	0	0	0		
0	1	1	-1	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	-1	1		
1	0	1	0	1		

If the second property of CSD is relaxed, then it leads to MSD representation. Although CSD representation is optimal for one constant (filter coefficient-in our case) and it provides unique solution, it is not suitable for common subexpression procedures of multiple constants. As the CSD representation is unique, it has received much attention and there are many methods of converting a given binary number into the CSD representation. The uniqueness is important in terms of mathematics but not in implementing hardware units. In general, the MSD representation providing multiple representations yielding the same value is more flexible than the CSD representation. This redundancy can result in smaller hardware units than those generated from the CSD representation provided appropriate MSD representation is selected for each constant. Thus the MSD representation is a superset of CSD number system and it provides a number of forms.

The MSD number system is appropriate in finding common sub expressions of multiple constants, in case proper MSD representation is selected for each constant to be synthesized. Since the MSD number system has an effect on the number of additions in the decomposed multiplication block and the number of common sub-expressions that can be eliminated, it has significant bearing on the reduction of area and power consumption. The advantage of using the MSD representation for a coefficient results from increasing the possibilities of sharing partial terms between coefficients. This results from the fact that, in general, there exist several alternatives to represent a given coefficient in MSD. Consequently, there are more ways to decompose the coefficient with different partial terms that can be shared with other coefficients.

6. SIMULATION RESULTS

The decimation filter design specification is shown in Table 2. The input signal frequency is chosen as 64 MHz and the decimation factors are chosen to be 8 and 32 respectively for the multistandard structures. The pass band of the filter circuit with the decimation factors of 8 and 32 will be 8 MHz and 2 MHz respectively. The pass band ripple and the stop attenuation are taken to be 0.001 and -60 dB. The filter circuit performance has been tested first using Matlab and the filter co-efficients are derived as per the given specifications of Table 2. For the implementation of decimation filter architectures in Spartan FPGA, the filter coefficients derived from Matlab are encoded in conventional binary number system, CSD and MSD representations. In both the architectures, the overall multistage filter networks are implemented on Xilinx Spartan FPGA .The area in terms of total gate count is analyzed for the architectures and the power analysis are carried out using the power estimating tool Xilinx Xpower Analyzer. Table 3 shows the comparison results of both decimation filter architectures in terms of total gate count, Number of slices, LUTs, IOBs, flip-flops and power consumption with respect to conventional, CSD and MSD number systems.

Table 2. Decimation Filter Specification

Specification Parameters	Standard I	Standard II
Decimation Factor	8	32
Pass Band	0 to 8MHz	0 to 2MHz
Pass Band Ripple	0.001	0.001
Cut Off Frequency	8.4 MHz	2.4 MHz

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Stop Band Attenuation	-60 dB	-60 dB
Output Word Length	16 bits	16 bits

Table 3.	Ca	omparison	Of	Deci	nation	Fi	ilter Arci	hitectur	es

S.No.	Architecture Type	Number	Total	No.	No.	No.	Logic	IOB	Total
		System	Gate	of	of	of			Power
		Representation	Count	Slices	FF	LUT			(mW)
1.	(I) Two Stage Decimation	Conventional	17624	554	492	822	770	207	1278
	Filter	Number System							
2.	(II) Cascaded Multistage		4279	467	392	442	278	36	57.45
	Decimation Chain								
3.	(II) Cascaded Multistage	Canonic Signed	3986	235	279	337	278	36	50.11
	Decimation Chain	Digit (CSD)							
4.	(II) Cascaded Multistage	Minimum	3172	154	92	163	138	27	42.77
	Decimation Chain	Signed Digit							
		(MSD)							



Figure 11: Frequency Response Of CIC Filter



Figure 12: Frequency Response Of Half Band Filter



Figure 13: Frequency Response Of Decimation Filter

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4650 ns Figure 15: Simulation Result Of Five Stage Comb Filter Output

Cursor 1

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🔶 /hb/clk			www.jatit.org												E-ISSN: 1817-3						
	1																				
🔷 /hb/rst	1																				
⊡	0101	0101		0110		1110		1010		0010											
⊕	0000000000000	0001011001000100				00010110	011101	00011100	01110	200011110	011000	0011010	10100	0010010	111						
⊕	0000001101010111	0000001101010111		0000010	000000	0000100	101011	00000110	10101	200000001	0101011	0									
⊞	**********	0000000011011100				10000000	100001	100000010	01101	100000001	10111	10000000	00101100	0							
⊕	**********	0001001000010001						00010101	10101	200110010	010010	0010010	000100	00000111	100						
⊕	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	0000010000110011		0000010	011011	00001010	001100	00001001	00010	100000011	00001	10000000	10101110)							
⊡	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	0001011001000100		0001011	011101	0001110	01110	100011110	11000	100110101	10100	10010010	11010	00001000	<u>011</u>						
⊡	0101	0101			0110		1110		1010		0010										
⊡	υυυυ	0101				0110		1110		1010		0010									
⊡	υυυυ	0101					0110		1110		1010		0010								
⊕	υυυυ	0101						0110		[1110		1010		0010							
⊡	0101	0101		0110		1110		1010		10010											
⊕	0000001101010111	0000001101010111		0000010	000000	0000100	101011	00000110	10101	10000000	0101011	0									
⊡	000001010000000	0000010100000000		0000011	000000	00001110	000000	00001010	00000	200000010	0000000	0									
⊕	000000101000000	0000000101000000		0000000	110000	0000001	110000	200000010	10000	00000000	01000000	0									
⊡ /hb/u0/w3	000000001010000	0000000001010000		0000000	001100	100000000	011100	100000000	10100	100000000	00010000	0									
⊡ /hb/u0/w4	000000000010100	0000000000010100		0000000	000011	20000000	000111	100000000	00101	100000000	00000100	0									
⊕	0000001111000000	0000001111000000		0000010	010000	00001010	010000	00000111	10000	(0000000	1000000	0									
⊕	0000001101110000	0000001101110000		0000010	000100	0000100	110100	00000110	11100	10000000	0110000	0									

Figure 16: Simulation Result Of Half-Band Filter Using CSD Representation

🔷 /hb/clk	1																
🔷 /hb/rst	0																
⊕	1010	0101					1101		0001		1001		1010				
⊕	0010110010001000	υυυυι	υυυυυι	υυυυυ	0001011	001000100)		0001101	110011	0001010)11111	0011010	00101	0000101	11010	10
⊕	0000011010101110	000000	11010101	11			(0000100)	010101	20000000	010101	0000011	00000	20000011	10101110	1		
⊕	0000000110111000	000000	00110111	00					20000001	000111	20000000	00101	20000000	10001	0000000	1011100	0
⊕	0010010000100010	000100	10000100	01							0010111)11111	20000001	10011	0010000	10000	10
⊕	0000100001100110	000001	00001100	11			0000100	10001	0000001	011100	00000110	000101	0000100	000111	0000100	0110011	0
⊡- → /hb/a2	0010110010001000	000101	10010001	00			0001101	10011	0001010	011111	0011010	00101	10000101	11010	0010100	011101	0
⊕	1010	0101						1101		0001		1001		1010			
⊕	1010	0101							1101		0001		1001		1010		
⊞	1010	0101								1101		0001		1001		1010	
⊕	1010	0101									(1101		0001		(1001		1
⊕	1010	0101					1101		0001		(1001		1010				
⊕	0000011010101110	000000	11010101	11			0000100	10101	0000000	010101	0000011	000000	0000011	10101110	1		
⊕	0000010100000000	000000	10100000	00			00000110	10000	10000000	010000	0000010	010000	0000010	100000000			
⊡- → /hb/u0/w2	000000101000000	000000	00101000	00			0000000	10100	0000000	000100	<u> 10000000</u>	100100	0000000	10100000	1		
⊡- → /hb/u0/w3	000000001010000	000000	00001010	00			0000000	01101	10000000	000001	<u> 100000000</u>	01001	20000000	0101000			
⊕	000000000010100	000000	00000010	10			0000000	000011	0000000	000000	<u> 100000000</u>	000010	20000000	000010100			
⊕	0000011001000000	000000	11001000	00			00001000	000100	0000000	010100	0000010	10100	00000111	0100000			
⊕- ♦ /hb/u0/w6	0000011010010000	000000	11010010	00			(0000100)	10001	20000000	010101	0000010	111101	200000110	1001000			
A				-													
		6	00	8	00	1	us	12	200	10	100	1	500	18	300	2	us

Figure 17: Simulation Result Of Half-Band Filter Using MSD Representation

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Figure 18: Simulation Result Of Decimation Filter For Standard I



Figure 19: Simulation Result Of Decimation Filter For Standard II

7. CONCLUSION

Both the decimation filter architectures use the same CIC filter (Comb) network. Simulation results reveals that the total gate count of the decimation filter with MAC unit (two stage decimator) and Cascaded Multistage Decimation Chain architectures are 17624 and 4279. Further reduction in gate count can be achieved by using CSD and MSD representations for half band filter

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coefficients and it is identified to be 3986 and 3172 respectively. The power dissipation of the two stage decimator and the Multistage Cascaded Chain architectures are found to be 1278 mW and 57.45mW respectively. Using CSD and MSD representation for half band filters show considerable reduction in power dissipation of Cascaded Multistage Decimation Chain architecture and it is found to be 50.11mW and 42.77 mW respectively. Future work focuses on implementation of architectures using poly-phase digital filters and hybrid filter structure capable of supporting multi-standard applications.

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