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EFFECTIVENESS OF SHEPWM TECHNIQUE FOR PARALLEL CURRENT SOURCE INVERTERS USING ARTIFICIAL BEE COLONY ALGORITHM

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ABSTRACT

Now a days multilevel inverters are gaining popularity due to reduced voltage stress and low Total Harmonic Distortion (THD) output voltage waveform. This paper proposes a new concept of H-bridge based parallel current source inverter (CSI), used for grid application. In this paper five, seven and nine level inverter response/waveforms are analysed for sinusoidal pulse width modulation (SPWM) and Selective Harmonic Elimination (SHE). Effectiveness of Proposed SHE PWM technique using optimal switching angles found using bee colony algorithm for current source inverters are verified using MATLAB/Simulink software.

Keywords: *Parallel current source inverter, SHEPWM, SPWM, Total Harmonic Distortion.*

1. INTRODUCTION

Despite of that Voltage Source inverters (VSI) topology are widely used in industries, current source inverters are find its applications particularly when fast dynamic performance is not needed such as domestic fans, pumps, etc [1]. Current source inverter topologies are similar as compared as voltage source inverters, with lower switch count and more reliable over current and short circuit protection [2]. Current source inverters with pulse width modulation strategies are applied to have an acceptable input and output waveforms. Current source inverter has a great harmonics performance using selective harmonic elimination switching modulation and acceptable dynamic performance. Industry demand for higher power range and best performance provide vast field for new type of converters, which are different from conventional one [3].

In this paper a selective harmonic elimination (SHE) and SPWM schemes are introduced for 5, 7 and 9 level parallel current source inverters. To increase the power rating of a current source inverter two are more current source inverters can operate in a parallel manner [4, 5].

2. CURRENT SOURCE INVERTER (CSI)

The main aim of static power converters are to produce an ac output current from a dc current power supply. For sinusoidal ac outputs, its ac magnitude, frequency and phase should be controllable. Figures 1, 2 and 3 show the configure-ations of 5, 7 and 9 level parallel current source inverters respectively. In parallel operations of two or more inverters may cause unbalanced DC currents. The main causes for the unbalanced operation include a) Unequal voltages of the semiconductor devices affects DC current balance in steady state. b) Variations in the delay of the gating signals of the two inverters which affects both transient and steady-state current balance and c) Manufacturing tolerance in dc choke parameters.

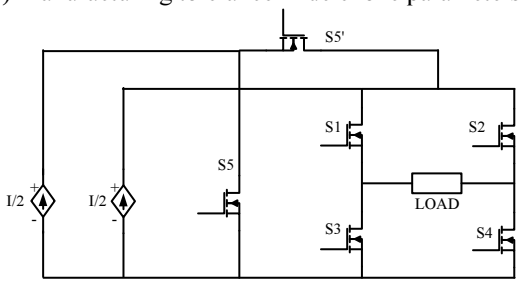

Figure 1: Five level parallel CSI

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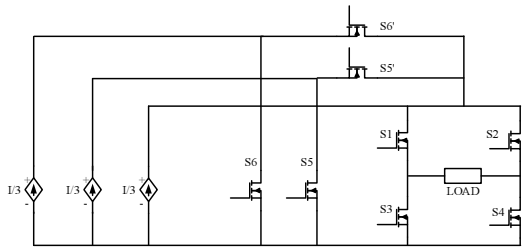

Figure 2: Seven level parallel CSI

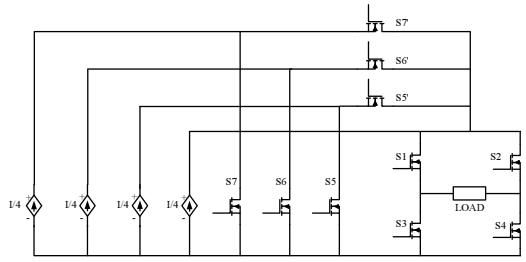

Figure 3: Nine level parallel CSI

As discussed ac magnitude is controlled by varying modulation index and S_1, S_4 and S_2, S_3 switches used to control the frequency as well as phase of the ac supply.

3. SELECTIVE HARMONIC ELIMINATION

In order to achieve a wide range of modulation indexes with minimized Total Harmonic Distortion (THD) for the synthesized waveforms, a generalized selective harmonic modulation method [6, 7] was proposed the Selective Harmonic Elimination (SHE) is considered as an optimum modulation scheme, which provides a superior harmonic profile with a low switching frequency. Unlike the SHE modulation schemes for current source inverters where the modulation index is usually fixed to its maximum value, the SHE scheme should provide an adjustable modulation index for dc current control in addition to the harmonic elimination [8, 9]. Figure 4 shows a typical half-cycle waveform of the PWM current i_w.

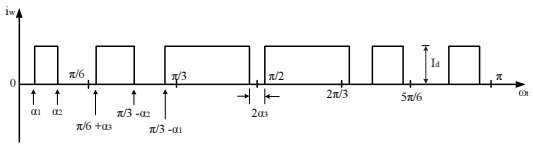

Figure 4: PWM current waveform (half-cycle) with three independent switching angles

The angles α_1, α_2, and α_3 can be used to eliminate harmonics and in the meanwhile provide an adjustable modulation index. The objective of the selective harmonics PWM is to eliminate the lower order harmonics, while remaining higher order harmonics are removed with the use of passive filter. In this paper, 5, 7 and 9 level parallel current source inverters are chosen as a case study to eliminate its lower order harmonics such as 3rd, 5th, 7th, 9th, 11th and 13th order harmonics using sinusoidal pulse width modulation and Selective Harmonic Elimination Pulse width Modulation techniques.

The PWM current waveform in Figure 4 can be expressed in Fourier series as

$$i_w(\omega t) = \sum_{n-1}^{\infty} a_n \sin(n\omega t) \quad (1)$$

Where,

$$a_n = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} i_w(\omega t)\sin(n\omega t)d(n\omega t) \quad (2)$$

$$= \frac{4I_d}{n\pi}\left\{\begin{array}{l}\cos(n\alpha_1)-\cos(n\alpha_2)\\ +\cos\left(n\left(\frac{\pi}{6}+\alpha_0\right)\right)\\ -\cos\left(n\left(\frac{\pi}{3}-\alpha_2\right)\right)\\ +\cos\left(n\left(\frac{\pi}{3}-\alpha_1\right)\right)\\ -\cos\left(n\left(\frac{\pi}{2}-\alpha_0\right)\right)\end{array}\right\} \quad (3)$$

To eliminate two dominant harmonics such as the 5th and 7th, we have

$$F_1 = \cos(5\alpha_1)-\cos(5\alpha_2)+\cos\left(5\left(\frac{\pi}{6}+\alpha_0\right)\right) - \cos\left(5\left(\frac{\pi}{3}-\alpha_2\right)\right)+\cos\left(5\left(\frac{\pi}{3}-\alpha_1\right)\right) - \cos\left(5\left(\frac{\pi}{2}-\alpha_0\right)\right)=0 \quad (4)$$

$$F_2 = \cos(7\alpha_1)-\cos(7\alpha_2)+\cos\left(7\left(\frac{\pi}{6}+\alpha_0\right)\right) - \cos\left(7\left(\frac{\pi}{3}-\alpha_2\right)\right)+\cos\left(7\left(\frac{\pi}{3}-\alpha_1\right)\right) - \cos\left(7\left(\frac{\pi}{2}-\alpha_0\right)\right)=0 \quad (5)$$

The following equation derived for modulation index adjustment

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$$F_3 = \frac{a_1}{I_d} - m_a = \frac{4}{\pi}\left\{\begin{array}{l}\cos\alpha_1 - \cos\alpha_2 \\ +\cos\left(\frac{\pi}{6}+\alpha_0\right) \\ -\cos\left(\frac{\pi}{3}-\alpha_2\right) \\ +\cos\left(\frac{\pi}{3}-\alpha_1\right) \\ -\cos\left(\frac{\pi}{2}-\alpha_0\right)\end{array}\right\} - m_a = 0 \quad (6)$$

Where ma is amplitude modulation index, given by

$$m_a = \frac{\hat{I}_{w1}}{I_d} \quad (7)$$

4. BEE COLONY ALGORITHM

The Bee algorithm is an optimization algorithm based on the natural foraging behavior of honeybees to find the optimal solution [10, 11]. A bee colony consists of three kinds of bees: employed bees, on-looker bees, and scout bees. Employed bees carry information about place and amount of nectar in a particular food source. They transfer the information to on-looker bees with dance in the hive. The time of dance determines the amount of nectar in a food source. An on-looker chooses a food source based on the amount of nectar in a food source. A good food source attracts more on-looker bees to itself. Scout bees seek in search space and find new food sources. Scout bees control the exploring process, while employed and on-looker bees play an exploiting role.

In this algorithm, food sources are considered as possible solutions to a problem. The food source is a D-dimensional vector, where D is the number of optimization variables. The amount of nectar in a food source determines the value of fitness. The basic flowchart of BA is shown in Figure 4. In step 1, random initial food sources are generated. The number of initial food sources is half of the bee colony. In step 2, employed bees are sent to the food sources to determine the amount of nectar and calculate its fitness. For each food source, there is only one employed bee. So, the number of food sources is equal to the number of employed bees. In addition, the employed bees modify the solutions, saved in memory, by searching in the neighborhood of its food source.

The employed bees save the new solution if its fitness is better than the older one. Employed bees go back to the hive and share the solutions with the onlooker bees. In step 3, on-looker bees, which are another half of the colony, select the best food sources using a probability-based selection process. Food sources with more nectar attract more on-looker bees. On-looker bees are sent to the selected food sources. The on-looker bees improve the chosen solutions and calculate its fitness. Similar to employed bees, the on-looker bees save a new solution if its fitness is better than an older solution. In step 4, the food sources that are not improved for a number of iterations are abandoned. So, the employed bee is sent to find new food sources as a scout bee. The abandoned food source is replaced by the new food source. Finally, in step 5, the best food source is memorized. The maximum number of iterations is set as a termination criterion which is checked at the end of iteration. If it is not met, the algorithm returns to step 2 for the next iteration.

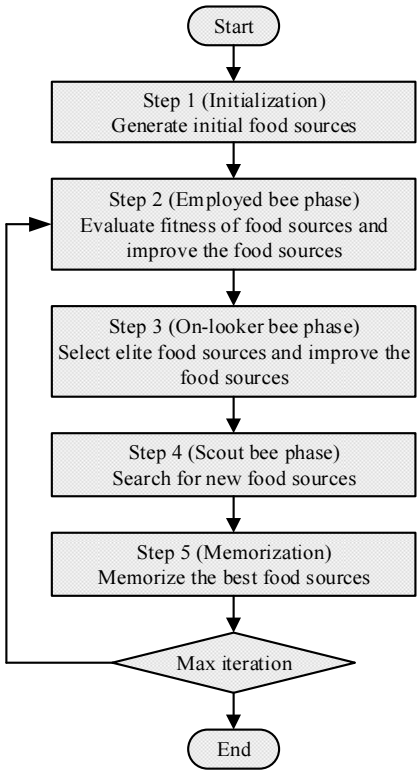

Figure 4: Basic flowchart of Bee Colony Algorithm

4.1 Bee Colony Algorithm Implementation

For achieving switching angle, the Bee Colony algorithm is written using MATLAB software. The size of population is 40. In addition, the number of iterations for each run is 80 is assumed as termination criterion. Fitness function used in proposed algorithm is given below,

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$$f = \min_{\theta i}\left\{\left(100\frac{I_1^* - I_1}{I_1^*}\right)^4 + \sum_{s=2}^{S}\frac{1}{h_s}\left(50\frac{I_{hs}}{I_1}\right)^2\right\} \quad (8)$$

Where

$$i=1, 2,\ldots, S \text{ and } 0 \le \theta_i \le \frac{\pi}{2}$$

Here I_1^* is the desired fundamental harmonic, S is the number of switching angles, and h_s is the order of s^{th} viable harmonic at the output of proposed parallel multilevel inverter, e.g., h_2=5 and h_3=7. In this sections, switching angles are found such that low-order harmonics (3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th} and 13^{th}) are eliminated and the magnitude of the fundamental harmonic reaches to its desirable value (I_1^*). If the fundamental harmonic violates its set point by more than 1%, the first term of the fitness function fines it by a power of 4. Because of the use of the power of 4, corresponding penalties for any deviations under 1% get a negligible value. The second term of fitness function neglects harmonics under 2% of fundamental. But, when any harmonic exceeds this limit, the objective function is subject to a penalty by power of 2. Finally, each harmonic ratio is weighted by inverse of its harmonic order, i.e., 1/hs. By this weighting method, reducing the low-order harmonics gets higher importance. The algorithm is run 1, 2, 5, and 10 times and the best solution based on the minimum fitness function is selected.

5. SIMULATION RESULTS

Simulation has been carried out for 5, 7 and 9 level parallel H-bridge current source inverters. The bee colony algorithm is proposed to found the switching angles (α_1, $\alpha 2$,….α_n) using equation (8); which is shown in table 1. Figure 5 show the schematic representation of proposed inverter using SHEPWM. Figures 6-35 show the simulated responses of 5, 7 and 9 level parallel CSI with sinusoidal PWM and Bee colony algorithm implemented Selective Harmonic Elimination PWM using MATLAB/ Simulink software. Figures 6 and 7 show the output voltage and current of 5 level parallel current source inverter using sinusoidal PWM. Figure 8 shows the FFT analysis of 5 level parallel current source inverter using sinusoidal PWM. From Figure 8 it is observed that the 5^{th} and 7^{th} order harmonics are eliminated. Figure 9 shows the switching sequence of 5 level parallel current source inverter using sinusoidal PWM. Figures 10 and 11 show the output voltage and current of 5 level parallel current source inverter using SHEPWM. Figure 12 shows the FFT analysis of 5 level parallel current source inverter using SHEPWM. From Figure 12 it is observed that the lower order harmonics 3^{rd}, 5^{th} and 9^{th} are fully eliminated. Figure 13 shows the switching sequence of 5 level parallel current source inverter using SHEPWM.

Figures 14 and 15 show the output voltage and current of 7 level parallel current source inverter using sinusoidal PWM. Figure 16 shows the FFT analysis of 7 level parallel current source inverter using sinusoidal PWM. From Figure 16 it is observed that the 3^{rd} harmonic is totally eliminated. Figure 17 shows the switching sequence of 7 level parallel current source inverter using sinusoidal PWM. Figures 18 and 19 show the output voltage and current of 7 level parallel current source inverter using SHEPWM. Figure 20 shows the FFT analysis of 7 level parallel current source inverter using SHEPWM. From Figure 20 it is observed that the 3^{rd}, 5^{th} and 7^{th} order harmonics are totally eliminated. Figure 21 shows the switching sequence of 7 level parallel current source inverter using SHEPWM.

Figures 22 and 23 show the output voltage and current of 9 level parallel current source inverter using sinusoidal PWM. Figure 24 shows the FFT analysis of 9 level parallel current source inverter using sinusoidal PWM. From Figure 24 it is observed that all lower order harmonics are eliminated and 9^{th} order presented. Figure 25 shows the switching sequence of 9 level parallel current source inverter using sinusoidal PWM. Figures 26 and 27 show the output voltage and current of 9 level parallel current source inverter using SHEPWM. Figure 28 shows the FFT analysis of 9 level parallel current source inverter using SHEPWM. From Figure 28 it is observed that all lower order harmonics are fully eliminated and produce the best THD compare with all. Figure 29 shows the switching sequence of 9 level parallel current source inverter using SHEPWM.

Figure 30 shows the fitness function with respect to the range of modulation index for 5 level CSI. Figure 31 shows the situation of optimum switching angles versus MI of 5 level CSI. Figure 32 shows the fitness function with respect to the range of modulation index for 7 level CSI. Figure 33 shows the situation of optimum switching angles versus MI of 5 level CSI. Figure 34 shows fitness function with respect to the range of modulation index for 9 level CSI. Figure 35 shows the situation of optimum switching angles versus MI of 9 level CSI.

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5.1 Simulated Results of 5 Level Parallel CSI using Sinusoidal PWM

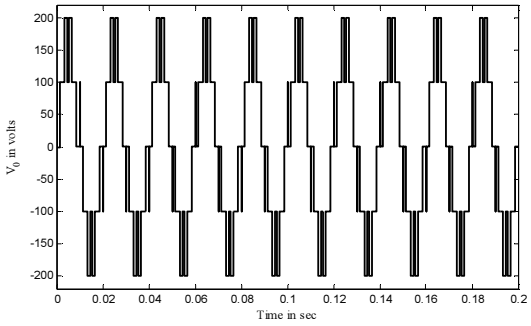

Figure 6: Output voltage of 5 level CSI with SPWM

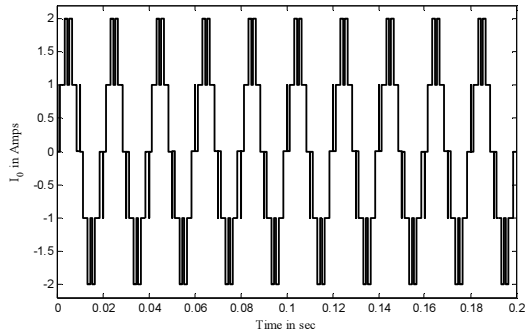

Figure 7: Current response of 5 level CSI with SPWM

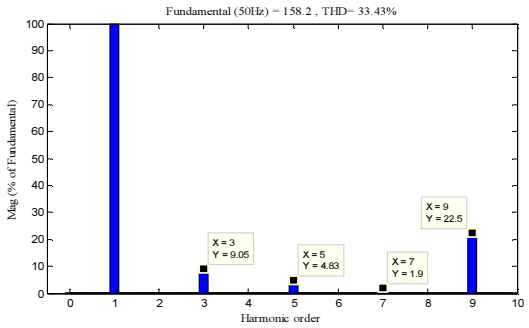

Figure 8: FFT analysis of 5 level CSI with SPWM

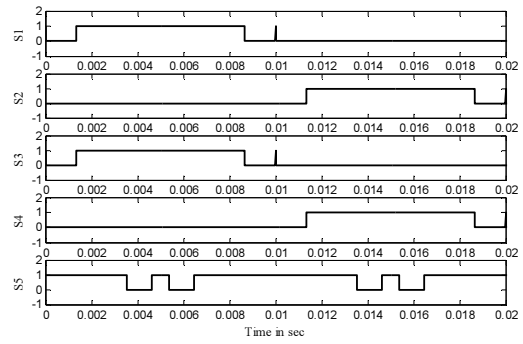

Figure 9: Switching sequence of 5 level CSI with SPWM

5.2 Simulated Results of 5 Level Parallel CSI using SHE PWM

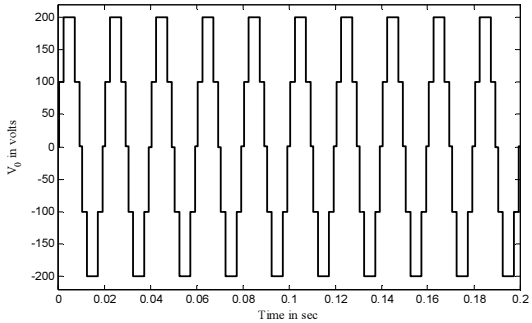

Figure 10: Output voltage of 5 level CSI with SHEPWM

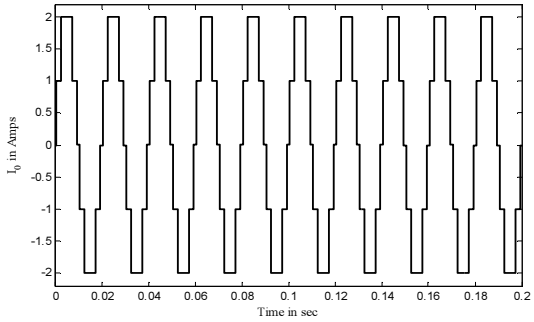

Figure11: Current response of 5 level CSI with SHEPWM

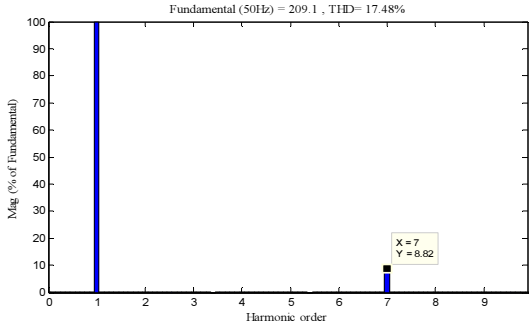

Figure 12: FFT analysis of 5 level CSI with SHEPWM

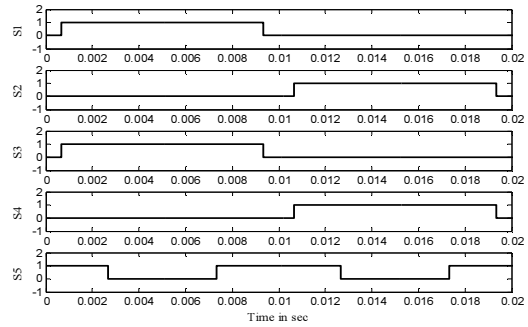

Figure 13: Switching sequence of 5 level CSI with SHEPWM

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5.3 Simulated Results of 7 Level Parallel CSI using Sinusoidal PWM

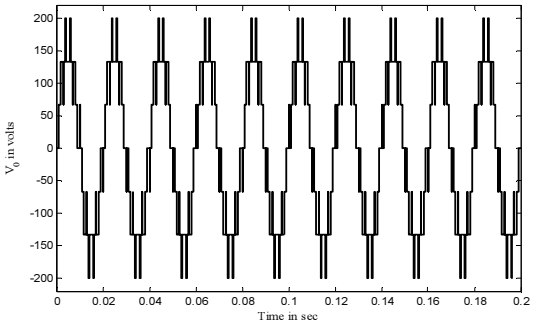

Figure 14: Output voltage of 7 level CSI with SPWM

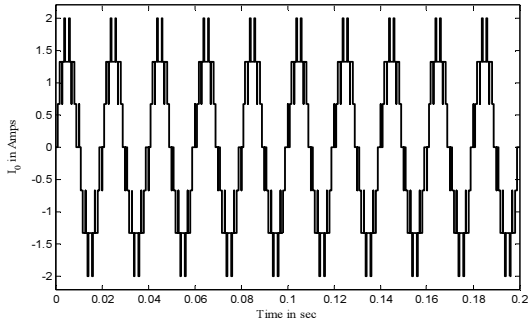

Figure 15: Current response of 7 level CSI with SPWM

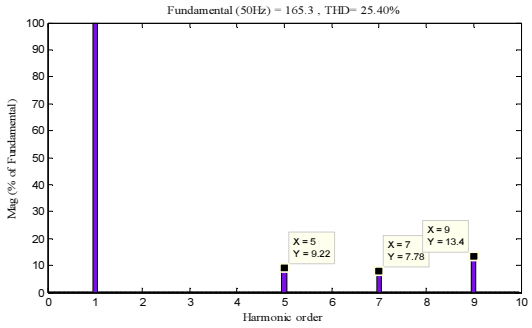

Figure 16: FFT analysis of 7 level CSI with SPWM

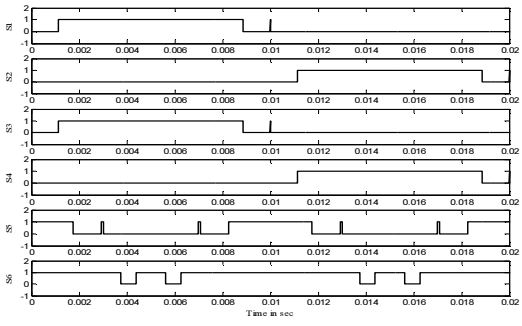

Figure 17: Switching sequence of 7 level CSI with SPWM

5.4 Simulated Results of 7 Level Parallel CSI using SHE PWM

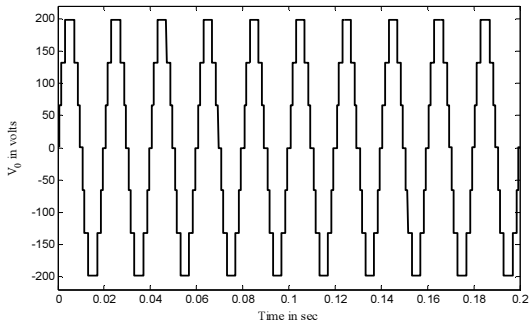

Figure 18: Output voltage of 7 level CSI with SHEPWM

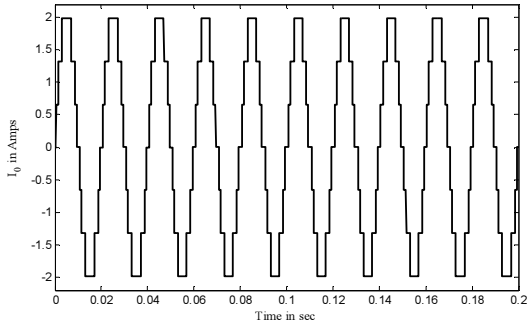

Figure19: Current response of 7 level CSI with SHEPWM

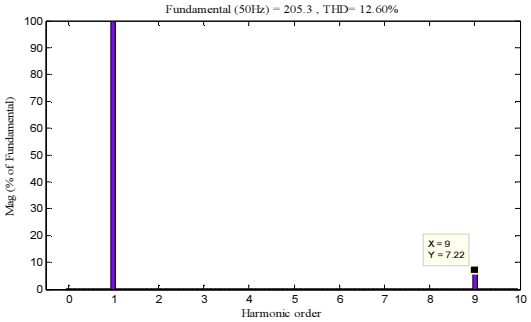

Figure 20: FFT analysis of 7 level CSI with SHEPWM

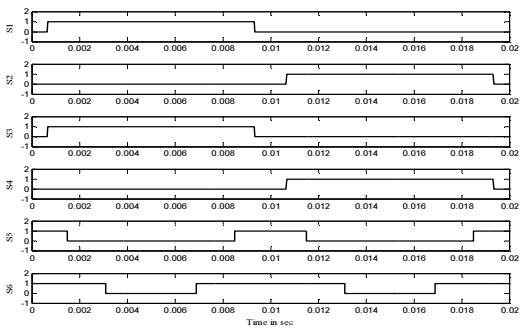

Figure 21: Switching sequence of 7 level CSI with SHEPWM

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5.5 Simulated Results of 9 Level Parallel CSI using Sinusoidal PWM

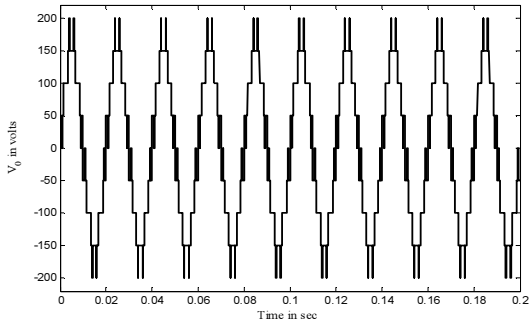

Figure 22: Output voltage of 9 level CSI with SPWM

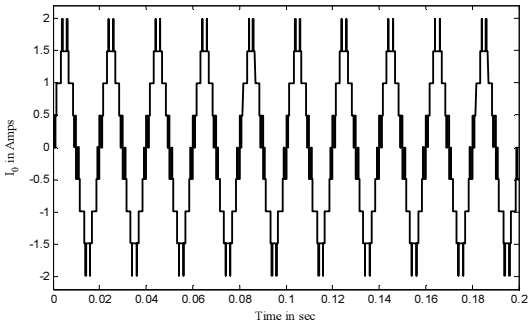

Figure 23: Current response of 9 level CSI with SPWM

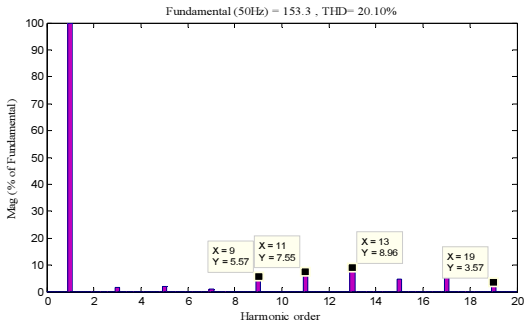

Figure 24: FFT analysis of 9 level CSI with SPWM

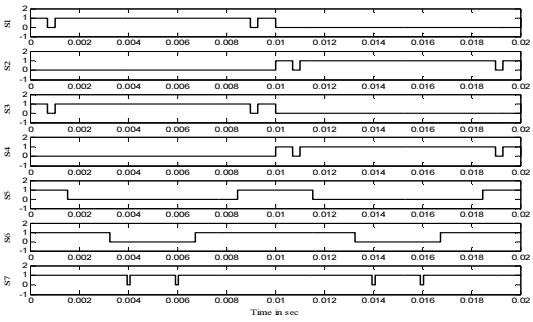

Figure 25: Switching sequence of 9 level CSI with SPWM

5.6 Simulated Results of 9 Level Parallel CSI using SHE PWM

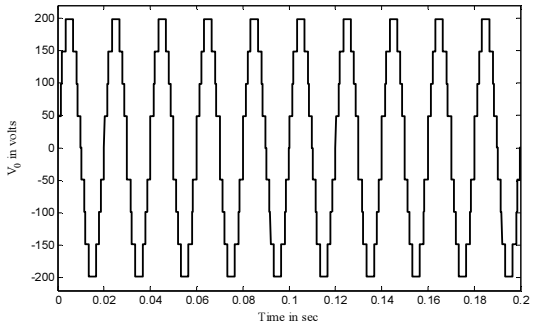

Figure 26: Output voltage of 9 level CSI with SHEPWM

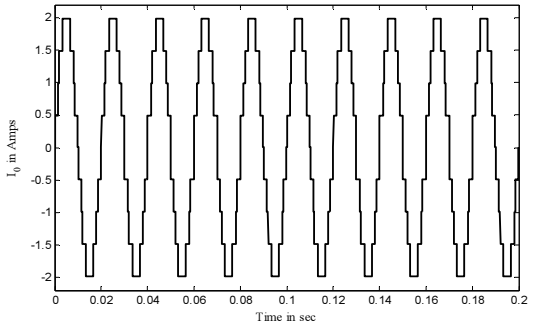

Figure 27: Current response of 9 level CSI with SHEPWM

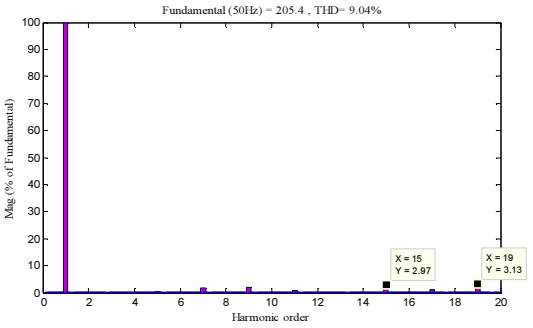

Figure 28: FFT analysis of 9 level CSI with SHEPWM

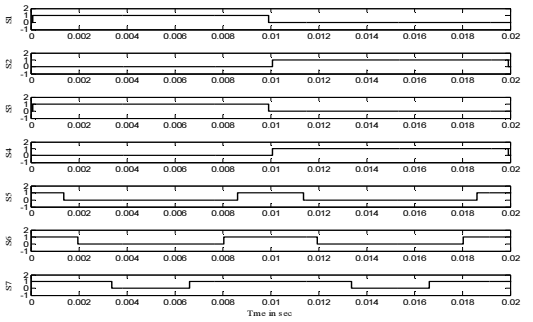

Figure 29: Switching sequence of 9 level CSI with SHEPWM

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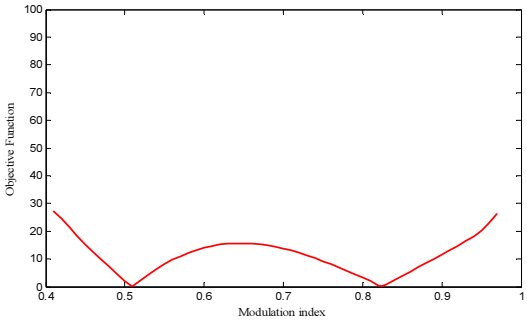

Figure 30: Optimum objective function versus MI of 5 level parallel CSI with SHEPWM

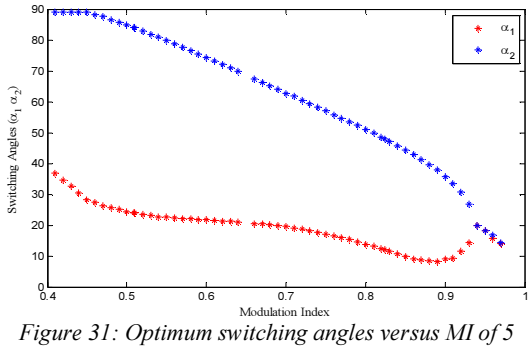

Figure 31: Optimum switching angles versus MI of 5 level parallel CSI with SHEPWM

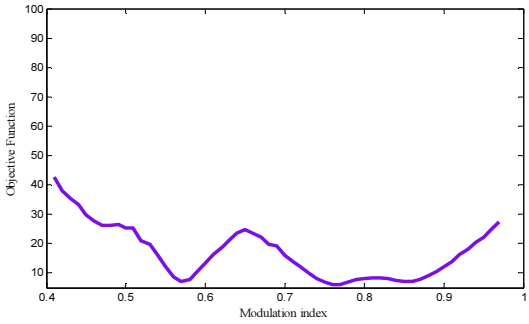

Figure 32: Optimum objective function versus MI of 7 level parallel CSI with SHEPWM

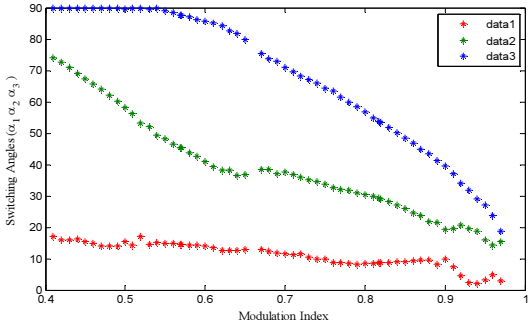

Figure 33: Optimum switching angles versus MI of 7 level parallel CSI with SHEPWM

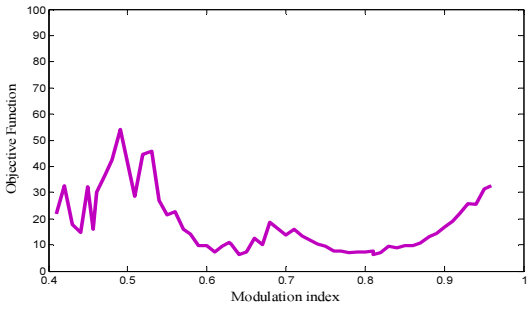

Figure 34: Optimum objective function versus MI of 9 level parallel CSI with SHEPWM

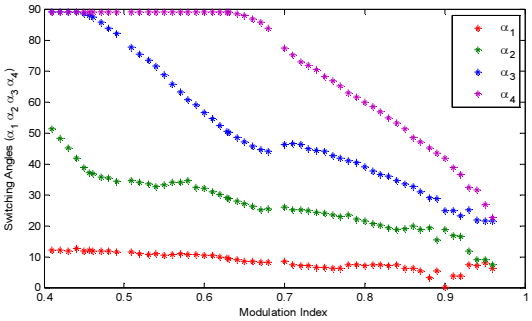

Figure 35: Optimum switching angles versus MI of 9 level parallel CSI with SHEPWM

Table: 1 Optimum switching angles

MI	Obj fun	α_1	α_2	α_3	α_4
0.700	8.126	8.400	26.055	46.277	77.222
0.710	7.558	7.329	25.098	46.658	75.216
0.720	7.007	7.123	25.044	46.363	73.045
0.730	6.594	6.991	24.789	44.904	71.881
0.740	6.300	6.501	24.281	44.196	70.308
0.750	6.012	6.540	23.996	44.004	68.060
0.760	5.622	6.361	23.419	42.648	66.872
0.770	5.099	6.316	22.894	41.903	65.205
0.780	4.370	7.302	23.340	40.982	62.945
0.790	3.646	7.251	22.164	40.280	61.432
0.800	3.031	7.163	21.603	39.053	59.979
0.810	2.776	7.287	20.831	37.715	58.511
0.810	2.777	7.302	20.782	37.757	58.460
0.820	3.067	7.249	20.178	36.582	56.857
0.830	3.737	6.992	19.379	35.929	54.946
0.840	4.595	7.232	18.828	34.563	53.245
0.850	5.515	6.337	18.962	33.570	51.146
0.860	6.657	6.307	19.886	32.691	48.384
0.870	7.707	5.461	18.865	30.914	47.127
0.881	9.198	3.078	19.259	28.928	45.187
0.890	10.544	5.503	15.417	28.872	43.528
0.900	11.950	0.240	18.701	24.779	41.846
0.910	13.586	3.707	16.800	24.905	38.866
0.920	15.336	3.806	16.588	23.206	36.412
0.930	17.246	7.334	11.933	25.130	32.380
0.940	19.330	6.964	9.136	21.716	31.649
0.950	21.631	8.034	9.146	21.523	26.828
0.960	24.122	6.211	7.394	21.406	22.602

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6. CONCLUSION

This work proposed a new topology of 5, 7 and 9 level parallel H-bridge current source inverters. The bee colony algorithm is proposed to found the switching angles of SHEPWM. Voltage, current and FFT analysis has been analysed using SPWM and SHEPWM. Figures 8, 12, 16, 20, 24 and 28 show the FFT analysis of proposed current source inverters it is observed that the SHEPWM eliminated the lower order harmonics and proved the effectiveness compared with traditional sinusoidal PWM.

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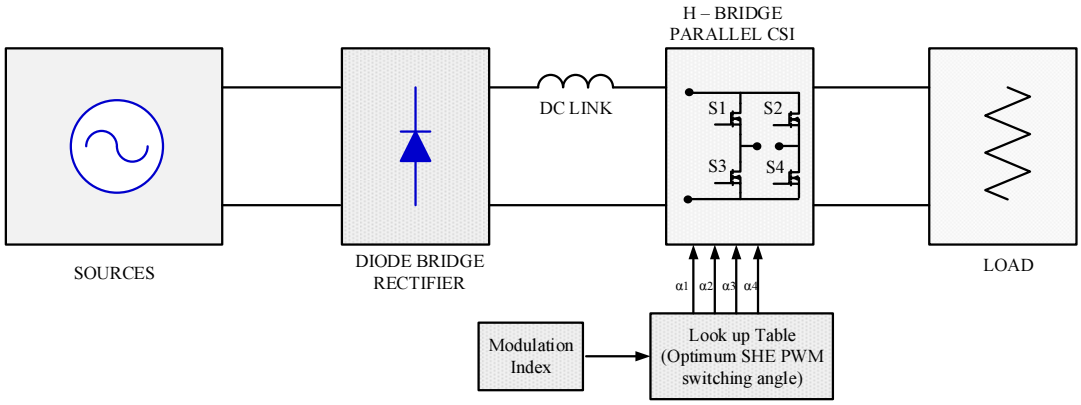

Figure 1: Schematic representation of parallel CSI with SHEPWM