

ANALYSIS AND SIMULATION OF CASCADED FIVE AND SEVEN LEVEL INVERTER FED INDUCTION MOTOR

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ABSTRACT

This paper presents the performance analysis of cascaded multilevel inverter fed induction motor drive. It deals with the study and analysis of five-level and seven-level inverters for three phase induction motor drive. Both five-level and seven-levels are realized by cascading the two H-bridge inverters. To minimize the harmonic distortion in the output waveform without decreasing the inverter power output a sinusoidal modulation technique is employed. A model for multilevel inverter fed induction motor is developed and simulated using PSIM package under steady state and transient condition to prove their merits.

Keywords: *Cascaded H-Bridge Multilevel Inverter, Total Harmonic Distortion (THD) And Induction Motor.*

1. INTRODUCTION

Multilevel Inverters [MLI] are used in adjustable speed drives [1], [2], static VAR compensator,[3],[4] and renewable energy systems [5]. A two level voltage source inverter (VSI) operates at low dc output voltage whereas the MLI operates at high dc voltage [6] using series connected switches. The MLI inverters are classified into three categories [7] as Diode clamped MLI, Flying Capacitor MLI and Cascaded MLI. Among the three, the cascaded MLI are the most preferred adjustable speed drive system. Further the pulse generations for the cascaded MLI are divided into two categories [8]: one with high switching frequency and the other for low switching frequency. High switching frequency employs carrier based sinusoidal pulse width modulation (PWM) and the low switching frequency employs fundamental component frequency to produce stair case output voltage which is most commonly used.

A multicarrier sinusoidal PWM is used to control the output voltage of the inverter. The five and seven level inverter output voltage contains harmonics which can be minimized by supplying non integer dc source voltage [9] or by using unequal dc source voltage. The switching angles of the MLI are calculated to minimize the total harmonic distortion. In three phase system the THD minimization algorithm [10] is applied to line and phase voltages where the switching angles are

calculated [11] to optimize the THD. In adjustable speed drive system the THD is further minimized by a frequency-weighted THD (WTHD). In H-Bridge diode clamped multi inverter THD and WTHD are minimized by varying [12] the switching frequency. A new topology [13] has been proposed to operate the motor in linear and over modulation region by varying the modulation index. In order to reduce the number of switches a new three phase five level inverter topology [14] has been designed to operate the inverter in three level and five level by disconnecting the H-bridge cells and using the flying capacitors. To balance the capacitor voltage a common mode voltage elimination [15] method has been proposed to balance the capacitor voltage at any power factor and modulation index

In this paper the cascaded H-bridge inverter for five and seven level inverter fed induction motor drives are discussed to produce output with low level of harmonics. The pulses are generated based on the multiple carrier signals instead of one carrier wave to eliminate the voltage ripple present in the output voltage. Section II explains the mathematical model of induction motor. Section III discusses the performances of five level and seven level cascaded H-bridge inverter with induction motor drive. Section IV discusses the conclusion of a five and seven level cascade H-bridge inverters fed induction motor drives.

Nomenclature

- v_{qs} = Quadrature axis stator voltage [V]
- v_{ds} = Direct axis stator voltage [V]
- i_{qs} = Quadrature axis stator current [Amps]
- i_{ds} = Direct axis stator current [Amps]
- i_{qr} = Quadrature axis rotor current [Amps]
- i_{dr} = Direct axis rotor current [Amps]
- R_s = Stator resistance [Ω]
- R_r = Rotor resistance [Ω]
- T_e = Electromagnetic torque [N.m]
- T_L = Load torque [N.m]
- L_{ls} = Stator leakage inductance [H]
- L_s = Stator inductance [H]
- L_{lr} = Rotor leakage inductance [H]
- L_r = Rotor inductance [H]
- L_m = Magnetizing inductance [H]
- P = Number of Poles
- J = Moment of Inertia [$\text{Kg}\cdot\text{m}^2$]
- ω_r = Motor speed [rad/sec]

2. MATHEMATICAL MODEL OF INDUCTION MOTOR

The machine equations are derived based on the reference frame fixed to the stator and all the quantities are referred to the stator. The detail of the reference frame is shown in Figure 1.

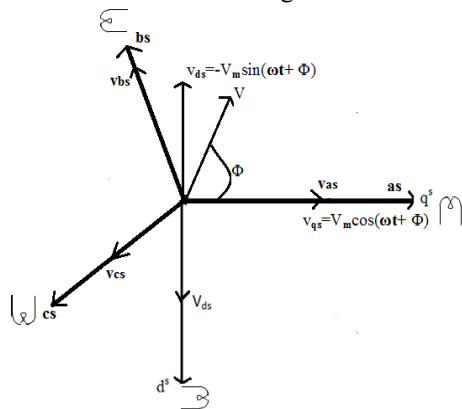


Figure 1. d-q Frame for Induction Motor

The electrical transient model of the squirrel cage induction motor in terms of voltage and current is given in matrix form as

$$\begin{bmatrix} v_{qs} \\ v_{ds} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_s + L_s p & 0 & L_m p & 0 \\ 0 & R_s + L_s p & 0 & L_m p \\ L_m p & -\omega L_m & R_r + L_r p & -\omega L_r \\ \omega L_m & L_m p & \omega L_r & R_r + L_r p \end{bmatrix} \begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{qr} \\ i_{dr} \end{bmatrix} \quad (1)$$

Where $L_s = L_{ls} + L_m$ and $L_r = L_{lr} + L_m$ $p = \frac{d}{dt}$

The expression for the electromagnetic torque T_e is given in equation (2).

$$T_e = T_L + J \frac{d\omega_m}{dt} = T_L + \frac{2}{P} J \frac{d\omega_r}{dt} \dots\dots\dots 2)$$

The expression for electromagnetic torque is expressed in terms of the mutual inductance L_m and the stator and the rotor currents as given in equation (3).

$$T_e = \frac{3}{2} \left(\frac{P}{2} \right) L_m (i_{qs} i_{dr} - i_{ds} i_{qr}) \dots\dots\dots (3)$$

The equations (1) (2) and (3) are used in the development of motor module using PSIM software as shown in Figure 2.

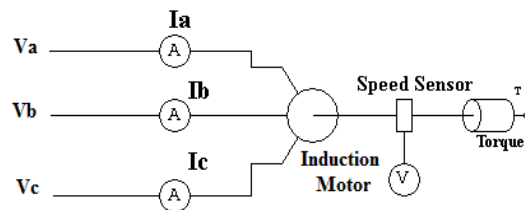


Figure 2 Motor Drive Module

The speed and torque sensors are coupled to the shaft of the induction motor to measure the speed and electromagnetic torque produced by the motor for the given voltage.

3. OPERATION OF CASCADED H BRIDGE MULTILEVEL INVERTER

The dc-ac cascaded H-bridge five and seven level inverters feeding an induction motor is shown in Figures 3 and 4. The cascaded inverter circuits are discussed below.

3.1. Simulation Model of Cascaded Five level Multilevel Inverter Fed Induction Motor

The three phase cascaded five level inverter for an induction motor load is shown in Figure 3 and the switching sequence operation during the

positive and negative half cycle for phase A is shown in Table I and II. Similarly the other two phases B and C conducts with 120° phase shift.

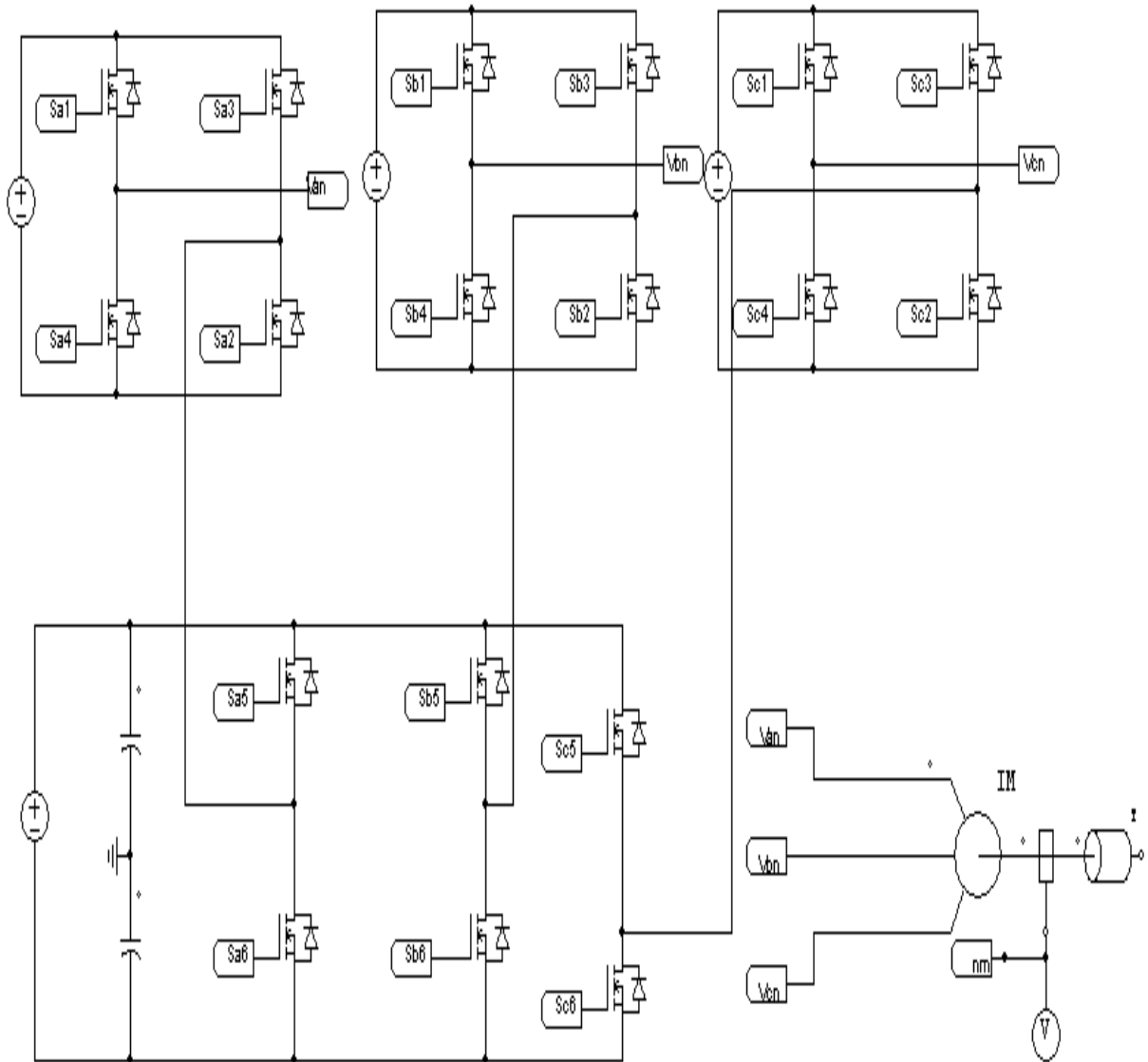


Figure 3 Five Level Cascaded Inverter Fed Induction Motor

Table I: Switching Sequence during Positive Half Cycle of a Five Level Inverter

Switch Number/ Voltage	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Time period
0	1	1	0	0	0	1	0 to t ₁
+V/2	1	1	0	0	1	0	t ₁ to t ₂
+V	1	1	0	0	1	0	t ₂ to t ₃
+V/2	1	1	0	0	1	0	t ₃ to t ₄
0	1	1	0	0	0	1	t ₄ to t ₅

Table II: Switching Sequence during Negative Half Cycle of a Five Level Inverter

Switch Number/ Voltage	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Time period
-V/2	0	0	1	1	0	1	t ₅ to t ₆
-V	0	0	1	1	0	1	t ₆ to t ₇
-V/2	0	0	1	1	0	1	t ₇ to t ₈
0	1	1	0	0	0	1	t ₈ to t ₉

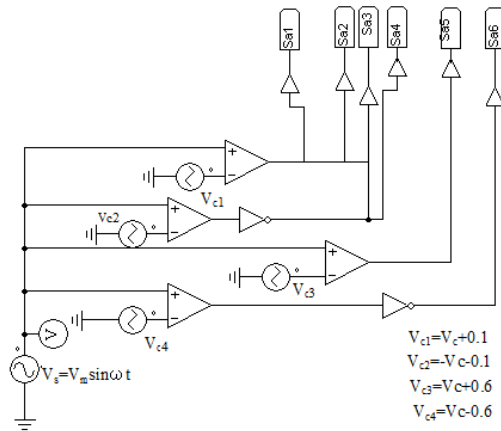


Figure 4. Generation of Firing Pulses for Phase A of Five Level Inverter

The firing pulse generator of phase A for a five level inverter is shown in figure 4. The generation of gating pulse is obtained by comparing the sinusoidal modulating signal, V_s with the triangular carrier signals, V_c as shown in Figure 5. The sinusoidal signal is generated with amplitude of 0.8 volts at a frequency of 50Hz. The carrier wave signals V_{c1} and V_{c2} are generated at a frequency of 3 KHz with a peak value of 0.5 volt and a dc offset of 0.1 volt with 50% duty cycle. The carrier wave signals V_{c3} and V_{c4} are generated at a frequency of 3 KHz with peak value of 0.5 volt and a dc offset of

0.6 volt with 50 % duty cycle. The switching pattern for the phase A is shown in Figures 6 and 7.

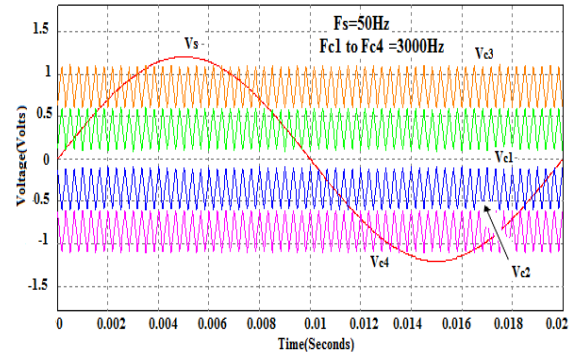
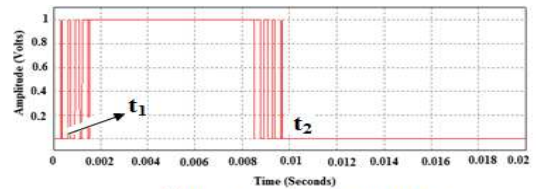
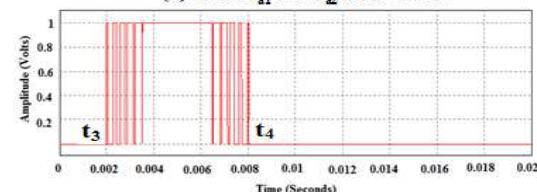


Figure 5 Sinusoidal PWM Signal for Phase A of a Five Level Inverter

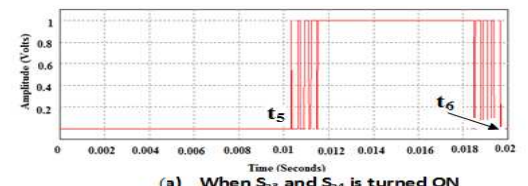


(a) When Sa1 and Sa2 is turned ON

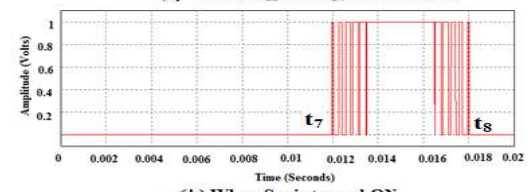


(b) When Sa5 is turned ON

Figure 6 Switching Pulse Waveform During Positive Half Cycle of a Five Level Inverter



(a) When Sa3 and Sa4 is turned ON



(b) When Sa6 is turned ON

Figure 7 Switching Pulse Waveform During Negative Half Cycle of a Five Level Inverter

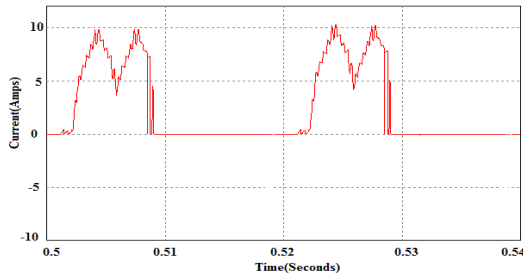


Figure 8. Waveform of Switch current Sa1 for five Level MLI

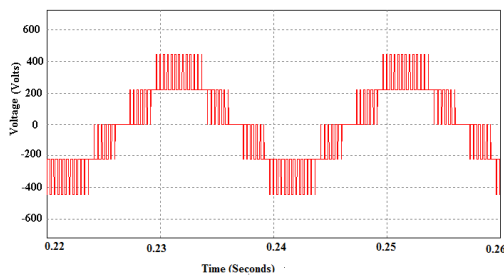


Figure 9. Waveform of Phase A Voltage for a Five Level MLI

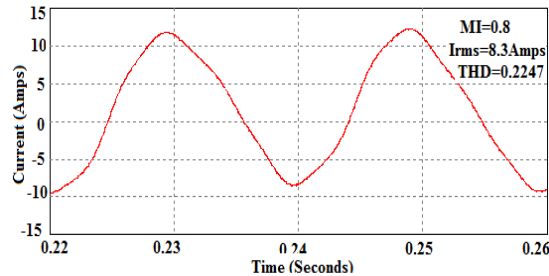


Figure 10. Waveform of Phase A Current for a Five Level Multilevel Inverter

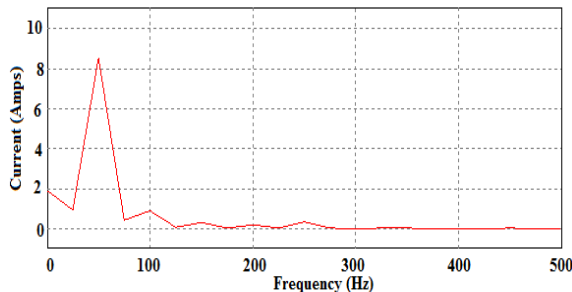


Figure 11. Frequency Spectrum of Phase A Current for a Five Level MLI

The waveforms of switch current and voltage and current for Phase A of the inverter are shown in Figures 8 to 10. Five level output voltage is

obtained by varying the Modulation Index (MI) from 0.8 to 1.2 and a three level output voltage is obtained when MI varies from 0.4 to 0.75. The Fast Fourier Transform (FFT) is applied to measure the harmonics present in the current waveform. The harmonic analysis of phase A current shown in Figure 11 depicts the presence of the fundamental, third, fifth and seventh harmonics.

Table III: Performance a Five Level Cascaded H-Bridge Inverter Fed Induction Motor

Torque (Nm)	Va (Volts)	Ia (Amps)	Speed (Rpm)	Slip %	THD
5	400	4.85	1490	0.66	0.691
10	400	5.3	1478	1.46	0.622
15	400	6.1	1465	2.33	0.527
20	400	7.1	1450	3.33	0.438
25	400	8.3	1435	4.33	0.342

The performance analysis of a five level induction motor drive is shown in Table III, for the load torque from 0 to 25Nm in steps of 5Nm. When the load torque is increased, the slip increases and the corresponding speed decreases from the rated speed of 1500rpm. The Figures 12 and 13 show the speed response when the load torque of 25Nm and full load torque of 15Nm are suddenly applied. The speed is reduced from 1500 rpm to 1435 rpm when full load torque is suddenly applied.

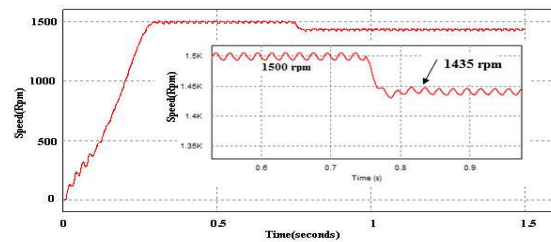


Figure 12. Speed response When Load Torque of 25Nm Applied at 0.75 sec

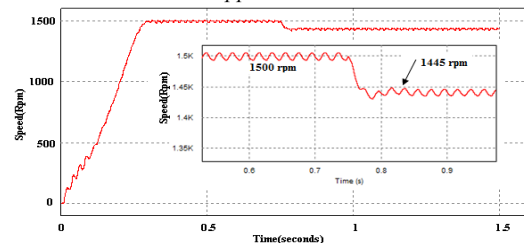


Figure 13. Speed Responses When Load Torque of 15Nm applied at 0.75 sec

3.2. Seven Level Cascaded Multilevel Inverter Fed Induction Motor Model

In this section the performance analysis of a cascaded seven level inverter with induction motor is discussed. The cascaded seven level inverter for

of an induction motor is shown in Figure 14 and the switching sequence operations during positive and negative half cycle are shown in Tables IV and V. Similarly, the other two phases B and C have similar sequences with 120° phase shift.

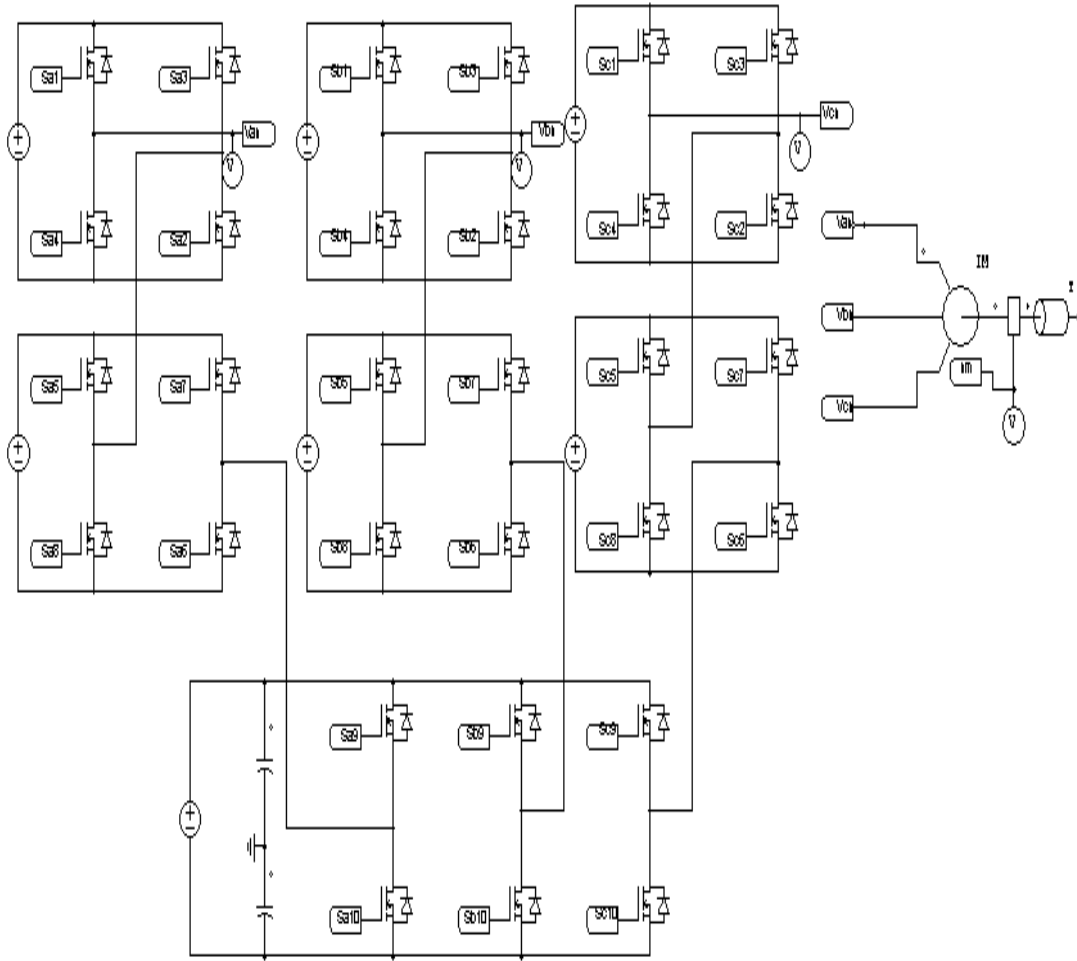


Figure 14. Seven-Level Cascaded H- Bridge Inverter Fed Induction Motor

Cycle of a Seven Level Inverter

Switch Number/ Voltage	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Sa7	Sa8	Sa9	Sa10	Time period
0	1	1	0	0	1	0	1	0	0	1	0 to t ₁
V/2	1	0	1	0	1	0	1	0	1	0	t ₁ to t ₂
+V	1	1	0	0	1	0	1	0	1	0	t ₂ to t ₃
+3V/2	1	1	0	0	1	1	0	0	1	0	t ₃ to t ₄
+V	1	1	0	0	1	0	1	0	1	0	t ₄ to t ₅
V/2	1	0	1	0	1	0	1	0	1	0	t ₅ to t ₆
0	1	1	0	0	1	0	1	0	0	1	t ₆ to t ₇

Table V: Switching Sequence for the Negative Half Cycle of a seven Level Inverter

Switch Number / Voltage	Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Sa7	Sa8	Sa9	Sa10	Time period
-V/2	1	0	1	0	1	0	1	0	0	1	t ₇ to t ₈
-V	0	0	1	1	1	0	1	0	0	1	t ₈ to t ₉
-3V/2	0	0	1	1	0	0	1	1	0	1	t ₉ to t ₁₀
-V	0	0	1	1	1	0	1	0	0	1	t ₁₀ to t ₁₁
-V/2	1	0	1	0	1	0	1	0	0	1	t ₁₁ to t ₁₂

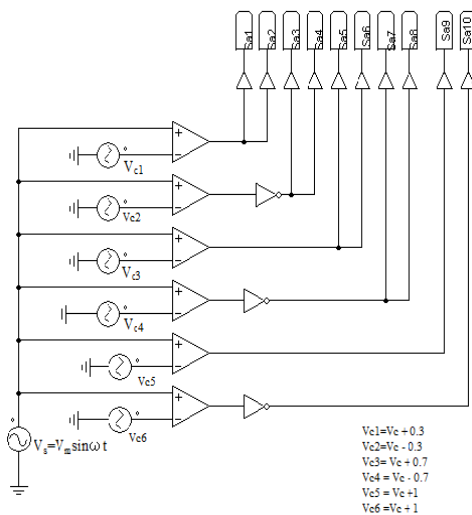


Figure 15 Generation of Firing Pulse of a Seven Level Inverter

The firing pulse generator for a seven level inverter is shown in figure 15. The sinusoidal signal

Table IV: Switching Sequence for the Positive Half is generated with amplitude of 0.8 volt at a frequency of 50Hz. The carrier wave signals V_{c1} and V_{c2} are generated at a frequency of 4 KHz with a peak value of 0.25 volt and a dc offset of 0.3 volt for 50% duty cycle. The carrier wave signal V_{c3} and V_{c4} are generated with a frequency of 2 KHz with peak value of 0.25 volt and a dc offset of 0.7 volts for 50% duty cycle. The carrier wave signal V_{c5} and V_{c6} are generated with a frequency of 4 KHz with peak value of 0.25 volt and a dc offset of 1 volt for 50% duty cycle as shown in Figure 16. The positive and negative half cycle switching pulse pattern for a seven level inverter is shown in Figures 17 and 18.

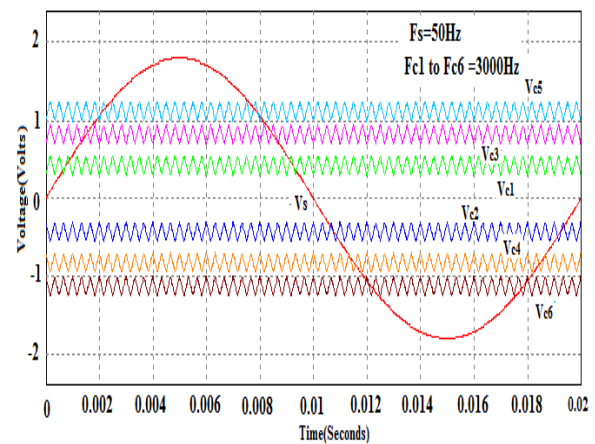


Figure 16. Sinusoidal PWM Signal for Phase A of Seven Level Inverter

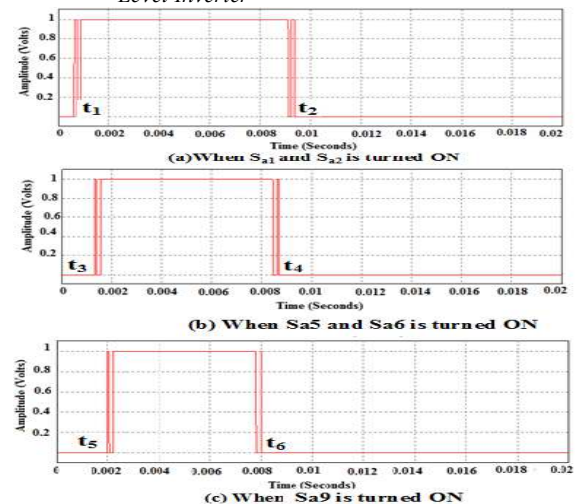


Figure 17 Switching Pulse Waveform During Positive Half Cycle of Seven level Inverter

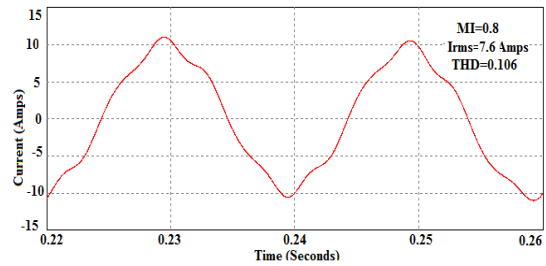
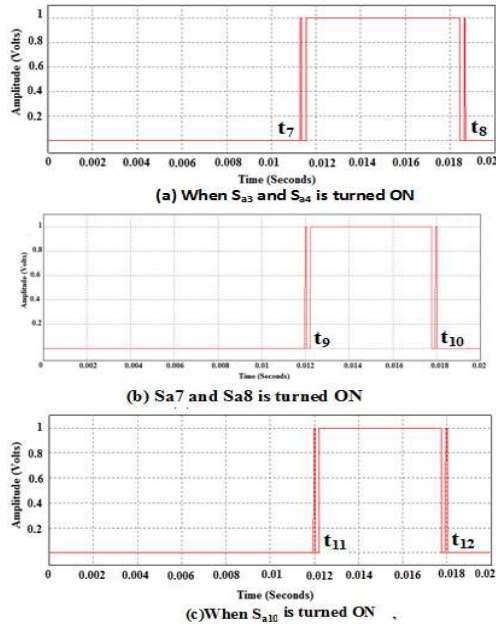


Figure 20 Waveform of Phase A Current for a Seven Level Multilevel Inverter

The responses of phase A's voltage and current for a seven level cascade H-bridge inverter are shown in Figures 19 and 20. Seven level output voltage is obtained by varying the Modulation Index (MI) from 0.8 to 1.2 and a five level output voltage is obtained when MI is varied from 0.4 to 0.75. The harmonic analysis of Phase A current shown in Figure 21 explains the presence of the fundamental and fifth harmonics.

Table VI: Performance of Seven Level Cascaded H-Bridge Inverter Fed Induction Motor

Torque (Nm)	Va (Volts)	Ia (Amps)	Speed (Rpm)	Slip (%)	THD
5	400	3.9	1492	0.53	0.038
10	400	4.6	1480	1.33	0.034
15	400	5.4	1468	2.13	0.029
20	400	6.4	1457	2.67	0.024
25	400	7.6	1445	3.67	0.02

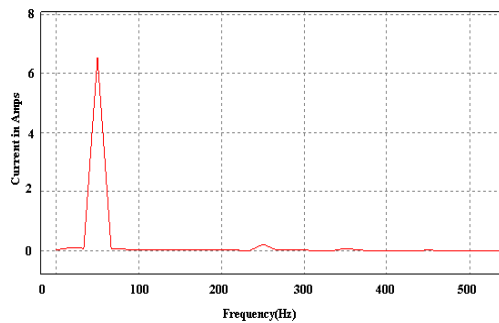


Figure 21. Frequency Spectrum for Phase A Current for a Seven Level Multilevel Inverter

Figure 18. Switching Pulse Waveform During Negative Half Cycle of Seven Level Inverter

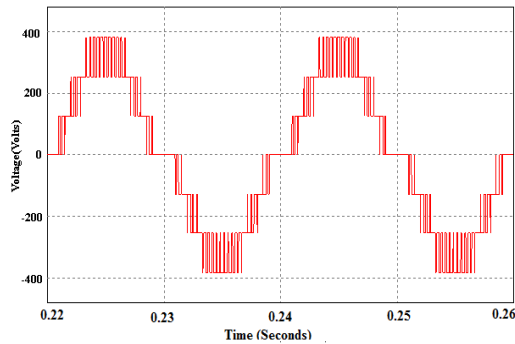


Figure 19 Phase A Voltage Waveform for a Seven Level Multilevel inverter

The performance analysis of seven-level cascaded H-bridge inverter fed induction motor is shown in Table VI. The slip increases when the load torque is increased from no-load to full load and correspondingly the speed decreases. The Figures 22 and 23 show the speed response of an induction motor drive when load torque of 15Nm and 25Nm are applied at .75 seconds. The speed is reduced from 1500 rpm to 1435 rpm when full load torque of 25Nm is applied. The Figure 24 shows the speed response at full load torque when the supply voltage is increased at 2 seconds. The speed reaches steady state at 2.15sec with a peak overshoot of 1478 rpm and a peak undershoot of 1420 rpm. A decrease in supply voltage at 2 seconds reduces the speed with a peak overshoot of 1407 rpm and peak undershoot of 1378 rpm as shown in Figure 25.

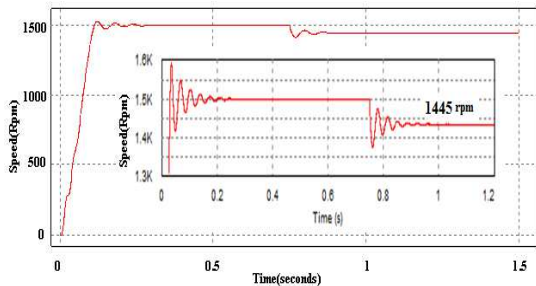


Figure 22. Speed Response When Load Torque of 15 Nm Applied at .75sec

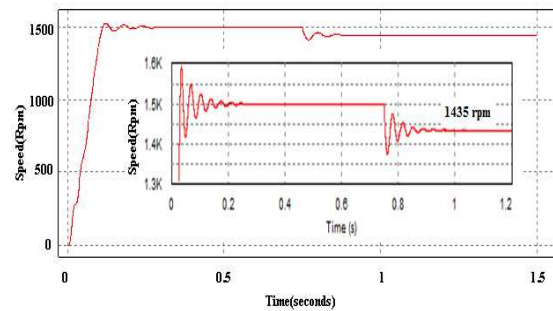


Figure 23 Speed Response When Load Torque of 25 Nm Applied at .75sec

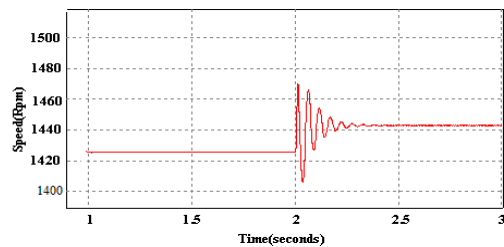


Figure 24 Speed Response When Supply Voltage is Increased at 2sec

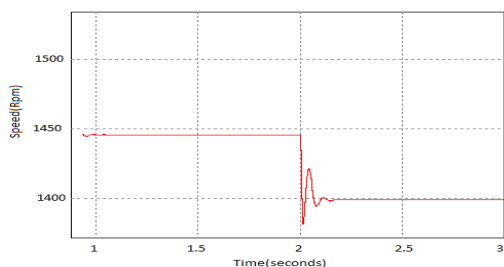


Figure 25. Speed Response When Supply Voltage is Decreased at 2sec

In the five level cascaded H-bridge inverter fed induction motor, the motor reaches rated speed

and settles at 0.3seconds. In seven level cascaded inverter the motor reaches the rated speed much earlier than a five level cascaded inverter.

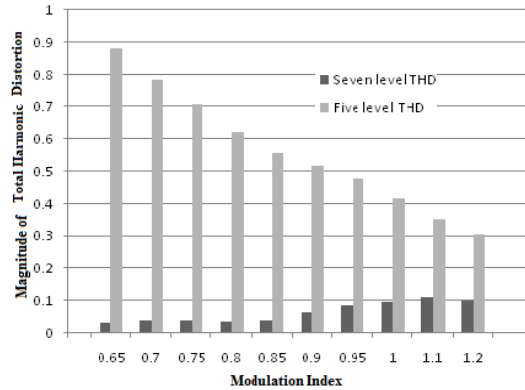


Figure 26. Total Harmonic Distortion Vs Modulation Index for a Five and Seven Level Inverter

The Figure 26 shows the magnitude of THD for five and seven level inverter fed induction motor for rated load torque of 25 Nm. The THD decreases for the five level inverter as the MI increases from 0.65 to 1.2. The THD remains low when the MI is increased from 0.65 to 0.85 for the seven level inverter and it increases when MI varies from 0.9 to 1.2. The Figure 27 shows the variation of the voltage for five and seven level inverters by varying modulation index from 0.4 to 1.2. The Figure 28 shows the variation of the total harmonic distortion for various load torque. It is observed that a seven level inverter gives lesser harmonics when compared to a five level inverter .

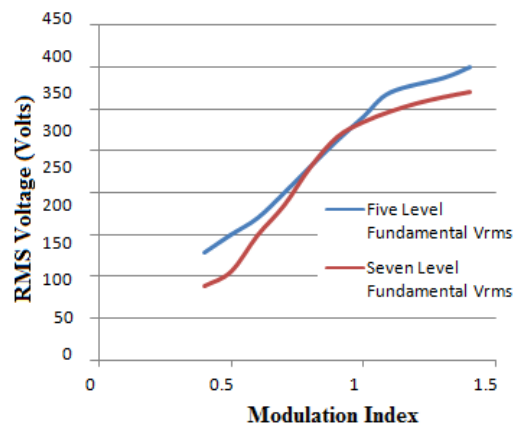


Fig. 27. Variation of RMS Voltage with Modulation Index for a Five and Seven Level Inverter

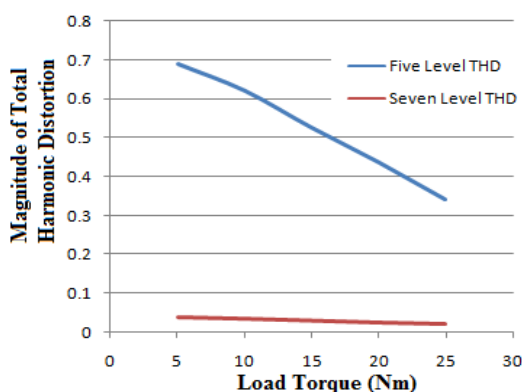


Fig. 28. Variation of THD with Load Torque for a Five and Seven Level Inverter

4. CONCLUSION

The Cascaded H-bridge inverters for five and seven-level with an induction motor are simulated using PSIM software. The firing pulses for the multilevel inverter are generated by using multi carrier triangular signals with a sinusoidal modulating signal of 50Hz frequency. The voltage magnitude of the fundamental component for a five level inverter is 1.8 times the magnitude of dc voltage whereas the voltage magnitude of fundamental component is 2.7 times the dc voltage for a seven level inverter. It is observed from the harmonic analysis that the value of THD for a seven level inverter is 3.45 % whereas for a five level inverter it is 37.3% at rated power output. When the machine delivers 3 KW output power, the loss in the seven level inverter is 0.500 KW whereas the power loss in a five level inverter is 0.960KW. The rise time and the settling time in a speed response for a seven level inverter fed motor are 0.15 and 0.2 seconds respectively. But, the rise time and settling time for a five level inverter fed motor are 0.3 and 0.35 seconds. Therefore, the speed response of a seven level inverter is much better than a five level inverter fed induction motor drive. It is inferred from the study that the seven level cascaded H-bridge inverter fed induction motor drive has high efficiency and quick response time when compared to a five level inverter. A seven level inverter fed induction motor drive is a good choice where improved efficiency and reduced harmonic content is required.

APPENDIX I

Specifications Adopted For the Induction Motor

RATINGS	VALUES
Power	3 KW
Frequency	50 Hz
Voltage	400V
Speed	1500 r/min
Stator Resistance, R_s	1.405 Ω
Rotor Resistance, R_r	1.395 Ω
Stator Leakage Inductance, L_s	0.005839H
Rotor Leakage Inductance, L_r	0.005839H
Magnetizing Inductance, L_m	0.1 722 H
Moment of Inertia, J	0.0131 kg-m ²
Poles	4

REFERENCES:

- [1] K. Sivakumar, A. Das, R. Ramchand, C. Patel, and K. Gopakumar, "A five-level Scheme for a four-pole induction motor Drive by feeding the identical voltage-Profile windings from both sides", *IEEE Transactions on Industrial Electronics*, Vol. 57, No.8, pp. 2776–2784, Aug.2010
- [2] F. Khoucha, S. M. Lagoun, K. Marouani, A. Kheloui, and M. El Hachemi Benbouzid, "Hybrid cascaded H-Bridge multilevel-Inverter Induction motor- drive direct torque Control for automotive applications", *IEEE Transactions on Industrial Electronics*, Vol. 57, no. 3, pp. 892–899, Mar. 2010.
- [3] W. Song and A. Q. Huang, "Fault-tolerant Design and control strategy for cascaded H-Bridge multilevel converter-based STATCOM", *IEEE Transactions on Industrial Electronics*, Vol. 57, No.8, pp. 2700–2708, Aug. 2010
- [4] N. Farokhnia, S. H. Fathi, and H. R. Toodeji, "Direct nonlinear control for individual DC Voltage balancing in cascaded multilevel DSTATCOM", in *Proc. IEEE International Conference EPECS*, 2009, pp. 1–8.
- [5] C. Cecati, F. Ciancetta, and P. Siano, "A Multilevel inverter for PV systems with Fuzzy logic control", *IEEE Transactions Industrial Electronics*, Vol. 57, No. 12 pp. 4115–4125, Dec.2010.
- [6] Jang-Hwan Kim, Seung Ki Sul, "A carrier based PWM method with optimal switching sequence for a multilevel four leg voltage source inverter", *IEEE Transactions on*

- Industry applications*, Vol. 44, No. 4, July/August 2008.
- [7] J. Rodriguez, J.S. Lai, and F. Z. Zeng, "Multilevel inverters: A Survey of Topologies Controls and Applications" *IEEE Transactions on Industrial Electronics*, Vol. 49, No. 4, pp.724 - 738, Aug.2002
- [8] K. El-Naggar and T. H. Abdelhamid, "Selective Harmonic Elimination of New Family of Multilevel Inverters Using Genetic Algorithms", *Energy Conversation Management*, Vol. 49, No. 1, pp. 89–95, Jan. 2008.
- [9] Bill Diong, Hossein Sepahvand and Keith A. Corzine, "Harmonic Distortion Optimization of Cascaded H-bridge Inverters Considering Device Voltage Drops and Non integer DC Voltage Ratios" *IEEE Transactions on Industrial Electronics* Vol. 60, No. 8, pp 3106-3104, August 2013
- [10] Yu Liu, Hoon Hong, P, and Alex Q Huang P "Real-Time Algorithm for Minimizing THD in Multilevel Inverters with Unequal or Varying Voltage Steps under Staircase Modulation" *IEEE Transaction on Industrial Electronics*, Vol. 56, No. 6, pp 2249-2253, June 2009.
- [11] Nima Yousefpoor, Naeem Farokhnia, and Hossein skarian Abyaneh, "THD Minimization Applied Directly on the Line-to-Line Voltage of Multilevel Inverters", *IEEE Transactions on Industrial Electronics*, Vol. 59, No. 1, pp 373-380, January 2012.
- [12] Alireza Nami, Firuz Zare, Arindam Ghosh, Frede Blaabjerg "A Hybrid Cascade Converter Topology with Series-Connected Symmetrical and Asymmetrical Diode-Clamped H-Bridge Cells" *IEEE Transactions on Power Electronics*, Vol. 26, No. 1, pp 51-65, January 2011.
- [13] P. P. Rajeevan, K. Sivakumar, K. Gopakumar "A Seven-Level Inverter Topology for Induction Motor Drive Using Two-Level Inverters and Floating Capacitor Fed H-Bridges" *IEEE Transactions on Power Electronics*, Vol. 26, No. 6, pp 1733-1740, June 2011.
- [14] P. Roshankumar, P. P. Rajeevan, Jose I. Leon, Leopoldo G. Franquelo "A Five-Level Inverter Topology with Single-DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge" *IEEE Transactions on Power Electronics*, Vol. 27, No. 8, pp 3505- 3512, August 2012.
- [15] P. P. Rajeevan and K. Gopakumar "A Hybrid Five-Level Inverter with Common-Mode Voltage Elimination Having Single Voltage Source for IM Drive Applications" *IEEE Transactions on Industry Applications*, Vol. 48, No. 6, pp 2037-2047, Nov/Dec 2012.