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DESIGN AND IMPLEMENTATION OF LOW COST SEPIC PHOTOVOLTAIC SYSTEM FOR CONSTANT VOLTAGE

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ABSTRACT

The photovoltaic (PV) system gives variable output voltage due to temperature and insolation variation with respect to time. This paper presents the design of a SEPIC converter for getting constant output voltage from PV system using a simple control circuit. The SEPIC is designed to make the power flow from PV module to load effectively and maintaining constant output voltage. This paper gives the detailed design and implementation of a 20W prototype SEPIC integrated PV power supply with soft start feature. The efficiency of the proposed method is proved with simulation results and prototype experimental results.

Keywords: *Boost, Control, Converters, Charging, Prototype , SEPIC.*

1. INTRODUCTION

Due to energy crisis throughout the world, tapping solar energy is more attractive nowadays. However due to more constraints it is difficult to maintain constant output from the PV Module during all hours in a day.

In recent years, many research works have addressed the development of solar system. In [1], a SEPIC with the PV module input and the peak-current-mode control has been developed including small-signal model of SEPIC, the PV voltage controller and the MPPT controller. A novel technique for efficiently maximizing the output power of a solar panel supplying to a load or battery bus under varying meteorological condition is discussed in [2]. A SEPIC which is used as PFC (Power Factor Correction) stage is a good solution for power supplies in electronic ballast [3]. A SEPIC is applied to interface the Thermoelectric (TE) power-generator output to the battery and to track the maximum power point (MPPT) of the TE power generator[4]. A Posicast control based on feedback structure has been designed and implemented to eliminate the peak overshoot output voltage of the SEPIC converter, to improve the settling time of step response and to reduce the sensitivity of classical feed forward Posicast control in [5].

The integration of a voltage multiplier cell with a classical SEPIC is introduced in [6], in order to obtain a high step-up static gain operating with low input voltage and a low step-up static gain for the high input voltage operation for wide input voltage ranges. In [7], a power distribution system having a central power supply that acts as a controlled current source whose output is connected to individual loads on a time shared basis is presented. The output voltage is regulated by hysteresis or constant frequency PWM technique.

In this paper the SEPIC integrated photovoltaic system with soft start feature is presented. The IC SG3525A is used to control the switching operation of MOSFET for maintaining constant output voltage of a solar panel supplying to the load under varying meteorological condition. The SEPIC converter is operated in continuous conduction mode and duty cycle of MOSFET is adjusted so that the output voltage is maintained constant. The capability of this proposed circuit is verified with the MATLAB simulation and experimental verification is carried out using the IC SG3525A. The tracking capability of the proposed technique has been verified experimentally with a 20W solar panel at different insolation (incident solar radiation) levels.

SOLAR ENERGY CONVERSION

A solar panel is a packaged and connected assembly of photovoltaic cells. The solar panel can be used as a component of a larger photovoltaic system to generate and supply electricity in commercial and residential applications. Each panel is rated by its DC output power under standard test conditions. Because a single solar panel can produce only a limited amount of power, most installations contain multiple panels. There are many types of PV systems namely the stand alone

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and grid connected PV system. The standalone PV system require battery for the supply of power to the load during the low solar period. Generally the I-V characteristic of a solar panel depends on insolation level and temperature. If the output voltage of PV system does not match with the battery voltage, the energy conversion efficiency of PV system is reduced. Hence it is required to track the PV panel voltage at all operating conditions.

Fig.1 shows the PV panel which is represented by a voltage source Vg connected in series with an output resistance rg. The input voltage and the equivalent input resistance of the SEPIC converter are Vi and ri respectively. Generally, converters are used to improve the efficiency and control of PV panel output voltage.

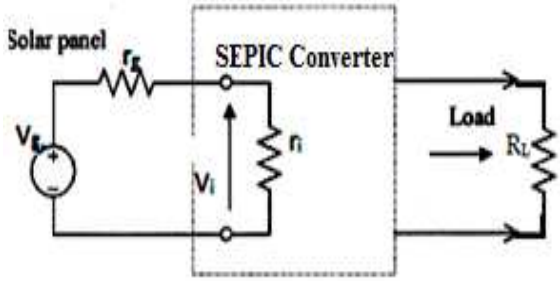

Fig.1 Equivalent Circuit Of PV With Converter.

Fig.2 illustrates the I-V characteristics of the PV panel under different insolation conditions.

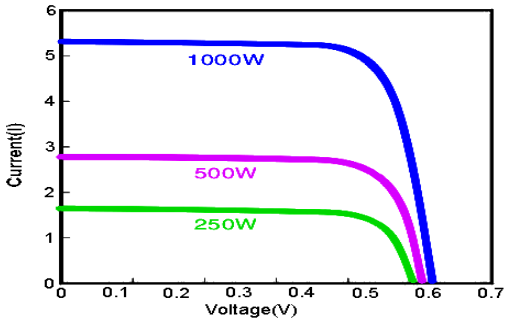

Fig. 2 PV Panel I-V Characteristics

2. THEORY AND PRINCIPLE OF SEPIC CONVERTER

The SEPIC is a DC to DC converter in which the output voltage is having same polarity as that of input voltage. One benefit of the SEPIC converter is that the input ripple current in the input capacitor is continuous. This reduces the amount of input capacitance necessary for low-ripple voltage, which reduces EMI (Electro Magnetic Interference). SEPIC converter maintains a fixed output voltage regardless of whether the input voltage is above, equal or below the output voltage.

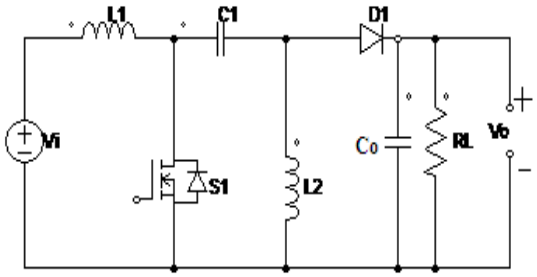

Fig.3 Basic SEPIC converter.

Fig.3. shows the SEPIC basic diagram. Vi is the input voltage of the converter, Vo is the output voltage, L1 is the inductor connected at the input end and the maximum load current flows in this inductance. L2 is connected in parallel to the load. The switch s1 is connected parallel with the input voltage. The switch can be made on and off during the operation.C1 is the coupling capacitor which stores the voltage. The duty cycle D is defined by the general equation:

$$M = \frac{v_o}{v_i} \quad (1)$$

$$D = \frac{T_{ON}}{T} \quad (2)$$

Where TON is the on-time of the switch and T is the switching period. The duty cycle is a function of M, where M is the voltage conversion ratio,

$$D = \frac{M}{M+1} \quad (3)$$

From the equation (3) the M as function of D,

$$M = \frac{D}{1-D} \quad (4)$$

From the equation (4), the output voltage can be defined as

$$V_o = \frac{D}{1-D} V_i \quad (5)$$

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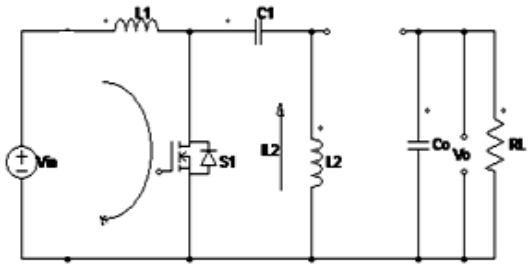

Fig.4. SEPIC current flow when S1 is in ON condition.

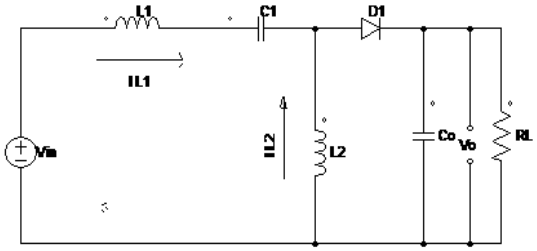

Fig .5 SEPIC current flow when S1 is in OFF condition.

A SEPIC is said to be in continuous-conduction mode if the current through the inductor L1 never falls to zero. During a SEPIC's steady-state operation, the average voltage across capacitor C1 is equal to the input voltage. Because capacitor C1 blocks direct current, the average current through C1 is zero, making inductor L2 the only source of load current. Therefore, the average current through inductor L2 is the same as the average load current and hence independent of the input voltage. The voltages are the same in magnitude as well as above or below. The ripple currents from the two inductors will be equal in magnitude.

Fig 4. Shows SEPIC current flow when S1 is turned on, current I_{L1} increases positive direction and the current I_{L2} increases in the negative direction. The energy to increase the current I_{L1} comes from the input source. Since S1 is a short while closed, and the instantaneous voltage V_{C1} is approximately V_{IN}, the voltage V_{L2} is approximately $-V_{IN}$. Therefore, the capacitor C1 supplies the energy to increase the magnitude of the current in I_{L2} and thus increase the energy stored in L2.

Fig.5. shows SEPIC current flow when switch S1 is turned off, the current I_{C1} becomes the same as the current I_{L1}, since inductors do not allow instantaneous changes in current. The current I_{L2} will continue in the negative direction, in fact it never reverses direction. It can be seen from the diagram that a negative I_{L2} will add to the current I_{L1} to increase the current delivered to the load. Using Kirchhoff's Current Law, it can be shown that $I_{D1} = I_{C1} - I_{L2}$. It can then be concluded, that while S1 is off, power is delivered to the load from L2, L1 and C1 of energy storage elements. And maintain the load voltage in constant.

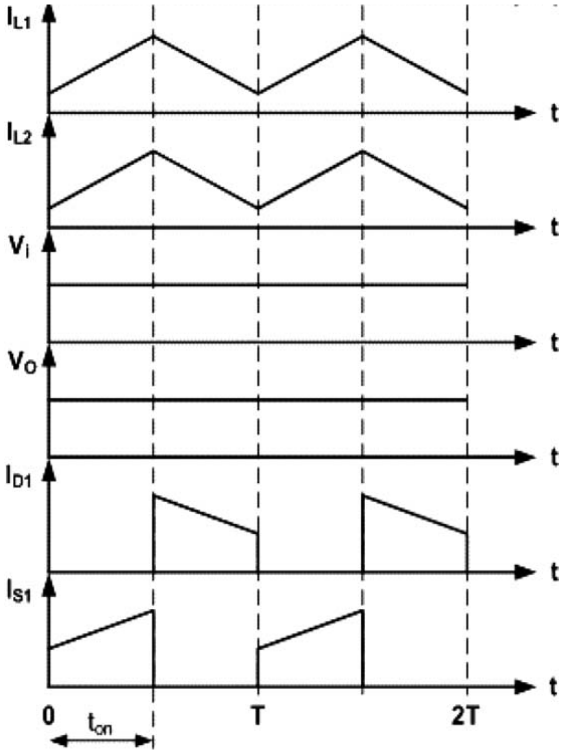

Fig.6.Theoritcal WAVEFORM OF Sepic CONVERTER

3. SIMULATION

The simulation results are presented in this section. In Fig.7, the SEPIC converter is implemented using the Simulink tool of Matlab. The values of inductors and capacitors are determined on the basis of current and voltage output criteria with design calculation. The implemented values are L1 = L2 = 2.51 mH, C1=10µF, Co=0.23µF. The SEPIC converter is simulated according to switching function, which is valid in CCM (Continues Conduction Mode) operations. The PI controller is used to regulate the output voltage. The simulations are carried out using a fixed step ode5 (Dormant-Prince) solver. The step size is 1µs.

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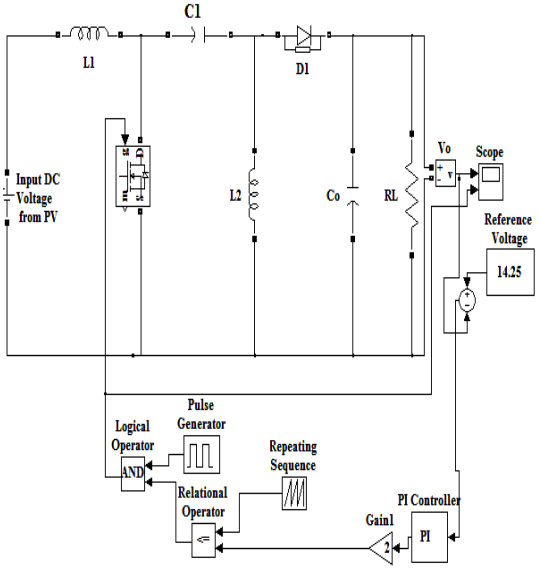

Fig 7. SEPIC Simulation Implemented In MATLAB

The PI controller compares the output voltage with reference output voltage which is 14.25V to calculate the error and the output of PI. Controller is used to control the duty cycle of the gate pulse given to the MOSFET.

The specification of SEPIC converter is given in Table 1.

Table 1 Specification Of SEPIC Converter.

SL.No	Description	Specification
1	Input Voltage	11V DC -20V DC
2	Output Voltage	14.25V DC
3	Output Current	1.42A
4	Ripple	40%
5	Duty Cycle range	0.55 to 0.42
6	Switching frequency	330KHz

Fig 8.illustrates the waveform of the input and output voltages by applying classical PI controller to the MOSFET. The switching frequency is 330 KHz. The DC output voltage Vo is stabilized at the reference value even though input voltage changes.

Fig .8 Simulated Input Voltage And Output Voltage

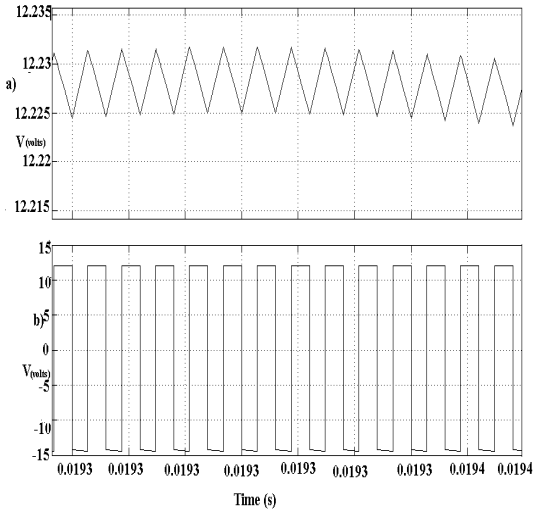

Fig.9 Simulated Output Voltage Waveform Across C1and L1

Fig.9.shows the output voltage waveform across C1 and L1.Fig.10. shows the simulated voltage and current waveform in MOSFET. Fig.11.shows the simulated a)output voltage and b) output current waveforms of SEPIC c) Inductor (L1) current and d) Inductor (L2) current.Fig.12. shows the simulated waveform of a) input voltage and b) input current.

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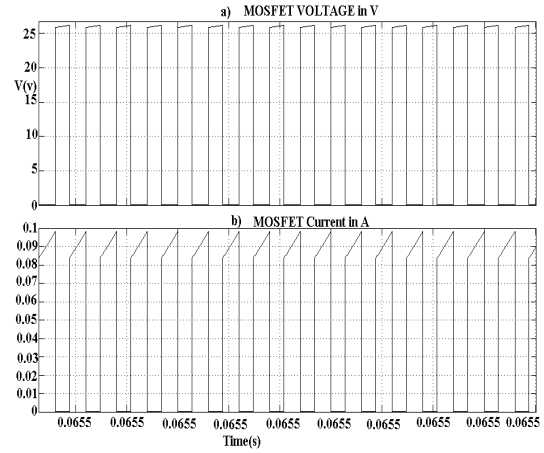

Fig.10.Simulated Voltage And Current Waveform In MOSFET.

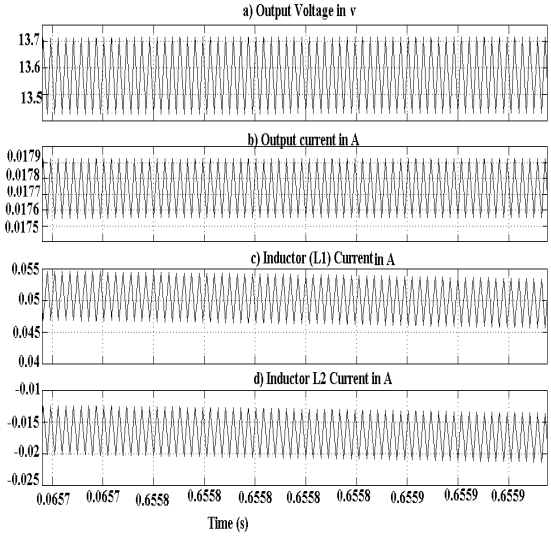

Fig.11.Simulated A) Output Voltage And B) Output Current Waveforms, Of SEPIC C) Inductor(L1) Current And D) Inductor (L2)Current.

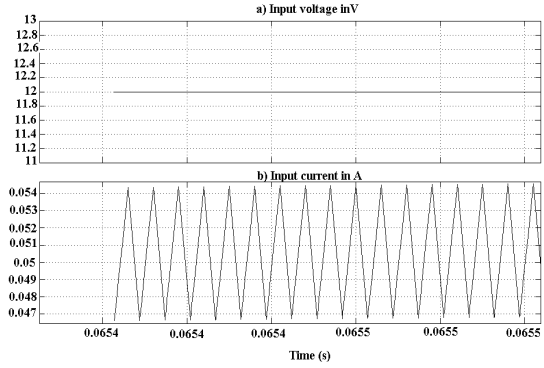

Fig.12.Simulated A) Input Voltage And B) Input Current Waveform.

4. EXPERIMENTAL DESIGN

A.SEPIC CIRCUIT DESIGN

The SEPIC converter designed is working with the continuous conduction mode that means current through inductor L1 and inductor L2 never reaches zero. The output voltage may be lower or higher than input voltage. In this circuit the capacitor C1 isolates the input from output and provides the protection against the short circuit.

Duty cycle is calculated with the equation (6).

$$D = \frac{V_o + V_D}{V_1 + V_o + V_D} \quad (6)$$

Where Vo is the output voltage, V_D is the diode voltage drop and Vi is input voltage.

In this circuit the input voltage is considered as 11-20V and the output voltage expected is 14.25V, since the input is coming from solar panel. Load voltage will be maintained almost constant irrespective of the solar panel voltage. The maximum and minimum duty cycle will be calculated from the equations [7-8].

$$D_{max} = \frac{V_o + V_D}{V_{1min} + V_o + V_D} \quad (7)$$

$$D_{min} = \frac{V_o + V_D}{V_{max} + V_o + V_D} \quad (8)$$

It is assumed that the V_D is 0.5 volts. Then the maximum duty cycle is calculated from the Equation [7] and is obtained as $D_{max} = 0.55$.

The minimum duty cycle is found from the equation [8] and is obtained as $D_{min} = 0.42$.

B. SELECTION OF INDUCTOR

The inductors L1 and L2 will be selected based on ripple current. The good inductor may have the peak to peak ripple current of approximately 40% of its maximum input current at minimum input voltage. In this circuit the ripple current flowing in equal value inductors can be calculated from the equation [9].

$$\Delta I_L = I_i \times 40\% = I_o \times \frac{v_o}{v_{1,min}} \times 40\% \quad (9)$$

and is obtained as $\Delta I_L = 0.6697A$

The inductor value can be calculated by the equation [10].

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$$L_1 = L_2 = L = \frac{v_{1,min}}{\Delta I_L \times f_s} \times D_{max} \quad (10)$$

Where fs is the switching frequency and Dmax is the maximum duty cycle during minimum input voltage from solar panel. The peak current has to be calculated so that it does not saturate the inductor and is given by the equation [11-12]

$$I_{l1peak} = I_o \times \frac{v_o + v_D}{v_{imin}} \times \left(1 + \frac{40\%}{2}\right) \quad (11)$$

$$I_{21peak} = I_o \times \left(1 + \frac{40\%}{2}\right) \quad (12)$$

C. MOSFET SELECTION

The consideration for the MOSFET IRF830 choice are the minimum threshold voltage (V_{thmin}), the ON-Resistance between drain and source R_{DS}=8mΩ, gate drain charge Q_{GD} =10nc and the maximum drain source voltage $V_{DS(max)}$ must be higher than the V_{IN}+V_{OUT}.

The logic level threshold MOSFET is selected based on the gate drive voltage. The gate drive current I_G=0.3A is given to MOSFET and it is considered in this design. The peak switch current $I_{s(peak)}$ is given by the equation (13).

$$I_{s(peak)} = I_{l1peak} + I_{l2peak} \quad (13)$$

RMS current of the MOSFET is given by the equation (14).

$$I_{srms} = I_o \sqrt{\frac{v_o + v_{imin} \times v_o}{v_{min}^2}} \quad (14)$$

The MOSFET power dissipation P_s is given (15).

$$P_s = I_{srms}^2 \times R_{DS} \times D_{max} + \left(V_{i,min} + V_o\right) \times I_{speak} \times \frac{Q_{CD} \times f_{sw}}{I_C} \quad (15)$$

The total power dissipation for MOSFET IRF830 is sum of conduction and switching losses. The drain source resistance is selected based on maximum operating temperature.

D. OUTPUT DIODE SELECTION

The output diode is selected to handle the peak current and reverse voltage. In SEPIC, the diode current is same as the switch peak current I_{Speak}.

The minimum peak reverse voltage is calculated using the equation (16).

$$V_{RD} = V_{i,max} + V_{o,max} \quad (16)$$

Schottkey diode is selected to minimize the conduction loss.

E. SEPIC COUPLING CAPACITOR

The selection of the capacitor C_1=10μF, depends on RMS current which is given by (17).

$$I_{cs(rms)} = I_o \times \sqrt{\frac{v_o + v_D}{v_{imin}}} \quad (17)$$

The SEPIC capacitor is selected for large RMS current relative to the output power. The voltage of SEPIC capacitor is selected larger than the maximum input voltage.

The peak to peak ripple voltage on C1 by taking no ESR (Equivalent Series Resistance) is given by the equation (18).

$$\Delta V_{c1} = \frac{I_o \times D_{max}}{c_1 \times f_{sw}} \quad (18)$$

The capacitor that meets the RMS current would mostly produce the small ripple voltage on C_1. The peak voltage will be close to the input voltage. Tantalum capacitor is selected for C1 and Co.

F. OUTPUT CAPACITOR SELECTION

In this SEPIC converter the switch (MOSFET) is turned on, the inductor L1 is charging and the capacitor Co gives the output current, hence the output capacitor faces the large ripple current. Thus the capacitor is selected so as to handle maximum RMS current. The RMS current calculated using the equation (19).

The capacitor that meets the RMS current would mostly produce the small ripple voltage on C_1. The peak voltage will be close to the input voltage. Tantalum capacitor is selected for C1 and Co.

$$I_{C2(rms)} = I_o \times \sqrt{\frac{v_o + v_D}{v_{imin}}} \quad (19)$$

G. SOLAR PANEL SELECTION

Mono crystalline silicon (c-Si) is often made using the Czochralski process. Single-crystal wafer cells tend to be expensive, and because they are cut from cylindrical ingots, do not completely cover a square solar cell module without a substantial waste of

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refined silicon. Hence most c-Si panels have uncovered gaps at the four corners of the cells.

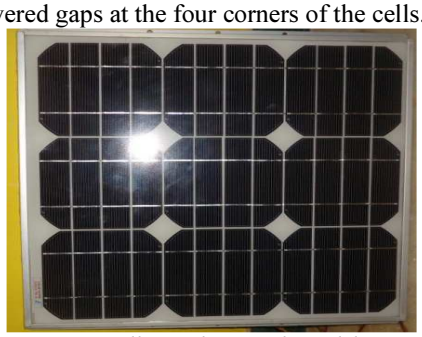

Fig.13.Monocrystalline Solar Panel, Model No Be18s12

The designed SEPIC converter utilizes the solar power source using the Bharat electronics solar photovoltaic module, Model No BE18S12. Its rated voltage is 12 V, rated peak power 18W, rated maximum voltage is 17 volts as given in Fig.13. Two panels are connected in series to reach the maximum voltage more than 21 volts. This panel is mono crystalline silicon panel which is more efficient than the polycrystalline solar panel. At 25° C temperature and about 1000W/m² solar insolation are given in the main specification of this panel.

H. PULSE WIDTH MODULATING CIRCUIT

In this work, a simple, low cost ICSG3525 is used as the control circuit. Fig 14. shows the compensation and soft-start terminals (Pins 9 and 8) which have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 mA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

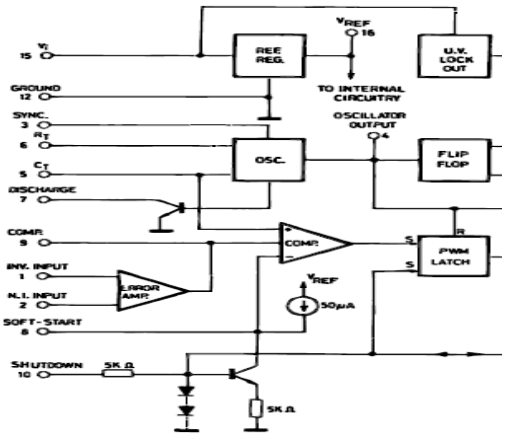

Fig 14. Soft Start Circuitry Of IC SG 3525.

The shutdown circuitry of pin 10 in SG3525 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on pin 10 performs two functions:

1. The PWM latch is immediately set providing the fastest turn-off signal to the outputs

2. 150 mA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor,

The convenient implementation of pulse-by-pulse current limiting is provided by holding pin 10 high for a longer duration, however, it will ultimately discharge the external capacitor, recycling slow turn-on upon release. The pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

The integrated circuit SG3535 is used, which is having advantage of lowered external parts count. The on-chip + 5.1 V reference is trimmed to ± 1 % and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors.

A single resistor between the CT and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages by providing instantaneous turn off. These functions are also controlled by an under voltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages.

This lockout circuitry includes approximately 500mV of hysteresis for jitter free operation. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG3525A output stage features NOR logic, giving a LOW output for an OFF state.

Fig.15 shows the SEPIC circuit with the IC SG 3525. The components of SEPIC are chosen as per the design calculation.

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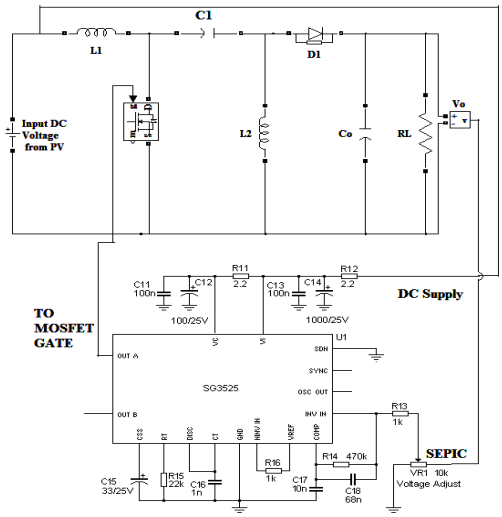

Fig. 15 Sepic With Pulse Width Control Circuit Sg3525

Table. 2 shows the list of components used in the developed SEPIC.

Table. 2 List Of Components

S.LNo	Symbol	Component	SPECIFICATION
1	C1	Capacitor	10µF/25v
2	Co	Capacitor	0.23µF
3	C11	Capacitor	1000µF/40v
4	C12	Capacitor	100µ/40v
5	C16	Capacitor	1nF /63v
6	C18	Capacitor	68nF
7	C15	Capacitor	33µF/25V
8	C17	Capacitor	10nF/63v
9	VR1	Variable resistor	10k
10	IC1	IC SG3525	12v/
11	S1	IRF 830A MOSFET	24V
12	L1	Inductor	2.51mH
13	L2	Inductor	2.51mH
14	Di	Diode	IN40001
15	D1	Diode	IN40001
16	D2	Zenar diode	12V
17	RL	Load Resistance	1.8K
18	R1	Resistor	1K
19	R11	Resistor	2.2K
20	R14	Resistor	470K
21	R16	Resistor	1K
22	R12	Resistor	2.2K
23	R13	Resistor	10K
24	R15	Resistor	22K
25	R25	Resistor	1K

Table. 3 shows the readings taken from the experimental setup. The values of Vi,Vo,Ii and Io are measured under different insolation condition. The input voltage is varying from 11.3 V to 20 V and the output voltage is maintained at nearly 14.25V.

Table. 3 Input And Output Voltages, Current, Power And % Efficiency

S.No	INPUT			OUTPUT			%EFFICIENCY
	VOLTAGE (volts)	CURRENT (A)	POWER (watts)	VOLTAGE (volts)	CURRENT (A)	POWER (watts)	Output power/ input power
1	11.3	1.48	16.72	13.38	0.99	13.24	79.2%
2	12	1.48	17.76	14.23	0.99	14.08	79.2%
3	12.5	1.43	17.87	14.23	1.04	14.79	82.8%
4	13	1.43	18.59	14.23	1.04	14.79	79.5%
5	13.5	1.38	18.63	14.24	1.04	14.80	79.4%
6	14	1.34	18.76	14.24	1.09	15.52	82.2%
7	14.5	1.30	18.85	14.24	1.09	15.52	82.3%
8	15	1.28	18.90	14.24	1.09	15.52	82.1%
9	15.5	1.23	19.06	14.25	1.11	15.81	82.9%
10	16	1.20	19.20	14.25	1.11	15.81	82.3%
11	16.5	1.17	19.30	14.25	1.11	15.81	81.9%
12	17	1.15	19.55	14.25	1.11	15.81	80.1%
13	17.5	1.12	19.60	14.25	1.11	15.81	80.6%
14	18	1.09	19.62	14.25	1.11	15.81	80.5%
15	18.5	1.07	19.79	14.25	1.15	16.38	82.7%
16	19	1.05	19.95	14.25	1.15	16.38	82.1%
17	19.5	1.02	19.89	14.25	1.15	16.38	82.3%
18	20	0.99	19.80	14.25	1.15	16.38	82.7%
19	20.5	0.97	19.88	14.25	1.15	16.38	82.3%

Fig.16 Shows the input voltage from the panel and output voltage in a day. From the graph, It is found that Vo is maintained constant though Vi changes .

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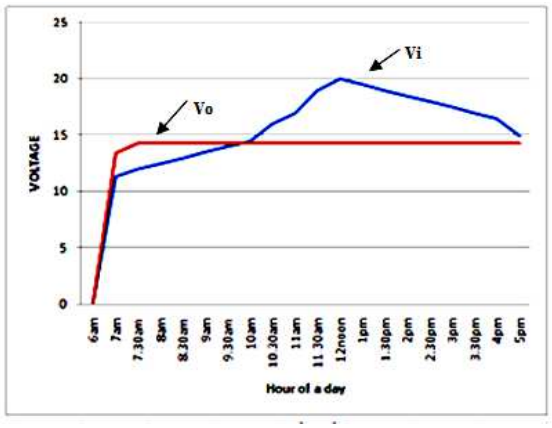

Fig.16. Plot Of Vi And Vo Variations During A Day

Fig.17 shows the experimental setup for the developed SEPIC converter.

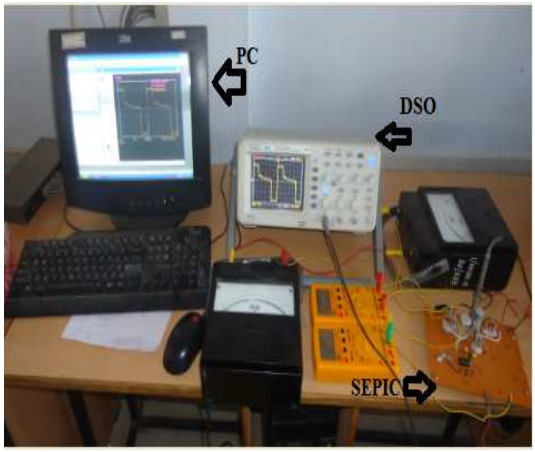

Fig.17. Experimental Setup

Fig.18 shows the plot of efficiency with respect to load current. The maximum efficiency is obtained as 82.9%.

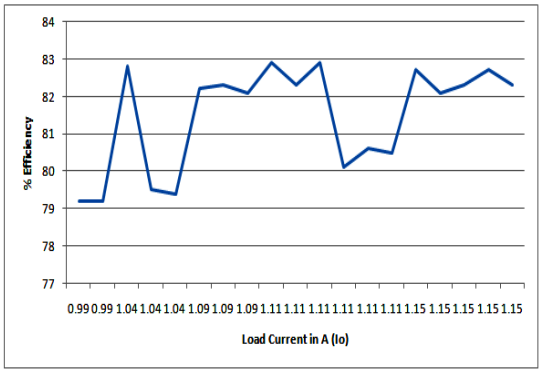

Fig .18 Plot Of Efficiency Vs Load Current

Fig.19 and Fig. 20 shows the output voltage waveform at 11.3V DC and 19VDC input respectively.

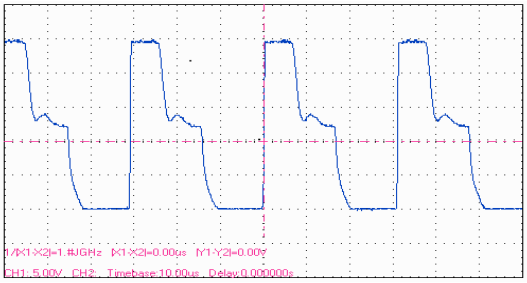

Fig.19. Output Voltage Waveform At 11.3V DC Input

3. CONCLUSION

A SEPIC converter using low cost control circuit based on IC SG3525 has been designed for PV system. The converter maintains constant output voltage even though the output voltage from PV system changes The simulation of the SEPIC converter based on PV system is done using MATLAB Simulink which uses PI controller. A prototype 20W SEPIC converter is constructed with two number of 12V solar panels and IC SG3525 and the results are also verified experimentally.

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