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A CLOCK CONTROL STRATEGY BASED CLUSTERING METHOD FOR PEAK POWER AND RMS CURRENT REDUCTION

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ABSTRACT

In VLSI circuits, peak power and RMS current reduction are the challenging tasks. Both power density and peak power are proportional to each other. If these parameters are reduced, it may lead to a timing violation and logic failures. In order to overcome these failures, Clock Control Strategy based Clustering Method (CCSCM) is proposed. In the proposed clustering method, we design to reduce the path delays, to find the inequality paths and to make it equality through a slack values using slack variables. In previous method, benchmark circuits are used which results in finding difficult in a slack delay and RMS current reduction. But in our proposed algorithm, CMOS full adder is developed which make use of finite impulse response (FIR) filter design based on the 180 NM technology. A 180 nm generation logic technology has been developed with high performance 140 nm LGATE transistors, six layers of aluminum interconnects and low-e SiOF dielectrics. The transistors are optimized for a reduced 1.3-1.5 V operation to provide high performance and low power. The interconnects feature high aspect ratio metal lines for low resistance and fluorine doped SiO2 inter-level dielectrics for reduced capacitance. 16 Mbit SRAMs with a 5.59 mm2 6-T cell size have been built on this technology as a yield and reliability test vehicle.
Keywords: *LGATE, Clock Control Strategy Based Clustering Method, FIR Filter, CMOS Full Adder, Path Delay, Slack Value, RMS Current Reduction.*

1. INTRODUCTION

Clustering is the process of partitioning or grouping a given set of patterns into disjoint *clusters*. This is done such that patterns in the same cluster are alike and patterns belonging to two different clusters are different. Clustering has been a widely studied problem in a variety of application domains including neural networks, AI, and statistics. Clustering algorithms are often useful in applications in various fields such as visualization, pattern recognition, learning theory, and computer graphics. A classical vector quantization problem is usually solved as a gradient-descent problem. However, in practice a more convenient computing scheme is batch computation, usually named the K-means algorithm [2]. The k-means method has been shown to be effective in producing good clustering results for many practical applications. However, a direct algorithm of k-means method requires time proportional to the product of number of patterns and number of clusters per iteration. This is computationally very expensive especially for large datasets.

The proliferation of portable systems and mobile computing platforms has increased the need for the design of low power consuming integrated circuits. The increase in chip density and clock frequencies due to technology advances has made low power design a critical issue. Low power VLSI design is further driven by several other factors such as thermal considerations and environmental concerns. In battery driven portable systems, the peak power, cycle difference power, peak power differential, average power and energy are equally critical design constraints.

In a modern VLSI circuit, the most common strategy for clock distribution is to insert a large number of buffers along the paths from clock source to flip-flops, forming a buffered-tree structure. Each transition of the clock signal changes the state of each capacitive node within the clock tree, in contrast with the switching activity in combinational block, where the change of logic states is dependent on the logic function. In low power VLSI design, using deep sub-micrometer and nano-meter technologies, both the

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peak power and the total power are equally critical design limits.

The reduction of peak power consumption is needed for the following reasons:

- to maintain supply voltage levels
- to increase reliability.

Energy and average power reduction is needed for the following reasons

- to increase battery life time
- to enhance noise margin
- to reduce cooling and energy costs
- to reduce use of natural resources
- to increase system reliability.

2. RELATED WORK

Yow-Tyng Nieh et.al [1] proposed opposite-phase scheme to reduce the peak current caused by the clock tree. to divide the clock buffers at each level of the clock tree into two sets: an half of clock buffers operate at the same phase of the clock source, and another half of clock buffers operate at the opposite phase of the clock source. Consequently, our approach can reduce the peak current of the clock tree nearly 50%. The idea of storing the data points in a kd-tree in clustering was considered by Moore in the context of estimating the parameters of a mixture of Gaussian clusters. He gave an efficient implementation of the well-known EM algorithm. The application of this idea to k-means was discovered independently. The purpose of this paper is to present a more detailed analysis of this algorithm. In particular, we present a theorem that quantifies the algorithm's efficiency when the data are naturally clustered and we present a detailed series of experiments designed to advance the understanding of the algorithm's performance.

Martin Ester et.al [2] proposed new clustering algorithm Density Based Spatial Clustering of Applications with Noise (DBSCAN) relying on a density-based notion of clusters which is designed to discover clusters of arbitrary shape. DBSCAN requires only one input parameter and supports the user in determining an appropriate value for it. It discovers clusters of arbitrary shape. Finally, DBSCAN is efficient even for large spatial databases.

Bellos et.al [3] proposed a novel peak power dissipation reduction method based on test vector ordering with vector repetition and vector modification. The proposed method takes advantage of the vectors repeated and through modification and copying/removal of vectors it achieves significant savings on peak power dissipation.

WaiChing Douglas Lam et.al [4] proposeD an algorithm that performs clock skew scheduling to minimize the number of simultaneous switching events such that the power supply noise is suppressed. Our approach establishes a direct relationship between current (drawn by a circuit element, sequential or combinational) and skew by the concept of envelope waveforms, using a graphical representation. We provide a graph based scheduling approach to reduce the peak current and to minimize the difference between the current peaks and valleys such that the current profile of the entire circuit is smoothened.

Inderjit et.al [5] proposed a parallel clustering algorithm on distributed memory multiprocessors, that is, on a shared-nothing parallel machine, and analytically and empirically validate our parallelization strategy. Specifically, we propose a parallel version of the popular *k*-means clustering algorithm based on the message-passing model of parallel computing

Bradly et.al [6] presented a scalable clustering framework applicable to a wide class of iterative clustering. We require at most one scan of the database. In this work, the framework is instantiated and numerically justified with the popular K-Means clustering algorithm. The method is based on identifying regions of the data that are compressible, regions that must be maintained in memory, and regions that are discardable. The algorithm operates within the confines of a limited memory buffer.

Saraju et.al [7] addressed simultaneous peak power and average power reduction at behavioral level using low power datapath scheduling techniques. Two datapath scheduling schemes, one using multiple supply voltage and dynamic clocking and another using multiple supply voltage and multicycling have been introduced. ILP based optimization techniques were used for the above two modes of datapath operations. Significant amount of peak and average power reduction over the single supply voltage and single frequency scenario could be achieved in both the cases by the proposed scheduling algorithm. The reductions attained in peak power, average power and power delay product by using combined multiple supply voltage and dynamic frequency clocking were noteworthy.

Hyman et.al [8] presented a new clock control strategy for peak-power reduction in VLSI circuits. In the proposed method, the simultaneous switching of combinational paths is minimized by

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taking advantage of the delay slacks among the paths and clustering the paths with similar slack values. Once the paths are identified based on the path delays and their slack values, the clustering algorithm determines the ideal number of clusters for the given circuit and for each cluster the maximum possible phase shift that can be applied to the clock. The paths are assigned to clusters in a load balanced manner based on the slack values and each cluster will have a phase shift possible on its clock depending on the slack. Thus, the proposed register-transfer level (RTL) method takes advantage of the logic-path timing slack to re-schedule circuit activities at optimal intervals within the unaltered clock period. In this work, slack values are 1st analysed, then peak current reduction is done. not able to produce reduction of peak power and rms current for all circuits other than benchmarks reduction of average and peak power at behavioral and logic level alone focused. Analysis of peak power is tedious through path clustering, identifying the path and doing this is also a tough path. Benchmarks circuit comparison alone discussed.

3. OVERVIEW OF PROPOSED K MEANS ALGORITHM

First Cluster the primary input based on maximum delay in the input and group the circuits which have the same slack values by using the K means algorithm, this can be done by the program coding which gives the clustered circuit values. Assign each observation to the cluster whose mean yields the least within-cluster sum of squares. Find the number of nodes associated with the cluster assign each point to nearest mean move "mean" to center of its cluster. algorithm exploits the fact that the change of the assignment of patterns to clusters are relatively few after the first few iterations K-means algorithm with dynamic adjustment of learning rate to induce a near-optimal clustering solution in a situation where the clustered ensemble is not available.

This be done by using the

$$P_i^{(t)} = \{ x_p : \| x_p - n_i^{(t)} \|^2 \leq \| \| x_p - n_j^{(t)} \|^2$$

Where from k mean algorithm, P be the path clustered and x_i and x_j are the different circuits under the different slack values. K mean has problems when clusters are of differing Sizes, by using the above clustered mean this be formulated. Many applications for clustering algorithms, particularly applications in data mining, usually required algorithms to work on massive data sets with an acceptable speed. We analyze the algorithm into communication steps and computation steps. Densities Non-globular shapes so arrange all this in proper. The dataset is partitioned into K clusters and the data points are randomly assigned to the clusters resulting in clusters that have roughly the same number of data points. For each data point: Calculate the distance from the data point to each cluster.

If the data point is closest to its own cluster, leave it where it is. If the data point is not closest to its own cluster, move it into the closest cluster. Repeat the above step until a complete pass through all the data points results in no data point moving from one cluster to another. At this point the clusters are stable and the clustering process ends. The choice of initial partition can greatly affect the final clusters that result, in terms of inter-cluster and intracluster distances and cohesion. Advantage With a large number of variables, K-Means may be computationally faster than hierarchical clustering (if K is small).K-Means may produce tighter clusters than hierarchical clustering, especially if the clusters are globular. K means algorithm is totally framed into a Verilog program component with a different circuit elements and the program is simulated to find the different clusters enabled with it.

Using the k means algorithm same slack value circuits are grouped into same clustered. Paths are identified using a previous proposed method using a path clustering by clock control strategy. Time complexity of the exiting method is reduced and paths are identified easily using a proposed algorithm.

We generate an acyclic graph from the grouped algorithm. So that these are modified, according to the timing constraint. Timing analysis needs to be performed on the structural net list generated after technology mapping using a K means algorithm. Timing analysis will identify slacks of various nodes in the circuit and the cumulative slacks on the various circuit paths. We chose to do timing analysis outside of the system tools so that we have more freedom to use our own definition in the delay annotation of the circuit for further analysis.

Peak power, RMS current is the main concept to be reduced in the proposed method. These values are calculated using a peak power formula. These are clustered into groups as like Verilog coding. Respective values are given to the voltage and current.

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Delay value with each primary input are identified that our clustering algorithm only has to operate on the inputs to assign a timing value for all the paths connected to it. Since the timing for the primary input correlates with all the connected paths, we must make sure that we account for the worst case timing value.

These clusters from the inputs are again re clustered and predicted as values. These designed structured are tested using a different structures. Bench mark circuits are plotted in a Cadence virtuoso and this algorithm is applies at the input end and output margin is measured. For the better performance of the operation the proposed algorithm is applied in a newly designed processor and comparison are seen from the existing methods.

Algorithm for k means clustering:
Algorithm formula for calculating the paths:

$$S_i^{(t)} = \{x_p : \|x_p - m_i^{(t)}\|^2 \leq \|x_p - m_j^{(t)}\|^2 \forall 1 \leq j \leq k\}$$

1. Cluster the primary input based on maximum delay in the input delay.
2. Assign each observation to the cluster whose mean yields the least within-cluster sum of squares
3. Find the number of nodes associated with the cluster
4. assign each point to nearest mean
5. move “mean” to center of its cluster.
6. K-means has problems when clusters are of differing Sizes – Densities Non-globular shapes so arrange all this in proper
7. The dataset is partitioned into K clusters and the data points are randomly assigned to the clusters resulting in clusters that have roughly the same number of data points.
8. For each data point: Calculate the distance from the data point to each cluster. If the data point is closest to its own cluster, leave it where it is. If the data point is not closest to its own cluster, move it into the closest cluster.
9. Repeat the above step until a complete pass through all the data points results in no data point moving from one cluster to another. At this point the clusters are stable and the clustering process ends.
10. The choice of initial partition can greatly affect the final clusters that result, in terms of inter-cluster and intra cluster distances and cohesion.

Advantages of our proposed algorithm

- With a large number of variables, K-Means may be computationally faster than hierarchical clustering (if K is small).
- K-Means may produce tighter clusters than hierarchical clustering, especially if the clusters are globular.

4. PERFORMANCE EVALUATION

The performance of proposed method is to be evaluated with Cadence Virtuoso Tool. Experimental results will be performed to achieve reduced peak power and high reduction in a RMS current than previous methods. Clocking is used with different strategies, according to the different clocking stages for the proposed method. The dissipation of power which occurs during the active mode of the circuit is active power. This active power consists of dynamic power as well as the static power so it is being named as an active power. It is measured by giving input vectors to the circuit and then calculating the average power dissipation and then comparing the result with the base adder i.e. conventional 1-bit CMOS full adder.

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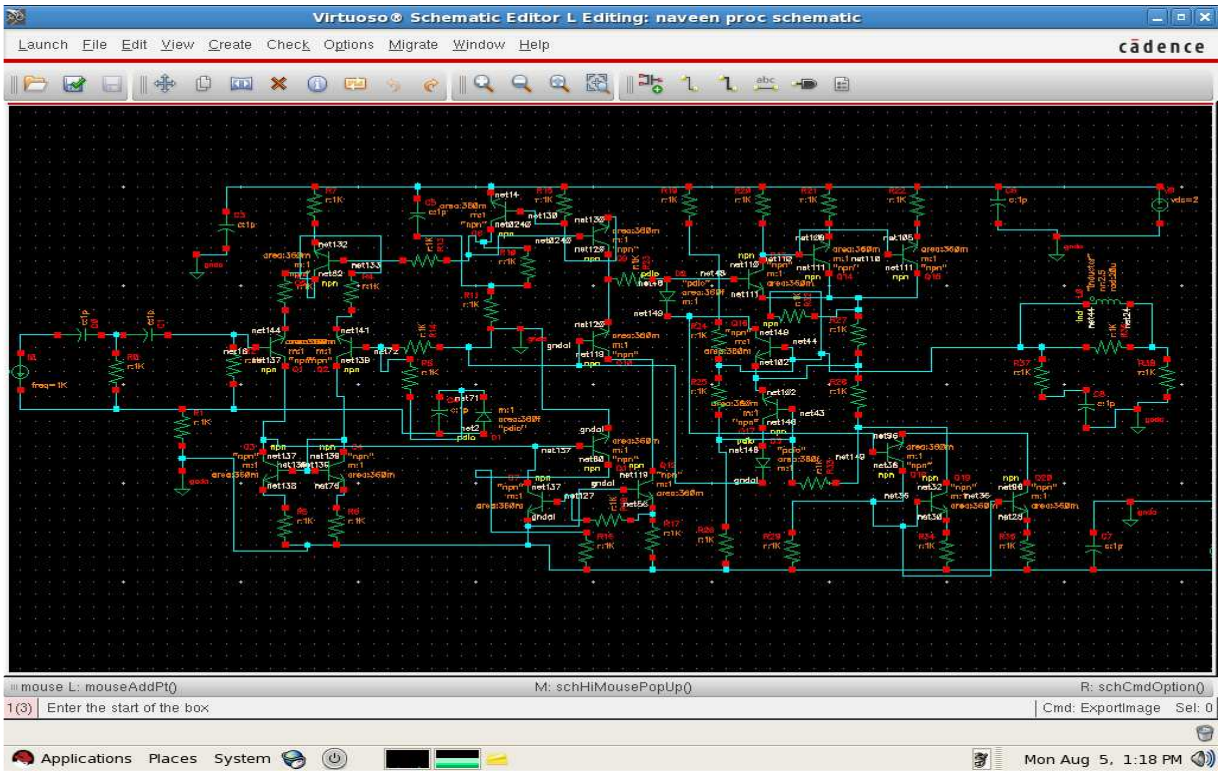
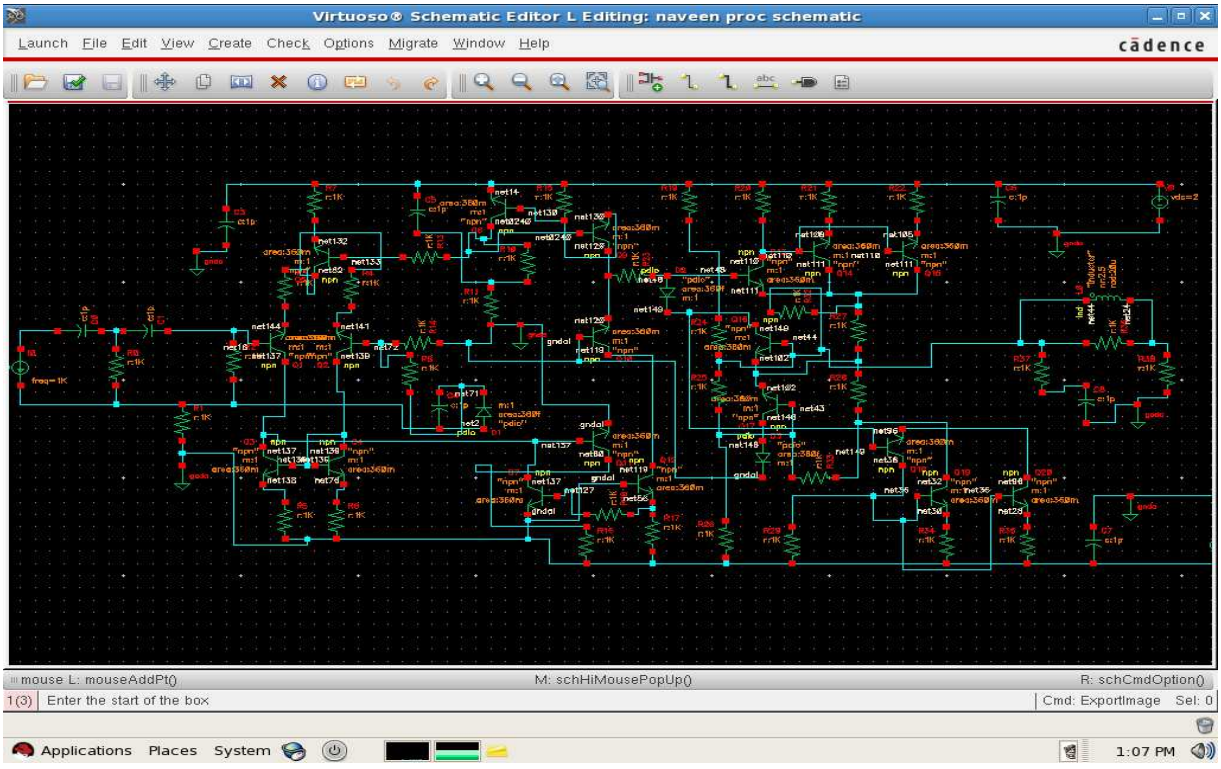


OUTPUT WAVEFORM OF TRANSIENT RESPONSE:



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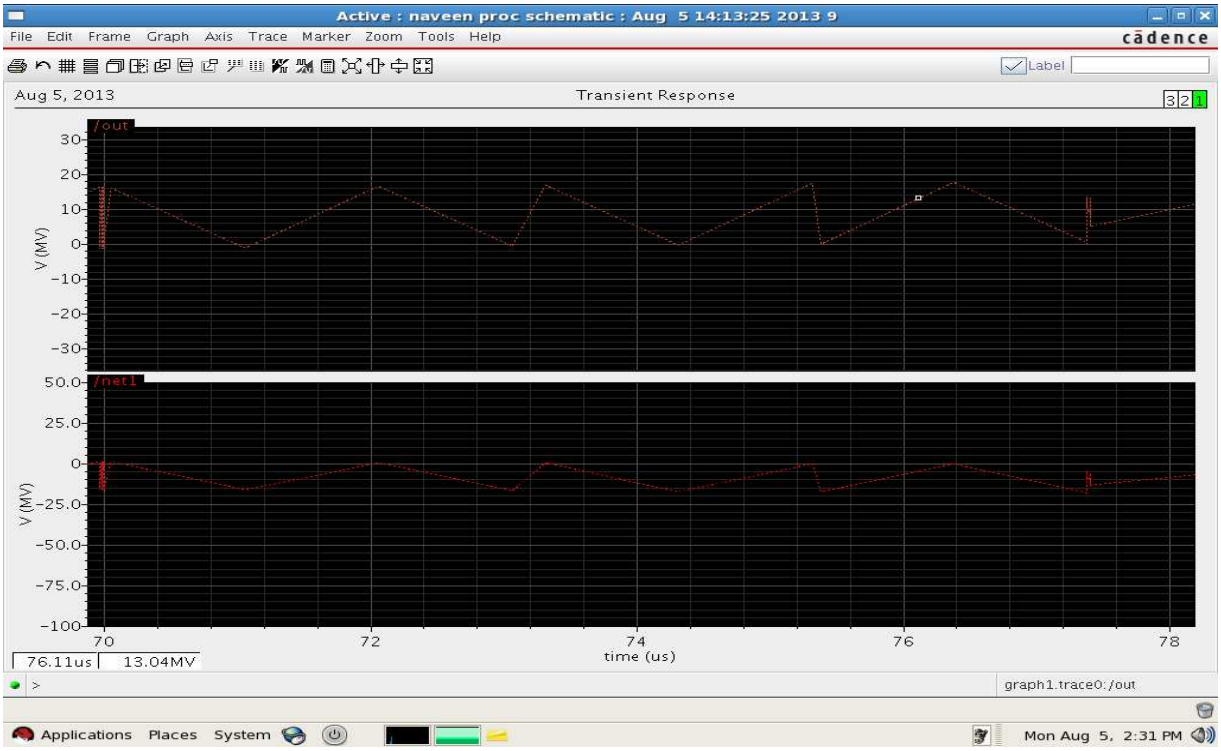
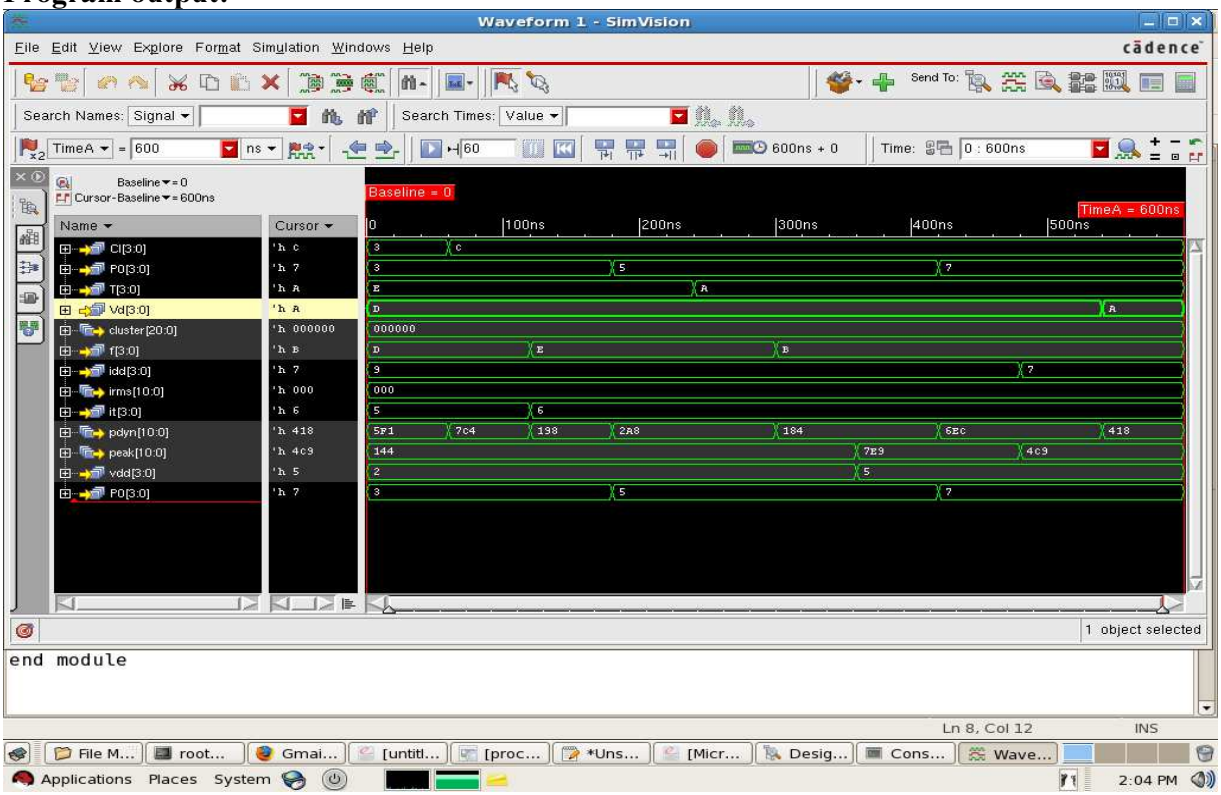


Program output:



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5.CONCLUSION

In the proposed method, CMOS full adder is designed to reduce RMS current reduction. Bur in pervious studies, there is some difficulty in finding slack delay and rms current. In our CCSCM method, both time violation and logic failures are reduced. 16 Mbit SRAMs with a 5.59 mm2 6-T cell size have been built on this technology as a yield and reliability test vehicle.

5.CONCLUSION

In the proposed method, CMOS full adder is designed to reduce RMS current reduction. Bur in pervious studies, there is some difficulty in finding slack delay and rms current. In our CCSCM method, both time violation and logic failures are reduced. 16 Mbit SRAMs with a 5.59 mm2 6-T cell size have been built on this technology as a yield and reliability test vehicle.

REFERENCES:

[1] Yow-Tyng Nieh, Shih-Hsu Huang and Sheng-Yu Hsu, "Minimizing Peak Current via Opposite-Phase Clock Tree", *Proceedings of the 42nd annual Design Automation Conference, ACM digital library*, 2005, pp.182-185.

[2] M. Ester, H. Kriegel, J. Sander, and X. Xu. A Density- Based Algorithm for Discovering Clusters in Large Spatial Databases with Noise. Proc. of the 2nd *Int'l Conf. on Knowledge Discovery and Data Mining*, August 1996.

[3] M. Bellos, D. Bakalis, D. Nikolos and X. Kavousianos, "vector epetition and modification for peak power reduction in vlsi testing", *IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems,* 2005, pp.160-165.

[4] WaiChing Douglas Lam, ChengKok Koh and ChungWen Albert Tsao, "Power Supply Noise Suppression via Clock Skew Scheduling", *International Symposium on Quality Electronic Design*, 2002, pp.1-6.

[5] Inderjit S. Dhillon and Dharmendra S. Modha, "A Data-Clustering Algorithm on Distributed Memory Multiprocessors", *Springer*, 2002, pp.245-260.

[6] Paul S. Bradley Usama M. Fayyad Cory A. Reina, "Scaling Clustering Algorithms to Large Databases", *American Association for Artificial Intelligence*, Microsoft Research, 1998, pp.1-7.

[7] Saraju P. Mohanty, N. Ranganathan and Sunil K. Chappidi, " Simultaneous Peak and Average Power Minimization during Datapath Scheduling for DSP Processors", *ACM digital library*, 2003, pp.1-6.

[8] Hyman, R, Ranganathan, N, Bingel, T. and Tran Vo, D., "A Clock Control Strategy for Peak Power and RMS Current Reduction Using Path Clustering", *IEEE Transactions on Very large Integration Systems*, Vol.21, Issue 2, 2013, pp.259-269.