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VLSI ARCHITECTURE OF DUAL STANDARD INTERLEAVER FOR TURBO CODES

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ABSTRACT

The superior error correcting performance of turbo codes is associated with the suitable interleaver design. The primary function of the interleaver is to improve the distance properties of the concatenated coding schemes and to disperse the sequence of bits in a bit stream so as to minimize the effect of burst errors introduced in the transmission. The key focus of the proposed work is to design an architecture with minimal hardware complexity and maximum reusable interleaver that can support two standards 3GPP WCDMA and 3GPP LTE. The proposed interleaver/ deinterleaver architecture receives an input data stream of any size established by the 3GPP standard and delivers the interleaved or deinterleaved stream depending on the user requirements. Various optimization techniques and novel VLSI architectures are utilized to achieve the proposed hardware interleaver address generation architecture. By introducing the algorithmic level transformations and hardware reuse methodology low complexity reconfigurable architecture is designed. The frequency of operation of the proposed interleaver is 122.46 MHz.

Keywords: *3GPP, Interleaver, Reconfigurable, LTE*

1. INTRODUCTION

Nowadays Communication systems have been growing and developing very quickly. Due to rapid advancements and changes in radio communication systems, there is always a need of flexible and general purpose solutions for processing the data. One of the challenging areas is the provision of flexible subsystems for forward error correction (FEC). FEC subsystems can further be divided in two categories, channel coding/decoding and interleaving / de-interleaving. Among these categories, Interleavers and De-interleavers appeared to be more silicon consuming due to the silicon cost of the permutation tables used in conventional approaches. Hence the importance of hardware reuse [1] of FEC modules for low silicon costs is therefore realized.

The newly evolved "3rd Generation Partnership Project (3GPP), Long Term Evolution (3GPP LTE) [2] represents a major advance in cellular technology. LTE is designed to meet carrier needs for high-speed data and media transport as well as high-capacity voice support well into the next decade. WCDMA technology has emerged as the most widely adopted third generation air interface. The WCDMA specification has been created in 3GPP, which is the joint standardization project from Europe, Japan, Korea, USA and China. Within 3GPP, WCDMA [3] is called UTRA (Universal Terrestrial Radio Access), FDD (Frequency Division Duplex) and TDD (Time Division Duplex), the name WCDMA being used to cover both FDD and TDD operation. And both standards use turbo codes for forward error correction.

Turbo Codes [4] are parallel or serial concatenations of simple good convolutional codes with significant interleaving to distribute the error events of the two codes with respect to one another was first discovered by Claude Berrou in 1993. Its superior performance in burst error correction over convolutional coders is heavily related to recursive

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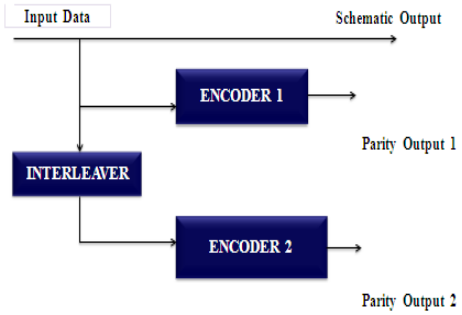
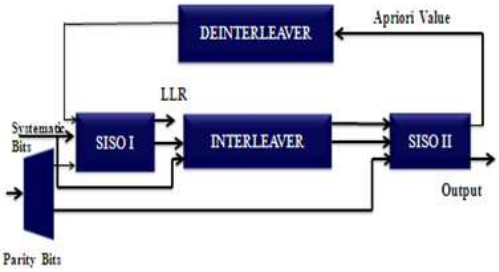
encoding, iterative decoding and the use of interleavers. The simplified schematic of the turbo encoder and decoder are shown in figure1.

There are two convolutional encoders in parallel, which are usually taken to be identical. Information bits are interleaved before being fed to the second encoder. The codeword in a turbo code consists of a frame of input bits followed by the parity check bits from the first encoder then the parity bits from the second encoder.



(a)



(b)

Figure 1 Turbo Encoder And Decoder

Each of the constituent encoders presents a parity sequence at its output. Padding is used to append the proper sequence of bits in order to force all the encoders at the end of the frame to the all zero state. The decoder works in an iterative way. The first decoder will decode the sequence and pass the hard decision together with a reliability estimate of this decision to the next decoder after proper interleaving.The second decoder will utilize the reliability estimates produced by the first encoder, and thus will have extra information for decoding. After a certain number of iterations are executed, a hard decision is made and the estimated sequence is delivered to the user.

Telecommunication Standards suchas 3GPP WCDMA and LTE have different interleaver structure. But in the proposed work, a single low cost hardware module of interleaver / de-interleaver is designed which is suitable for both the standards.

2. SYSTEM MODEL AND SPECIFICATIONS

A. 3GPP WCDMA Interleaver Design

According to the 3GPP WCDMA standard [3], the interleaver address generation algorithm for turbo coding and decoding can be summarized as below. In this algorithm the input bits feed a rectangular matrix and then some permutations are performed where i, j are the indexing variables for row and column starting from 0, top to bottom and left to right respectively.The algorithm is as follows.

1. Block size: K is the integer number of input bits and takes a value from 40 to 5114.

2. Determine the number of rows R of the rectangular matrix such that
   R=5; if (40<K<159)
   R=10; if((160<K<200)or(481<K<530)) R=20; if (k=any other value)
   where rows are numbered form 0 to R-1.

3.Determine the prime number p to be used in intra row permutations and the number of columns C of the rectangular matrix as
   If (481<K<530) then p=53 and C=p else
   Find the minimum prime number p such that K < (R(p-1)) and determine C such that
   C=p-1; if K<(R(p-1))
   C=p; if R(p-1)<K<(R*p)
   C=p+1; if (R*p)<K
   For every prime number p there exists a primitive root v in table(1) in [2]

4. Construct the base sequence S (j) for intra row permutation such that
   S(j)=(v*S(j-1))mod(p) and S(0)=1 where j=1,2,…,(p-2).

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Table 1 List Of Prime Number 'P' And Associated Primitive Root 'V'

p	v	p	v	p	v	p	v	p	v
7	3	47	5	101	2	157	5	223	3
11	2	53	2	103	5	163	2	227	2
13	2	59	2	107	2	167	5	229	6
17	3	61	2	109	6	173	2	233	3
19	2	67	2	113	3	179	2	239	7
23	5	71	7	127	3	181	2	241	7
29	2	73	5	131	2	191	19	251	6
31	3	79	3	137	3	193	5	257	3
37	2	83	2	139	2	197	2		
41	6	89	3	149	2	199	3		
43	3	97	5	151	6	211	2		

5. Determine the prime integers in the sequence q(i) such that g.c.d(q,p-1)=1,q(i)>6 and q(i) > q(i-1) for i=1,2,…..R-1.

6. Permute the sequence q(i) to make the sequence r(i) such that r(i)=T(q(i)), i=0,1,…,R-1.where T(i) is a simple indexing transform. It is defined by the standard and shown in table 2.

Table 2 Inter-row permutation patterns for Turbo Code Internal Interleaver

Number of input bits K	No. of Rows R	Inter-row permutation patterns < T(0),T(1),……T(R-1) >
(40 < K < 159)	5	< 4,3,2,1,0 >
(160 < K < 200) or(481 < K < 530)	10	< 9,8,7,6,5,4,3,2,1 >
(2281 ≤ K ≤ 2840) or(3161 ≤ K ≤ 3210)	20	<19,914,4,0,2,5,7,12,18, 16,13,17,15,3,1,6,11,8,1 0 >
K = any other value	20	<19,9,14,4,0,2,5,7,12,18, 10,8,13,17,3,1,16,6,15,1 1 >

7. Perform the intra row permutation which is denoted by
If (C=p), U(i,j)=S[(j*r(i))mod(p-1)]
where U(i,p-1)=0
If (C=p+1), U(i,j)=S[(j*r(i)mod(p-1)]
where U(i,p-1)=0; and U(i,p)=p
And If (K=R*C) then exchange U(R-1,0) with U(R-1,p)
If (C=p-1), U(I,j)=S[(j*r(i))mod(p-1)]-1 where i=0,1,…,R-1 and j=0,1,..,p-2.

8. Perform the inter row permutation for the rectangular matrix based on the pattern T(i). It is denoted as U(i)
U(i)=U(T(i)), where i=0,1,..,R-1.

9. Read out the addresses column wise.

From the algorithm explained above, to reduce the hardware usage, some of the complex functions are implemented using the support from ROM, while the others are simplified.

B. 3GPP LTE simplifications and hardware

Directly implementing the permutation polynomial in [2] causes hardware inefficient due to numerous multiplications and a complex modulo function. Hence some simplifications are made in the algorithmic level [11], to effectively use the hardware.For recursive computation the permutation polynomial is modified as,

$$f(x+1) = [f_1 * (x+1) + f_2 * (x+1)^2] \bmod K$$
$$f(x+1) = [f(x) + (f_1 + f_2 + 2 * f_2 * x)] \bmod K$$
$$f(x+1) = [f(x) + g(x)] \bmod K \quad (1)$$
$$g(x+1) = [f_1 + f_2 + 2 * f_2 * (x+1)] \bmod K$$
$$g(x+1) = [g(x) + 2 * f_2] \bmod K \quad (2)$$

Looking on to the hardware utilization the values of g(0),f_1 and f_2 are placed in a lookup table, addressed by block size. The terms *f(x+1)* and *g(x+1)* mentioned in equations (1) and (2) can be computed recursively by just using the adders and comparison. The computation of interleaving address is done every clock cycle and there is no latency.

3. MODES OF COMPUTATION

The interleaving process can be easily separated into two main modes.

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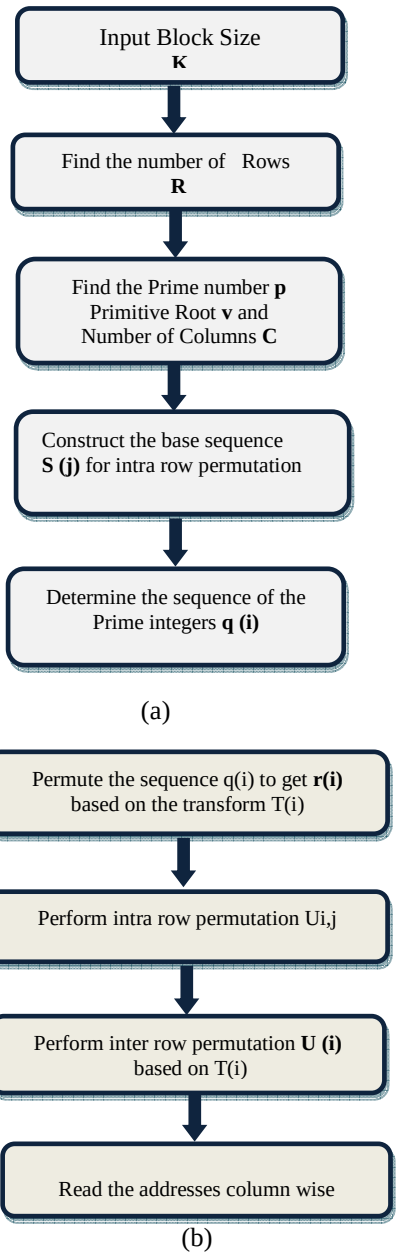

Figure 2 Flow Graph For Precomputation Mode And Execution Mode

A. Precomputation mode

Precomputation mode involves the computation of various parameters required for the interleaving process. It has to be performed each time the change in the block size occurs, that means for a fixed block size *K*, these operations have to be performed only once. This mode computes the number or rows *(R)*, number of columns *(C)* , prime number *(p)*, primitive root *(v)*, the base sequence for intra row permutations *(S(j))*, the sequence of minimum prime integers *q(i)* and the permuted prime integers *r(i)*. The computations performed in this phase are depicted in the flow graph shown in figure 2a.But the parameters needed for 3GPP-LTE are only f_2 and *g(0)*, which are taken from the lookup table, so parameter computation is not needed for LTE in the precomputation mode.

B. Run mode

Run mode calculates the intra row permutations *Ui,j*, and the interleaved address *i_addr* , where write or read operation of data bits can be taken place, depending upon whether interleaving or de-interleaving is performed. The run mode is performed for each data block. The operation of this mode is shown as a flow graph in the figure 2b.

4. COMPUTATION OF PARAMETERS

Multiplication, addition and comparison are needed for the computation of *p* and C, and these blocks are shown in figure 3 which is multiplexed to serve in precomputation mode as well as in execution mode for 3GPP WCDMA and LTE.

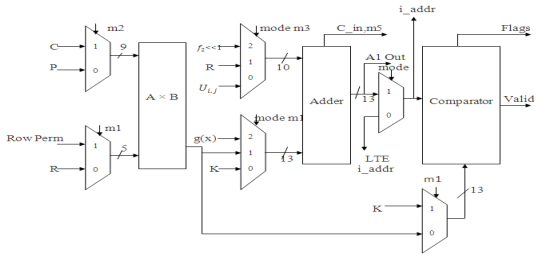

Figure 3 Multiplexed Block Of Multiplication, Addition And Comparison

Using the Interleaved Modulo Multiplication Algorithm [12] depicted in figure 4, the modulo function *[S(j-1)*v mod P]*, for intra-row permutation pattern is computed iteratively. The computation of *S(j)* values required three adders which can further be multiplexed. The first adder is used to compute *q mod (p-1)* and the remaining two adders are used to compute the RAM address recursively in run time.

During the pre-computation phase, the RAM write address is linear, and it is generated by the controller. The output *ModuloOut* is used as the data out for RAM during pre-computation phase, whereas it serves as the RAM read address during

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run time. After computing the *S(j)* values, these are stored in a RAM of size 256×8 bit. The controller is set in '*RUN*' state after completing the pre-computation phase or looking at the input mode (i.e. WCDMA/LTE), and the hardware is configured to perform run time computations for the generation of the interleaved addresses. The recursive function used to compute the RAM address and multiply-add function to compute the final interleaved address are as follows:

$$RamAdr(i,j) = (Ram\_Adr(i,j-1)+Q_{mod}(i)) \ mod \ (p-1) \quad (3)$$

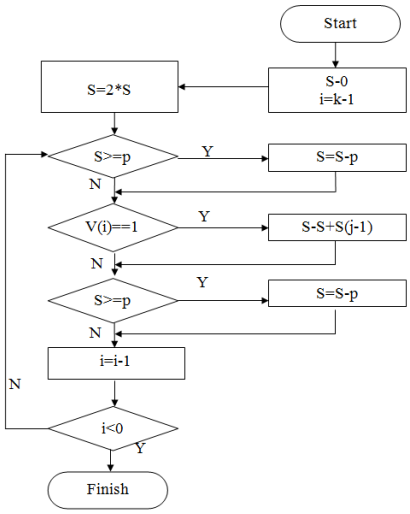

Figure 4 Interleaved Modulo Multiplication Algorithm

It can be seen that computing the RAM address using Q_{mod}=*q mod (p-1)* instead of *q*, helps to avoid the full computation of modulo multiplication. After computing the RAM address, the final interleaved address is computed by the following multiply-add function

$$i\_addr = (C \times Row\_Perm)+U(i,j) \quad (4)$$

Where *U*(*i*, *j*) is the intra row permutation coming from RAM. The final interleaved address is tagged valid or invalid using the comparator. This is called pruning of the interleaver and is needed for the case when interleaver block size is not exactly equal to *R*×*C*.

There exist some exceptions as well in the WCDMA algorithm which are listed below:

If (C=p) : $U_{i,(p-1)} = 0$;

If (C=p+1): $U_{i,(p-1)} = 0$; $U_{i,p} = p$;

and if (K=R×C) then exchange $U_{(R-1,0)}$ *with* $U_{(R-1,p)}$ (5)

Some flags related to first and last row and column are generated from row and column counters. Using these flags along with a couple of multiplexers a very small logic is needed to serve the purpose of exception handling. For the computation of the interleaver address for 3GPP LTE systems, the same hardware structure is used after getting the mode input as LTE [1'*b*0]. The controller jumps in to '*RUN*' state directly, and with a small difference of configuration vectors the same hardware is mapped to the hardware for computation of interleaver address for LTE. From the complete hardware block to compute the interleaved address in a multiplexed way for 3GPP WCDMA and 3GPP LTE, it can be seen that all the vital computing parts are being shared by the two standards which provides an illustration of the hardware reuse to get the low cost solution for multiple applications.

5. THE PROPOSED MULTIPLEXED INTERLEAVER ARCHITECTURE

The complete block diagram for the proposed multiplexed interleaver supporting two standards 3GPP WCDMA and LTE is shown in figure 5.

Based on the input mode the controller switches between WCDMA or LTE. For a input *K_Size*, if the mode is WCDMA (mode = 0), the controller executes the precomputation phase of the interleaved address generation, i.e., number of rows *R*, number of columns *C*, least prime number sequence *q(i)*, inter-row permutation pattern *T(i)*, prime number *p* and associated integer *v* are computed. In addition the intra-row permutation pattern *S* (*j*) is also computed in the precomputation phase and placed in a RAM. Or if the input mode is LTE (mode = 1), the controller directly jumps to execution mode of interleaved address generation for which the parameters f_2 and g(x) are taken from the lookup table. And then in the multiple computation block the interleaved address is

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generated for both WCDMA and LTE. Operation of each module is explained in following sections.

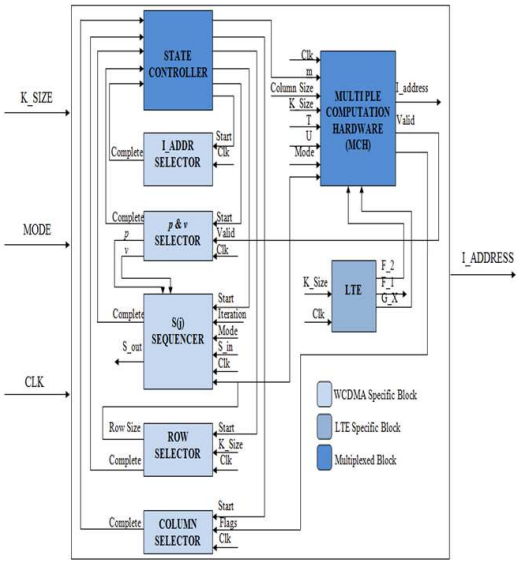

Figure 5 Complete Multiplexed Interleaver Design

A. Intra row permutation sequence s(j)

An important block in this architecture is Modulo Computation that performs modulo computation and also writes the base sequence for intra row permutations in a RAM. Flow chart depicting the operation of $S(j)$ sequencer is given in figure 6.

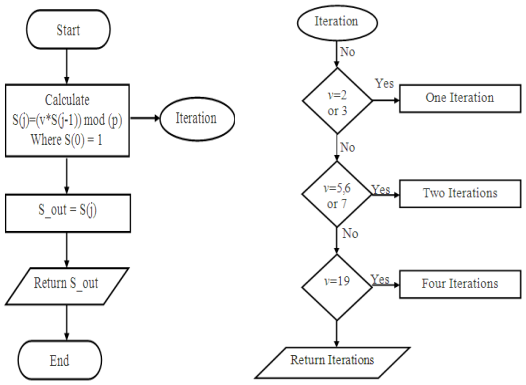

Figure 6 Flow Chart For S(J) Sequencer

This unit plays a crucial role in run time mode for computing the sequence of prime integers. It is also performed in precomputation mode for determining the base sequence $S(j)$ for intra row permutations. An iterative numerical algorithm based on additions, shift, comparison and bit retrieval is employed. This architecture enables the calculation and writing of every $S(j)$ in a RAM in atmost four clock cycles. The number of cycles needed to calculate every $S(j)$ depends upon v, which can take only 6 different values of 2,3,5,6,7 and 19. For v = 2 & 3, only one iteration, for v= 5, 6 & 7, only 2 iterations, and for v = 19, 4 are needed. Thus the complexity in iterative modulo computation is reduced by reducing the number of iterations.

B. State Controller

The heart of the proposed reconfigurable architecture of interleaver is the controller. The designed architecture provides a high degree of flexibility for a large range of input block sizes. The controller unit generates all the control signals to synchronize every block in this architecture. When the block size (K) is applied as the input, the controller performs the calculation of number of rows (R), number of columns (C), the prime number (p) and the primitive root (v). Thus it facilitates a quick change in block size and precomputation parameters without much delay.

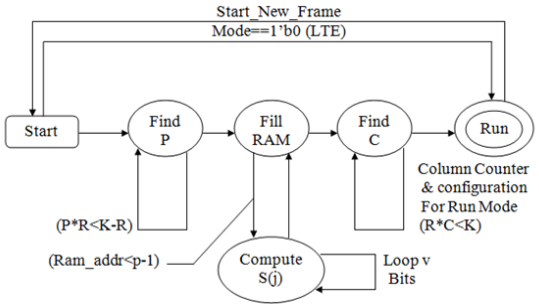

Figure 7 Control FSM Of WCDMA And LTE Interleaver

The state diagram of the controller for the proposed design is shown in figure 7. For 3GPP-LTE standard, the controller checks the mode and directly jumps in to the 'execution' state. When the controller is in the execution mode, the new frame and the new precomputation can always be initiated by just changing the block size K and the start signal. For 3GPP WCDMA standard all the precomputation parameters are computed and then jumps in to the 'execution' state.

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C. LTE module

LTE module holds the look up table having values of f_1 and f_2 corresponding to different *K* sizes indexed with a variable *i*. Using the values from the look up table, this module generates an address when mode is 1 (LTE) as given in figure 8a.

D. Multiple computation block

Multiple computation block generates the interleaved address for both 3GPP WCDMA and LTE using the algorithmic simplifications made in previous sections. In addition it generates the valid bit and flags which are used for prime value (*p*) and column size (*c*) selection. It is controlled by the flags (m1 to m5) generated from the controller unit. The operation is explained in the flow chart in figure 8b.

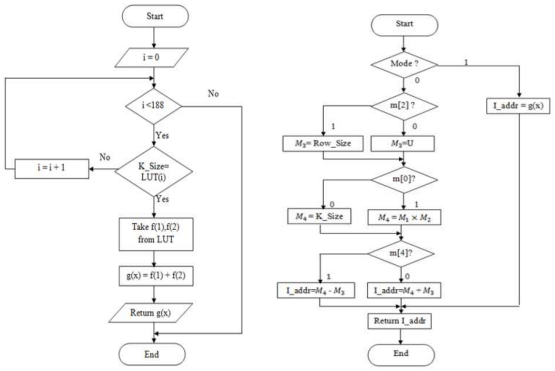

Figure 8 Flow Chart For LTE Module And Multiple Computation Block

6. PERFORMANCE ANALYSIS OF THE PROPOSED WORK

The RTL code for the proposed multiplexed interleaver design for turbo coded system supporting two standards such as 3GPP WCDMA and 3GPP LTE is written using verilog. The verilog coding is then synthesized and simulated to check the correctness of the design using Xilinx ISE 9.1i. The timing analysis of the work is carried out in Altera Quartus II 9.0

Table 3 shows the comparison of hardware usage by various modules. From the table, it is observed that modulo computation requires the use of adder to be the common computing element for all kinds of implementations. Further it shows that the computational part of the reconfigurable design can be restricted to have 10 additions, 1 multiplication, and 10 comparisons. Figure 9 provides a chart comparing the hardware usage of various modules of the architecture.

Table 3 Comparison Of Hardware Usage By Various Modules

Modules	Row Selector	*p & v* Selector	S(j) Sequencer	Column Selector	Controller	MCH	LTE
Adders / Subtractors	-	-	3	-	-	1	6
Comparators	6	-	1	-	-	1	2
Counters	-	1	1	-	-	-	-
Flip flops	7	21	-	1	-	-	26
IOs	22	24	54	6	16	98	45
Latches	-	-	-	-	7	-	2
Multipliers	-	-	-	-	-	1	-
Registers	2	3	2	1	-	-	3

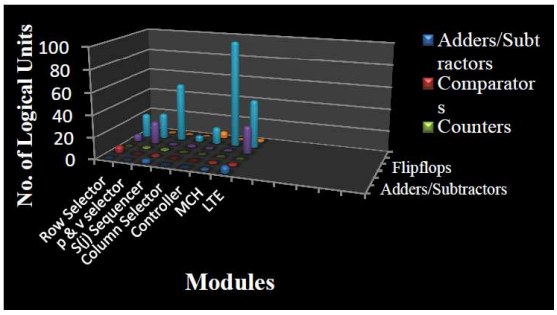

Figure 9 Hardware Usages Of Various Modules

Table 4 Memory Consumption By Various Modules

MODULES	MEMORY CONSUMPTION (Kilo Bytes)
Row Selector	120144
p&v Selector	122192
S(j) Sequence	121168
Column Selector	119120
Controller	120144
Multiple Computation Block	122192
LTE	264080

From the table 4, it is observed that the highest memory consuming module is the LTE where the look up table having values of f_1 and f_2 corresponding to different *K* size is present. Figure 10 compares the memory usage of different modules in a chart format.. From the analyzer report generated in Altera Quartus II 9.0 it is inferred that the proposed reconfigurable architecture can operate at a maximum frequency of 122.46 MHz. It is shown in figure 11. The RTL

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Schematic of the proposed dual standard interleaver is given in figure 12.

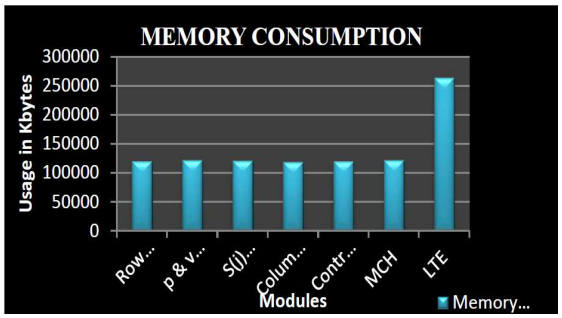

Figure 10 Memory Consumption By Various Modules

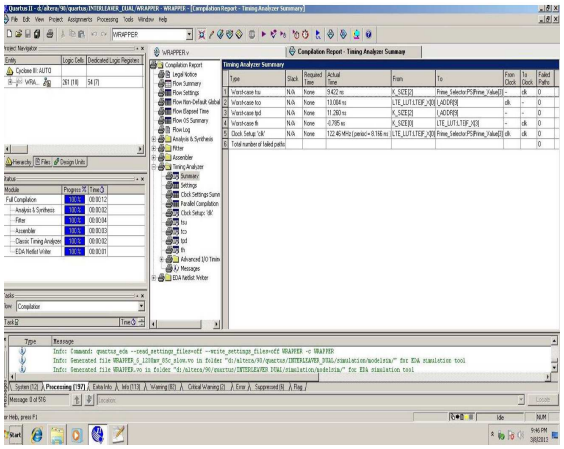

Figure 11 Snapshot Of The Timing Analyzer

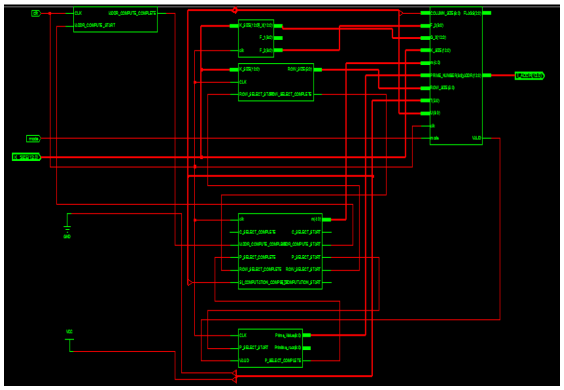

Figure 12 RTL Schematics Of The Dual Standard Interleaver Architecture

7. PERFORMANCE WITH EXISTING STATE-OF-THE-ART INTERLEAVERS

Table 5 provides the performance comparison of the proposed design to the existing interleaver designs. The total hardware consumed by the proposed design is 12K gates. The reference implementations [7], [8], [9] and [13] are single standard design. Though the silicon area needed for the proposed dual standard architecture coverage is slightly more than that of the work in [9] and [13], the proposed solution still provides a good tradeoff with an acceptable silicon cost and standards supported. Thus the design provides a very low cost dual standard design for hardware interleaver address generation for 3GPP WCDMA and 3GPP LTE.

Table 5 Performance With Existing State-Of-The-Art Interleavers

WORK	SIZE	REMARKS
ROM (All patterns)	< 100 M bit	Easily manage the data But impractical size and memory inefficient.
RAM ((big off-chip Memory required)	80 M bit	Can easily manage the data. But impractical size.
M.C.Shin and I.C Park 2003	~ 32K Gates	High Silicon area
P.Ampadu and Kornegay 2003	~ 30K Gates	No data streams
Z.Wang and Q. Li 2007	~ 4K Gates	No data streams
Rizwan Asghar and Dake Liu 2008	~ 2.2K Gates +2Kbit RAM	12% of interleaved path is failed.
Luis F.Gonzalez Perez,Fernando Landeros 2009	5000 Logical Elements ~ 100K Gates	Single Standard
J.M.Mathana and P.Rangarajan	4586 Logical Elements > 100K Gates	Single Standard Working as both interleaver and de-interleaver. It manages data streams.100% interleaved path is available.
Proposed Design	12 K Gates	Dual Standard

7. CONCLUSION

A very low cost reconfigurable hardware interleaver for two standards, 3GPP Wideband Code Division Multiple Access and 3GPP Long Term Evolution is proposed in this work, utilized the algorithmic level hardware simplifications to achieve very low cost solution. With all the features provided by this work, the reconfigurable interleaving is a step ahead towards faster time-to market solutions and rapid prototyping. In continuation to this work, further research can be done in designing a multi standard interleaver/deinterleaver which can be configured to suit several other standards like WiMAX, WLAN and DVB; therefore it can be a better candidate for many of the applications by incorporating multiple FEC algorithms and reconfigurable interleaver on to a single architecture.

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