ULTRA LOW POWER DIGITAL LOGIC CIRCUITS IN SUB-THRESHOLD FOR BIOMEDICAL APPLICATIONS

K. RAGINI [1*], DR. B.K. MADHAVI [2]

[1] Associate Professor in ECE, GNITS, Hyderabad, India, [2] Professor in ECE, Marconi Institute of Technology, Hyderabad, India.

ABSTRACT

Motivated by emerging battery operated applications that demand intensive computation in portable environments, techniques are investigated which reduce power consumption in CMOS digital circuits, by operating the devices at low currents and low voltages[1,2,3,4].It is known that MOS devices and circuits especially CMOS circuits consume relatively low power[5,6] . But there seems to be a need to reduce this power further to prolong the life of battery. One solution to achieve the ultra-power requirement is to operate in sub-threshold region [7]. Over the last 10 years, digital sub-threshold logic circuits have been developed for applications in the ultra-low power design domain, where performance is not the priority. Sub-threshold logic transistors, that is the power supply voltage is below the threshold voltage. In this paper, analysis was done both CMOS and Pseudo-NMOS logic families operating in sub-threshold region. The results were compared with CMOS in normal strong inversion region.

KEYWORDS: *Ultra low power, digital logic, sub-threshold operation, sub-threshold pseudo NMOS, Sub-threshold CMOS, Strong inversion, Weak inversion*.

INTRODUCTION

Rapid development of such portable systems as Laptops, PDAs, digital wrist watches [10], pacemakers and cell phones require low power consumption and high density Integrated Circuits. As a result there is a surge of innovative development in low power device and design techniques. In most cases, the requirements for low power consumption must meet the equally demanding goals of high chip density and high through put circuits. Hence low power digital design and digital ICS are very active fields of research and development.

In this cutting-edge technology, reduction in power dissipation is a critical task, especially as the size of transistors is scaled down to increase the transistor density over the silicon chip. Reduction in power dissipation is also an important objective in the design of digital circuits.

This paper mainly focuses on various digital circuits operating in sub threshold region for achieving ultra low power. One way to achieve this goal is by running the digital circuits in sub-threshold mode. [11,12 ,13] The incentive of operating is able to exploit the sub-threshold leakage current as the operating drive current. The sub-threshold current is exponentially related to gate voltage. This exponential relationship is expected to give an exponential reduction in power consumption, but also an exponential increase in delay. This Paper is organized as follows. In section 1, we analyze sub-threshold–CMOS circuit. Pseudo-NMOS logic is compared with CMOS circuit in Section 2. Voltage transfer characteristics (VTC) of CMOS inverter and pseudo- NMOS inverter were compared in section 3. Section 4 shows the comparison of power delay product (PDP) for both CMOS and Pseudo-NMOS logic.

APPLICATION AREAS:

MOS circuits operating in sub-threshold region are particularly suited for systems where power dissipation is a very important consideration. Inside electronic watches there is sophisticated circuitry whose operation depends on MOS sub-threshold characteristics. A typical watch to-day has about 100,000 transistors, most of them operating in sub-threshold. With an increased interest in low power devices and mobile technologies, sub-threshold MOS operation is becoming more and more important. Other devices critical to our everyday activities, such as cardiac pacemakers [8, 9] and hearing aids also use MOS transistors in sub-threshold. The sub-threshold region is particularly important for low-voltage, low-power applications, such as when the MOSFET is used as switch in digital logic and memory applications, because the sub-threshold region describes how the switch turns on and off.

1. Digital Sub-threshold logic circuits

Sub-threshold logic circuits operate with power supply V_{dd} less than transistors threshold voltage, V_t. This is done to ensure that all the transistors are indeed operating in the sub-threshold region [14,15]. We used 0.1µm technology for our circuit simulation with V_t of NMOS and PMOS transistors as 0.35V and -

0.35V. The voltage transfer characteristics of the inverter gate running in sub-threshold mode are closer to ideal compared to one in strong inversion region. The improvement is mainly caused by the increase in the circuit gain. The merits of regular CMOS logic such as excellent robustness, good noise margin and low power consumption are inherited in sub- threshold region. However, performance of sub-threshold logics becomes more sensitive to supply & process variations due to the exponential dependency of weak inversion current on Vgs and V_t.

Table 1 shows the simulation results for Inverter, 2 input NOR, 2 input NAND and 2 input XOR gates in strong inversion and sub-threshold regions respectively. Power and delay of digital logic gates in both strong inversion and sub-threshold regions were compared.

2. Pseudo-NMOS Logic:

The pseudo-NMOS logic style is particularly attractive when designing complex gates with a large fan-in. The pull up network of complementary CMOS gates is replaced by a single load transistor. In order to utilize pseudo-NMOS logic, the drawbacks of ratioed logic such as large static current consumption and degradation in static noise margin should be carefully taken into account. Pseudo-NMOS logic in sub-threshold region inherits the advantages it has in the strong inversion such as good performance and smaller area. In addition to this, the drawbacks of ratio-ed logic are relieved in sub-threshold region. This is mainly because in sub-threshold region, the drain current saturates and becomes independent of V_{ds} for V_{ds} > -3KT/q. Note that a transistor in strong inversion region only enters the saturation region when $V_{ds} > V_{gs}- V_{th}$ which gives a much narrower saturation region, and thus, an undesirable VTC.

Careful sizing of PMOS to NMOS ratio is a must. Pseudo -N MOS logic uses fewer transistors because only the NFET logic block is needed to create the logic. For N inputs, a pseudo-NMOS logic gate requires (N+1) FETS. Pseudo-NMOS logic gates like inverter, 2 input NAND, 4 input NAND and 8 input NAND are compared with pseudo-NMOS inverter, 2 input pseudo-NMOS NAND, 4 input pseudo-NMOS NAND and 8 input pseudo-NMOS NAND gates both in weak inversion and strong inversion region respectively in Table 2.

Pseudo-NMOS logic in the sub-threshold region will have the advantage of smaller area and good performance, when compared to CMOS logic. Sub-threshold pseudo-NMOS is also efficient as sub-threshold CMOS in terms of power delay product (PDP). But PDP is much worse when we go to strong inversion of pseudo-NMOS, because of large static power dissipation when operated at regular 1V supply voltage.

The reason behind the lower PDP in sub pseudo-NMOS is the smaller delay and relatively small short circuit current in sub-threshold region. In the strong inversion region, the static power consumption was due to transistor on – current, which is orders of magnitude larger than off current. In the sub-threshold region, however the short circuit current is also weak inversion current which is relatively much less significant. Pseudo-NMOS NAND logic is compared with pseudo-NMOS NOR logic in Table 3 both at strong inversion and weak inversion region. From Table 3 we can observe that PDP is much worse than for pseudo-NMOS NOR logic in strong inversion, when compared with PDP of pseudo-NMOS NAND logic.

Table 1 Power and Delay comparison of digital CMOS logic for strong inversion region(1V) and weak inversion region(0.3V)

	V_{dd}	**Power**	**Delay**	**PDP**
Inverter	1V	1.343 µw	t_{PLH}= 5ps t_{PHL}= 7ps	8.058×10^{-18}J
	0.3 V	0.296 µw	t_{PLH}= 0.1ns t_{PHL}= 0.1ns	0.029×10^{-15}J
NAND 2 input	1 V	1.563 µw	t_{PLH}= 4ps t_{PHL}= 13ps	13.285×10^{-18}J
	0.3 V	0.276 µw	t_{PLH}= 0.18ns t_{PHL}= 0.4ns	0.01×10^{-15}J
NOR 2 input	1 V	1.236 µw	t_{PLH}= 12ps t_{PHL}= 8ps	12.36×10^{-18}J
	0.3V	0.292 µw	t_{PLH}= 0.3ns t_{PHL}= 0.5ns	0.116×10^{-15}J
XOR 2 input	1V	7.212 µw	t_{PLH}= 1021ps t_{PHL}= 1041ps	7435.57×10^{-18}J
	0.3V	1.674 µw	t_{PLH}= 0.18ns t_{PHL}= 0.2ns	0.318×10^{-15}J

Table 2. Power and Delay comparison of CMOS logic and Pseudo-NMOS logic for strong inversion region (1V) and weak inversion region(0.3V)

	CMOS					Pseudo-N MOS		
	V_{dd}	Power	Delay	PDP	V_{dd}	Power	Delay	PDP
Inverter	0.3V 1V	0.296µw 1.343µw	t_{PLH}=0.1ns t_{PHL}=0.1ns t_{PLH}=5ps t_{PHL}=7ps	0.029×10^{-15}J 8.058×10^{-18}J	0.3V 1V	P=0.190 µw P=40.368µw	t_{PLH}=0.4ns t_{PHL}=0.1ns t_{PLH}=8ps t_{PHL}=5ps	0.047×10^{-15}J 262.392×10^{-18}J
NAND 2 input	0.3V 1V	0.276 µw 1.563 µw	t_{PLH}=0.18ns t_{PHL}=0.4ns t_{PLH}=4ps t_{PHL}=13ps	0.08×10^{-15}J 13.285×10^{-18}J	0.3V 1V	P=0.36 µw P=14.755 µw	t_{PLH}=0.45ns t_{PHL}=0.2ns t_{PLH}=6ps t_{PHL}=8ps	0.117×10^{-15}J 103.285×10^{-18}J
NAND 4 input	0.3V 1V	0.123 µw 0.638 µw	t_{PLH}=0.4ns t_{PHL}=0.8ns t_{PLH}=12ps t_{PHL}=19ps	0.073×10^{-15}J 9.889×10^{-18}J	0.3V 1V	P=0.093 µw P=4.188 µw	t_{PLH}=0.2ns t_{PHL}=0.7ns t_{PLH}=5ps t_{PHL}=2ps	0.041×10^{-15}J 14.658×10^{-18}J
NAND 8 input	0.3V 1V	0.131 µw 1.464 µw	t_{PLH}=0.2ns t_{PHL}=0.7ns t_{PLH}=18ps t_{PHL}=53ps	0.058×10^{-15}J 51.972×10^{-18}J	0.3V 1V	P=0.263 µw P=19.728 µw	t_{PLH}=0.6ns t_{PHL}=0.3ns t_{PLH}=4ps t_{PHL}=13ps	0.118×10^{-15}J 167.68×10^{-18}J

Table 3. Power and Delay comparison of Pseudo-NMOS NAND logic and Pseudo-NMOS NOR logic for strong inversion region(1V) and weak inversion region(0.3V)

	Pseudo-NMOS NAND					Pseudo-NMOS NOR			
	V_{dd}	Power	Delay	PDP		V_{dd}	Power	Delay	PDP
NAND 2	0.3V	0.360µw	t_{PLH}=0.45ns t_{PHL}=0.2ns	0.117×10^{-15}J	NOR 2	0.3V	0.202µw	t_{PLH}=0.8ns t_{PHL}=0.25ns	0.106×10^{-15}J
	1 V	14.755µw	t_{PLH}=6ps t_{PHL}=8ps	103.28×10^{-18}J		I V	40.923µw	t_{PLH}=15ps t_{PHL}=4ps	388.76×10^{-18}J
NAND 4	0.3V	0.093µw	t_{PLH}=0.2ns t_{PHL}=0.7ns	0.041×10^{-15}J	NOR 4	0.3V	1.074µw	t_{PLH}=0.7ns t_{PHL}=0.15ns	0.456×10^{-15}J
	1 V	4.188µw	t_{PLH}=5ps t_{PHL}=2ps	14.658×10^{-18}J		1 V	60.604µw	t_{PLH}=25ps t_{PHL}=20ps	$1,363.5\times10^{-18}$J
NANS 8	0.3V	0.263µw	t_{PLH}=0.6ns t_{PHL}=0.3ns	0.118×10^{-15}J	NOR 8	0.3V	1.094µw	t_{PLH}=0.8ns t_{PHL}=0.1ns	0.49×10^{-15}J
	1 V	19.728µw	t_{PLH}=4ps t_{PHL}=13ps	167.68×10^{-18}J		1 V	61.505µw	t_{PLH}=40ps t_{PHL}=20ps	$1,845\times10^{-18}$J

3. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS INVERTER:

Voltage versus Time graph and VTC characteristics of CMOS inverter both at strong inversion (1V) and Sub-threshold region (0.3V) are shown in Fig 1, Fig 2, Fig 3 and Fig 4. The VTC of CMOS Inverter gate running in sub-threshold mode which is shown in Fig 4 was closer to ideal compared to one in strong inversion region shown in Fig 2. It has a good Noise-margin.

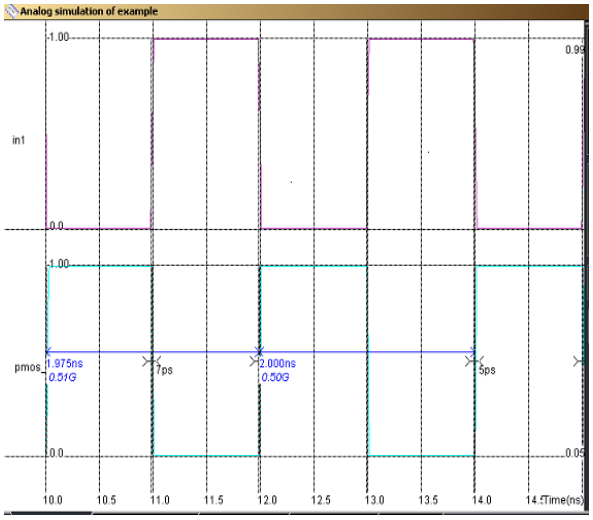


Fig 1.Voltage vs Time graph for CMOS inverter at V_{dd}= 1V

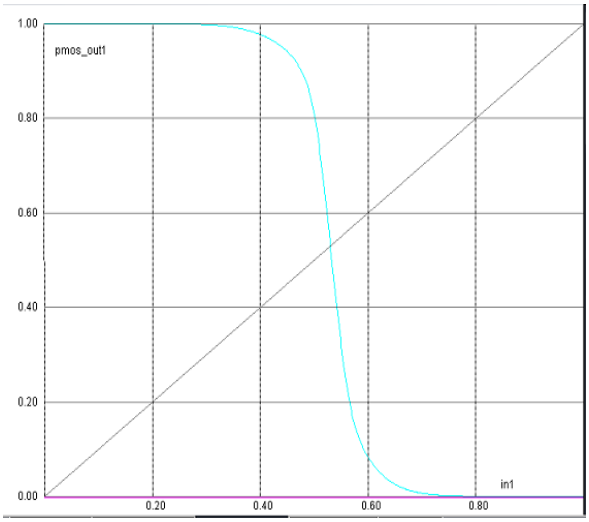


Fig 2. VTC Characteristics for CMOS inverter at V_{dd}= 1V

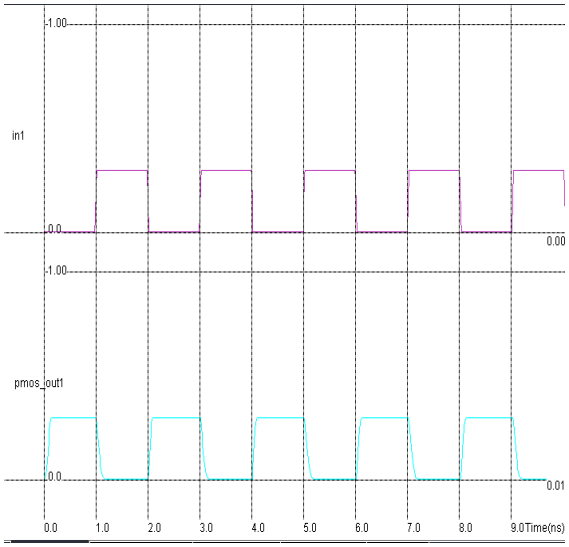


Fig 3. Voltage vs Time graph for CMOS inverter at V_{dd}= 0.3V

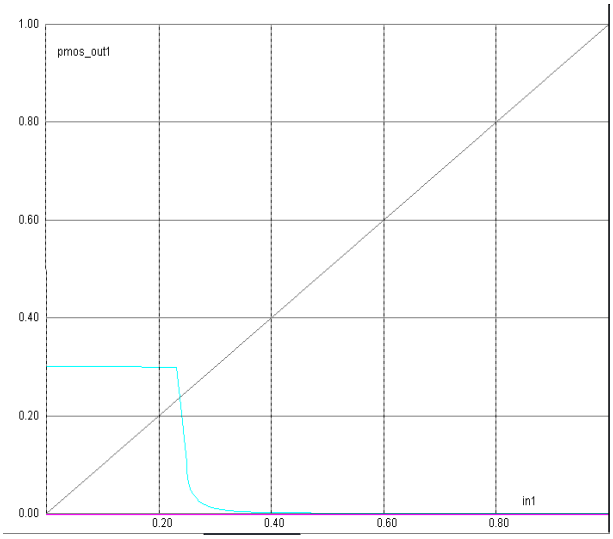


Fig 4. VTC Characteristics for CMOS inverter at V_{dd}= 0.3V

4. VOLTAGE TRANSFER CHARACTERISTICS OF PSEUDO-NMOS INVERTER

The Voltage Vs Time graph and VTC characteristics of pseudo NMOS Inverter at both strong inversion (IV) and sub-threshold region (0.3V) are shown in Fig 5, Fig 6, Fig 7 and Fig 8 respectively.

Increasing the width of PMOS load caused the VOL to rise and lower the static Noise margin in the strong inversion region. However, VTC of sub-pseudo-NMOS logic resembles that of standard CMOS having an ideal VOL which is close to zero. Here for pseudo-NMOS Inverter (W/L)p=2 and (W/L)n=8 is chosen. 5.

Comparison of Power Delay Product for CMOS and Pseudo-NMOS Logic.

Comparison of PDP for both CMOS and pseudo-NMOS inverter at both weak inversion and strong inversion is shown in Fig 9, Fig 10 and for CMOS 2 input NAND and pseudo-NMOS 2 input NAND is shown in Fig 11 and Fig. 12.

From the Figures 9 and 10 the PDP of pseudo-NMOS in weak inversion is almost comparable with PDP of CMOS in weak inversion. From the Figures 11 and 12 it is observed that power delay product of pseudo-NMOS is much worse when we go to strong inversion compared to CMOS in strong inversion. This is because of large static power dissipation, when operated at regular 1V supply voltage.

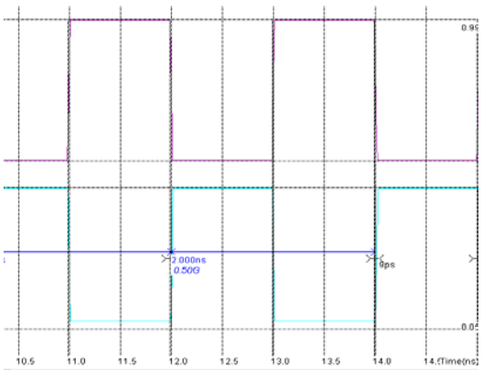


Fig 5. Voltage vs Time graph for Pseudo-NMOS inverter at V_{dd}= 1V

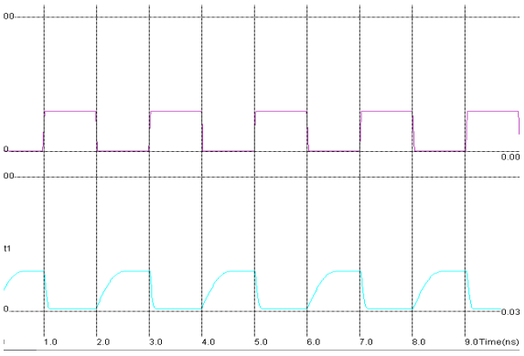


Fig 7. Voltage vs Time graph for Pseudo-NMOS inverter at V_{dd}= 0.3V

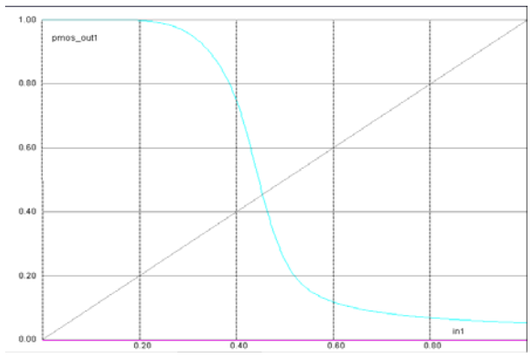


Fig 6. VTC Characteristics for Pseudo-NMOS inverter at V_{dd}= 1V

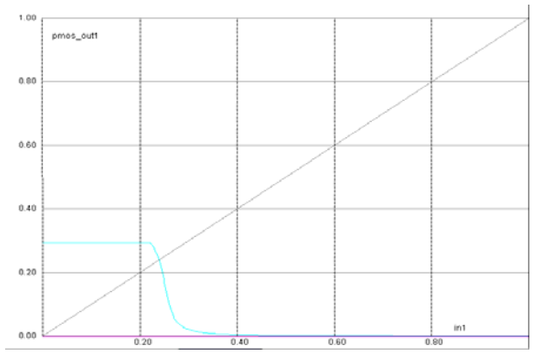
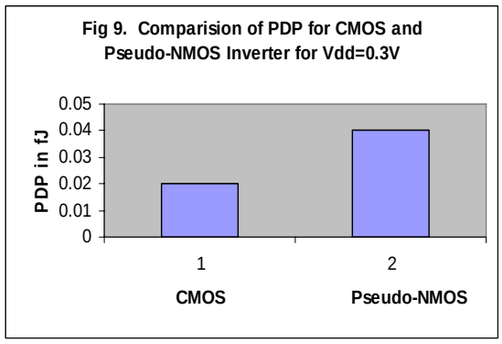
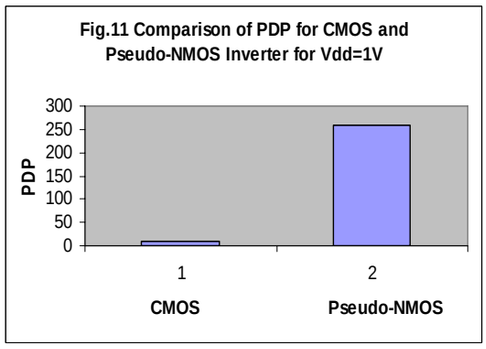
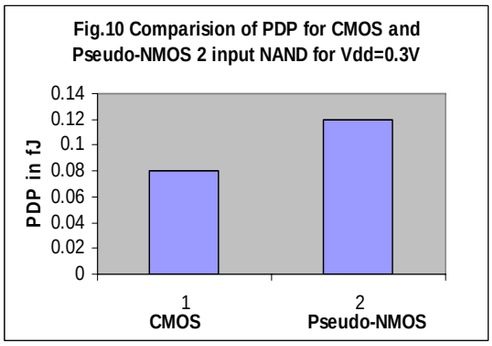
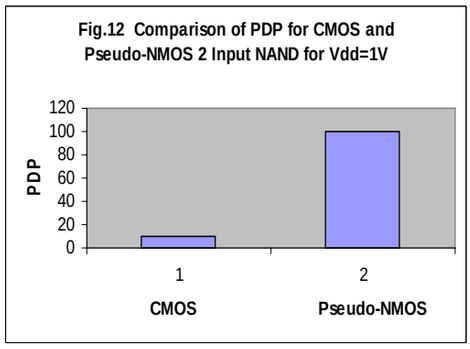


Fig 8. VTC Characteristics for Pseudo-NMOS inverter at V_{dd}= 0.3V









RESULTS AND DISCUSSION:

From Table1 and VTC characteristics of CMOS logic circuits, it is observed that in digital sub-threshold CMOS logic circuits, there is an excellent robustness, good noise-margin and low power consumption. It is also observed that performance of sub-threshold logic circuits become more sensitive to supply, process variations due to the exponential dependency of weak inversion current on Vgs and Vt.

Sub-threshold region of pseudo-NMOS logic inherits the advantages it has in the strong inversion such as good performance and smaller area, when compared to CMOS logic. From Table 2 it is observed that sub-threshold pseudo-NMOS is as efficient as sub-threshold CMOS in terms of PDP. From Table 3 it is also observed that PDP of pseudo-NMOS NOR logic in strong inversion is much worse, compared to pseudo-NMOS NAND logic.

It is observed from the Figures 9, 10, 11 and 12, weak inversion PDP of pseudo-NMOS is almost comparable with CMOS logic. But the PDP of pseudo-NMOS in strong inversion is much worse when compared to PDP of CMOS in strong inversion.

CONCLUSION:

This paper focuses on various digital circuits operating in sub threshold region for achieving ultra low power. A number of advantages in sub threshold operation includes improved gain, noise margin, and tolerant to higher stack of series transistors while being more energy efficient than standard CMOS at low frequency of operation. However, due to its slow performance, sub threshold circuit is limited to only certain applications, where ultra-low power is the main requirement, and performance is of secondary importance.

REFERENCES.

[1]. Frenkil.J "A Multilevel Approach to Low-Power IC design," in IEEE spectrum Vol.35, PP.54 -60, February 1998.

[2]. Chandrakasan, A.P, "Low-Power CMOS Digital Design" in IEEE Jl of Solid state rcuits.

[3]. Chandrakasan, A.P and Brodersen, R.W., "Low Power CMOS Digital Design," IEEE

[4]. M. Horowitz., et. A1, "Low Power Digital Design", IEEE symposium on Low Power Electronics 1994, pp. 8-11.

[5]. 5. H. Soeleman, “Ultra low power digital Sub-threshold logic design,” Ph.D. dissertation, Dept. Elect. Comput. Eng, purdue university, W.Lafayette, IN 2000

[6]. 6. M. Horowitz, et. Al, “Low Power Digital Design”, IEEE symposium on Low Power Electronics 1994, pp. 8-11.

[7]. 7. Soeleman. H and Roy.K and Bipul Paul, “Robust Sub-threshold Logic for Ultra Low-Power Operation,” in IEEE Trans on VLSI system special issue-2000

[8]. 8. L.A. Feddes, “Historical Highlights in cardiac pacing”, IEEE Engineering in Medicine and Biology magazine, pp. 12- 18, June 1990.

[9]. 9. A.P. Pentland, et. al., “Digital Doctor. An experiment in wearable telemedicine”, International Symposium on wearable computer, pp. 173-174, 1997.

[10]. 10. T. Starner, “Human powered wearable computer”, IBM systems journal, pp 618-629, v. 35, 1996.

[11]. 11. Y. Taur, and T.H. Ning, “Fundamentals of modern VLSI devices,” Cambridge university press, New York,1998.

[12]. 12. A.P. Chandrakasan et.al., “Low-power CMOS digital design,” in IEEE Jl. Of solid state circuits, vol. 27, pp. 473-484, April 1992.

[13]. 13. C.H. Kim, and K. Roy, “Dynamic V_{TH} scaling schema for active leakage power reducing,” in Proc. of Design Automation and Test in European Conference and Exhibition, pp.163 - 167,2002.

[14]. 14. H. Soeleman, K. Roy, and B.C.Paul, “Robust Sub-threshold logic for ultra low power operation,” in IEEE trans. On VLSI systems, vol .9., no.1 pp. 90-99, 2001.

[15]. 15. H. Soeleman, K. Roy, and B.C.Paul, “Robust ultra low power sub-threshold DTMOS logic,” in IEEE Intl. Symp. On low power electronics (ISLPED, pp.94- 96, 2000.