FPGA IMPLEMENTATION OF DES USING PIPELINING CONCEPT WITH SKEW CORE KEY-SCHEDULING

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ABSTRACT

This paper presents a high-performance reconfigurable hardware implementation of the Data Encryption Standard (DES) algorithm. This is achieved by combining pipelining concept with novel skew core key scheduling method and compared with previous illustrated encryption algorithms. The DES design is implemented on Xilinx Spartan-3e Field Programming Gate Arrays (FPGA) technology. Final 16-stage pipelined design is achieved with encryption rate of 7.160 Gbit/s and 2814 number of Configurable logic blocks (CLBs). This result is among the fastest hardware implementations with better area utilization.

Key Words: *Data Encryption Standard (DES) algorithm, Field Programming Gate Arrays (FPGA), pipelining, key scheduling, skew core concept.*

1. INTRODUCTION

The DES algorithm is a private-key encryption algorithm, which was developed by IBM and has been a federal standard since 1977 [1]. Presently replaced by the Advanced Encryption Standard (AES) algorithm, but still used widely in the public domain and provides a basis for comparison for new algorithms.

A 16-stage pipelined DES Algorithm hardware implementation is outlined in this paper. It allows 16 data blocks to be processed simultaneously resulting in an impressive gain in speed. It also supports the use of different keys every clock cycle, thus improving overall security since users are not restricted to using the same key during any one session of data transfer. The design is implemented on Xilinx Spartan FPGA technology. Implementing cryptographic algorithms on reconfigurable hardware provides major benefits over VLSI (very large scale integrated circuits) and software platforms since they offer high speed similar to VLSI and high flexibility similar to software. VLSI implementations are fast but must be designed all the way from behavioral description to the physical layout. They have to follow an expensive and time consuming fabrication process. Software implementations offer high flexibility but they are not fast enough for the applications where time factor is vital.

On the other hand, reconfigurable devices are attractive since the time and costs of VLSI design and fabrication can be reduced. Moreover, they offer high potential for reprogramming and experimenting on multiple architectures or several revisions of the same architecture.

The rest of this paper is organized as follows: Section 2 describes the DES algorithm. Our proposed DES architecture and its implementation on a reconfigurable hardware device are presented in Section 3 and Section 4. Section 5 gives implementation summary. Section 6 compares the achieved results with the previous DES implementations. Conclusions and references are given in Section 7 and 8 respectively.

2. DES ALGORITHM DESCRIPTION

An outline of DES is shown in Fig. 1. It is a block cipher operating on 64- bits blocks of plaintext utilizing a 64-bits key. Every eight bit of

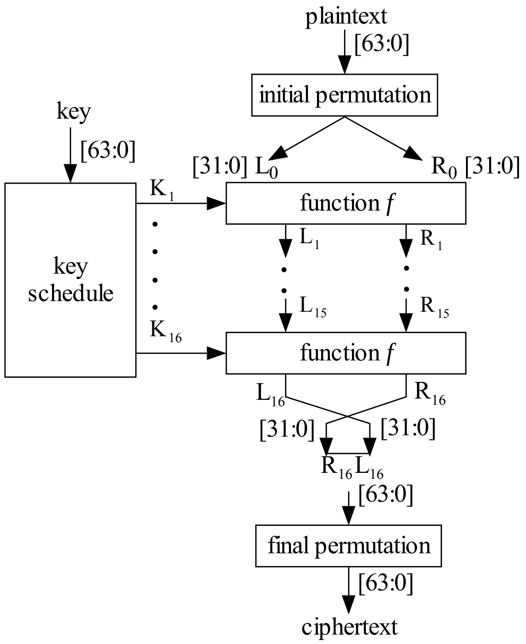


Fig. 1. DES algorithm block diagram

the 64-bits key is used for parity checking and otherwise ignored. After an initial permutation, the 64-bits input is split into a right (R_0) and left half (L_0), each 32 bits in length. DES has 16 iterations or rounds. In each round a function f is performed in which the data is combined with a 48-bits permutation of the key. After the 16th iteration, the right (R_{16}) and left (L_{16}) halves are concatenated and a final permutation, which is the inverse of the initial permutation, completes the algorithm.

2.1 *f* – Function

The function f of the DES algorithm is made up of four operations. Firstly, the 32-bits right half of the plaintext R_0 is expanded to 48-bits and then XORed with a 48-bits sub-key K1. The result is fed into eight substitution boxes (s-boxes), which transform the 48-bits input to a 32-bits output. Finally, a straight permutation (P-permutation) is performed, the output of which is XORed with the initial left half, L_0 to obtain the new right half R_1. The original right half R_0becomes the new left half L_1. This is shown in Fig. 2.

2.2 Key-Scheduling

The initial step in the in this procedure is to remove the parity check bits in the 64-bit key. Every eighth bit is used for parity checking, leaving 56-bits. A different 48-bits sub key is now generated for each of the 16 rounds of DES. The sub-keys are determined by first splitting the 56-bits into two 28-bits lengths of data. Then both halves are shifted left by either one or two bits depending on the round number.

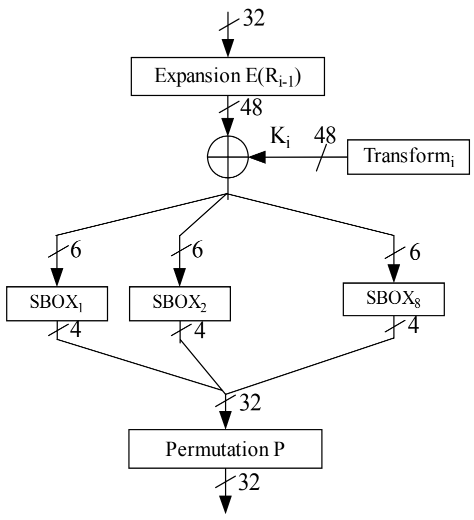


Fig. 2. f – function

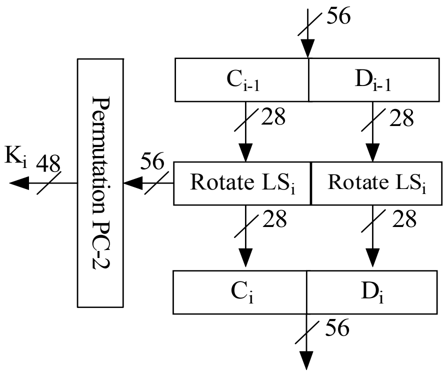


Fig. 3. One round of Keyschduling unit.

3. PIPELINING THE DES ALGORITHM

Pipelining is wildly use method in large design for speed enhancement. The iterative nature of the DES algorithm makes it ideally suited to pipelining and that can be 4, 6, 8 or 16 stages. The DES algorithm implementation presented in this paper is based on the ECB mode with 16 stages pipelining. Although the ECB mode is less secure than other modes of operation, it is commonly used and its operation can be pipelined [9].

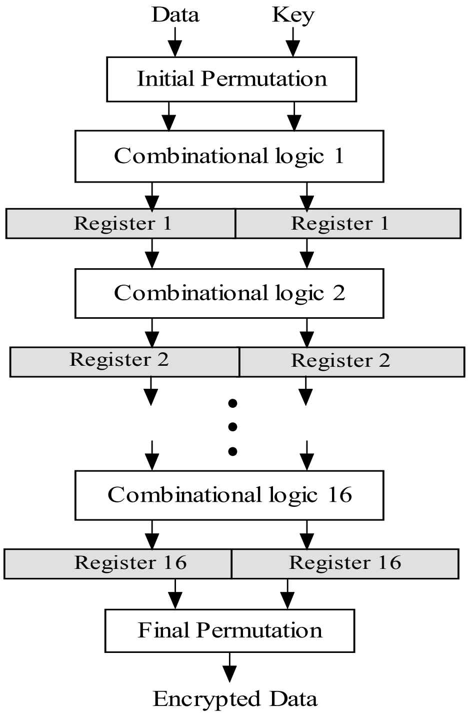


Fig. 4. DES Pipeline Architecture.

4. SKEW CORE KEY-SCHEDULING

In the implementation of the DES algorithm key schedule employed here same as above stated. the sub-keys are pre-computed that can also be done by direct mapping [6] of given key in required sub-keys but both ways using only wiring resources, So this part will be executed very fast and no optimizations would have any stage pipelined DES design and key-scheduling, it is necessary to control the time at which the sub-keys are effect. For maintaining proper synchronization in 16-available to each function *f* block. This is accomplished by the addition of a skew [6] that delays the individual sub-keys by the required amount. The skew consists of 48 bits array of register shown in Fig. 5. An outline of this key scheduling method is provided in Fig. 6, since the DES algorithm consists of 16 rounds, the skew

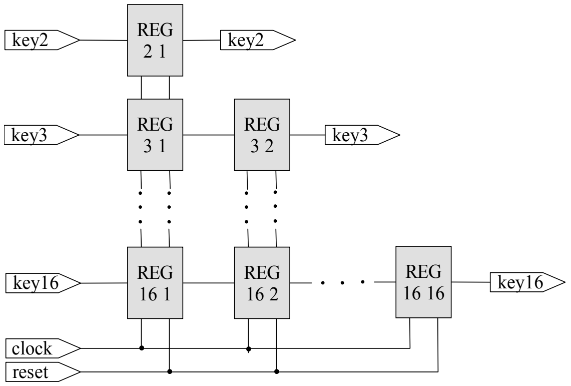


Fig. 5. Register arrays.

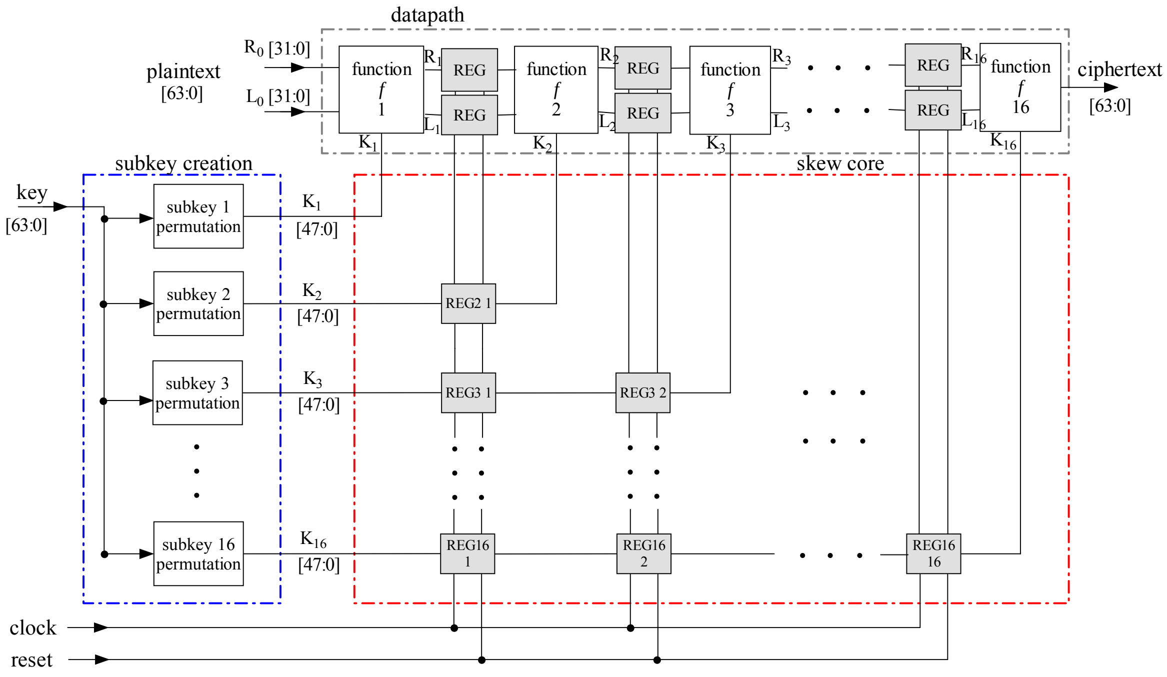
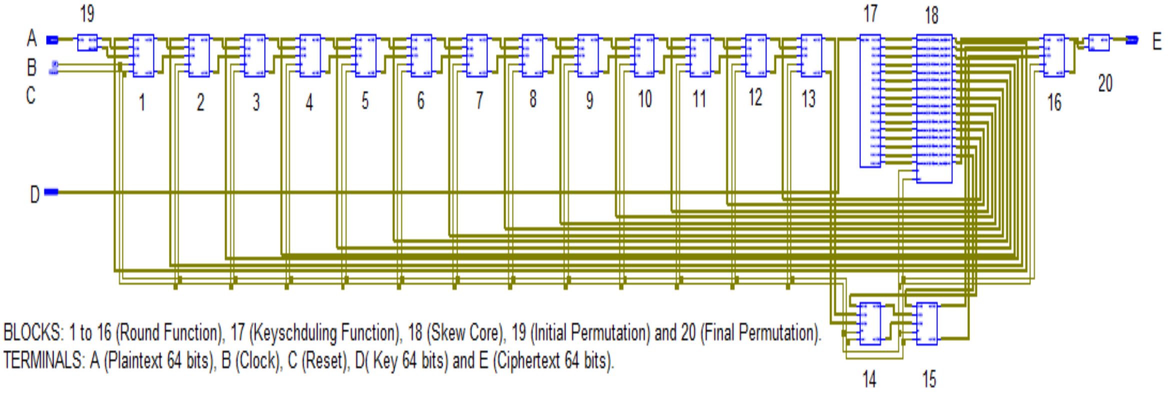


Fig. 6. Skew core Key-scheduling in DES design.

core is set to loop 15 times since a register is not required to delay the first sub-key. The number of resister in each sub-key path same as plaintext passes the no. of register before reaching respective round as shown in Fig. 6. It is noticeable that design of these registers same as used in Round blocks.

5. IMPLEMENTATION SUMMARY

FPGA implementation of DES algorithm was accomplished on a Spartan-3e device XC3s500e-4bg320 using Xilinx Foundation Series F 9.2i as synthesis and Modelsim 6.3f as simulation tool. The design was coded using VHDL language. It occupied 2814 (60%) CLB slices, 1704 (18%) slice Flip Flops and 186 (80%) I/Os. The design achieves a frequency of 111.882 MHz. It takes 16 clock cycles latency first time only then encrypts one data block (64-bits) per clock cycle. Therefore, the achieved throughput is (111.882 ×64) = 7.160 Gbits/s. full design schematic and simulation window shown in fig. (15).



BLOCKS: 1 to 16 (Round Function), 17 (Keyschduling Function), 18 (Skew Core), 19 (Initial Permutation) and 20 (Final Permutation).
TERMINALS: A (Plaintext 64 bits), B (Clock), C (Reset), D(Key 64 bits) and E (Ciphertext 64 bits).

Fig. 7. Full DES design schimatic genrated by Xilinx ISE tool.

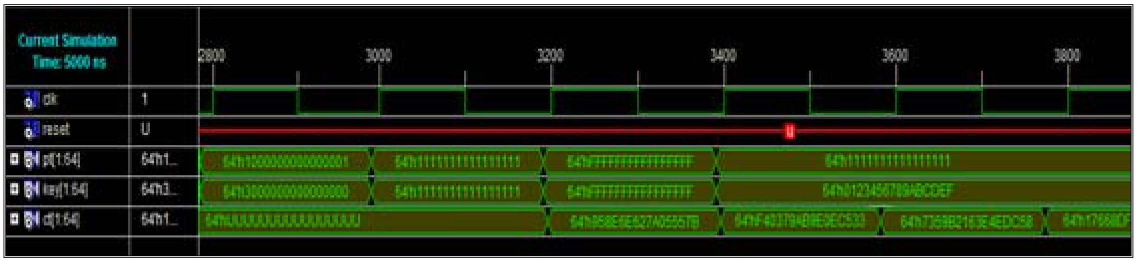


Fig. 8. Simulation Window of DES design.

6. PERFORMANCE COMPARISON

Table 1 shows the performance figures for some representative DES hardware implementations. Notice that the achieved results are competitive with the existing implementations.

A VLSI implementation of DES on static 0.6 micron CMOS technology at [7] is the fastest implementation of DES reported in the literature. Using a pipeline approach, the encryption can be performed at the rate of ≥ 6.7Gbs. Several FPGA implementations of DES have been reported in the literature achieving throughput ranges from 26 to 10752 Mbits/s using different design strategies. A DES implementation at [5] is a free DES cores which uses pipeline approach in ECB mode and achieves a data rate of 3052 Mbits/s. A java-based (Jbits) DES implementation at [8] achieves the fastest encryption rate of 10752 Mbits/s. DES implementation at [6] implements both 2-stage and 4-stage pipeline approaches obtaining throughput of 183.8 Mbits/s and 402.7 Mbits/s respectively. Almost all FPGA architectures for DES implement use partially or fully pipeline approaches.

Now compare our Design with various claims of DES implementation based on pipeline approach in

Table 1 Performance comparison.

Manufacture	Device Used	CLB slices	System clock(MHz)	Data rate(Mbit/s)	
Wong et al. (3)	XC4020E	438	10	26.7	Non-pipeline, One round Design
Bilam (9) (software)	Alpha 8400	----	300	127	16 stage Pipeline Designs
Kaps and Paar (4)	XC4028EX	741	25.18	402.7	
Free-DES(5)	XCV400	5263	47.7	3052	
McLoone, McCanny(6)	XCV1000	6446	59.5	3808	
Sandia Laboratories(7)	ASIC	----	----	9280	
Patterson(Jbits)(8)	XCV150	1584	168	10752	
Proposed Design	**XC3S500E**	**2814**	**111.882**	**7160**	

ECB mode shown in Table 1 with name of "Proposed Design", we find that only one claim, A java-based (Jbits) DES implementation [8] is above our design with encryption rate of 10752 Mbits/s, which is fastest FPGA design up to now. However, in this design the key schedule is computed in software and can only support one key per data transfer session. Therefore, performance of the presented DES design is ranked second in over all designs and one of the fastest single-chip FPGA designs.

7. CONCLUSION

This paper describes the design of a high performance silicon intellectual property core for the DES encryption algorithm. A 16-stage pipelined DES algorithm design is presented. This involved the instantiation of the function *f* block 16 times. Data blocks can be loaded every clock cycle and after an initial delay of 16 clock cycles the corresponding encrypted/decrypted data blocks will appear on consecutive clock cycles. Different keys can be loaded every clock cycle allowing the possibility of using multiple keys in any one session of data transfer. In general, hardware implementations of encryption algorithms and their associated keys are physically secure, as they cannot easily be modified by an outside attacker. At a clock frequency of 111.882 MHz, the 16-stage pipelined design can encrypt or decrypt data blocks at a rate of 7.16 Gbit/sec and should prove very useful in applications where speed is vital as with real-time communications such as satellite communications and electronic financial transactions etc.

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