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EVALUATION OF VARIOUS MULTICARRIER SPWM STRATEGIES FOR SINGLE PHASE SEVEN LEVEL CASCADED QUASI-Z-SOURCE INVERTER

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ABSTRACT

This paper focused on the performance analysis of various Multicarrier Pulse Width Modulation (MCPWM) strategies with Sinusoidal reference for single phase seven level cascaded quasi-Z-source inverter (qZSI). It is a new topology derived from the traditional Z-source inverter (ZSI), employing an impedance network which couples the source and the inverter to achieve voltage boost and inversion. The qZSI inherits all the advantages of the ZSI, which can realize buck/boost, inversion and power conditioning in a single stage with improved reliability. In addition, the proposed qZSI has the unique advantages of lower component ratings and constant dc current from the source. The cascaded quasi-Z-source based MLI strategy enhances the fundamental output voltages particularly at lower modulation index ranges with reduction in Total Harmonic Distortion (THD). Performance factors such as %THD, V_{RMS} where measured and CF, DF of output voltage are calculated for different modulation indices 0.8-1. The results are compared. The simulation results indicate that the use of quasi-Z-Source in CMLI boost 45% of the total output voltage. PODPWM strategy provides low THD and COPWM strategy is found to perform better since it provides relatively higher fundamental V_{RMS} output voltage.

Keywords: *Cascaded Multilevel Inverter (CMLI), Z-source inverter (ZSI), quasi-Z-source inverters (qZSI), Multicarrier Pulse width modulation (MCPWM), Total Harmonic Distortion (THD), Shoot-through, Buck-Boost*

1. INTRODUCTION

Quasi-Z-source inverter (qZSI) is a new promising power conversion technology perfectly suitable for interfacing of renewable energy sources. The quasi z-source inverter (qZSI) is a single stage power converter derived from the Z-source inverter topology, employing a unique impedance network. The conventional VSI and CSI suffer from the limitation that triggering two switches in the same leg or phase leads to a source short and in addition, the maximum obtainable output voltage cannot exceed the dc input, since they are buck converters and can produce a voltage lower than the dc input voltage. Both Z-source inverters and quasi-Z-source inverters overcome these drawbacks, by utilizing several shoot-through zero states. Minh-Khai Nguyen et al [1] presented the operating principles, analysis, simulation results of Embedded Switched-Inductor Z-Source Inverter and compares them to the conventional switched-inductor Z-source inverter. V.Arun et al [2] focussed on multicarrier sinusoidal pulse width modulation (MCSPWM) technique for the three phase seven level Z source cascaded inverter. Shajith et al [3] proposed a new carrier based pulse width modulation (PWM) strategy for the quasi-z-source inverter (QZSI). Mohamed Yousuf et al [4] presented a comparative THD analysis of NPC multilevel Z-Source inverter using novel PWM control strategies, which is effectively used for harmonic mitigation. Kandasamy et al [5] presented an effective utilization of non – conventional resource (wind) which is used as source of one of the H bridge in cascaded multilevel inverter. Seyezhai et al [6] presented a cascaded five level Z-Source inverter for renewable energy systems and employs Z network between the DC source and inverter circuitry to achieve boost operation. Josh et al [7] presented about the 3-level NPC inverter with Z-Source and the same inverter along with various multicarrier PWM techniques. Palanivel et al [8] presented various carrier pulse width modulation techniques, which can minimize the total harmonic distortion and enhances the output voltages from five level inverter. The comparison of pulse width modulation methods for a quasi impedance source inverter was described in [9]. Poh Chiang Loh et al [10] introduced a new family of embedded EZ-source inverters which can produce the same gain as the Z-source inverters but with smoother and smaller current/voltage maintained across the DC input source and within the impedance network. Mohd.Shafie Bakar et al [11] analysed various PWM controls on single-phase Z-source inverter(1) Yuan Li et al [12] presented a quasi-Z-source inverter (qZSI) which is a new topology derived from the traditional Z-source inverter (ZSI). The qZSI inherits all the advantages of the ZSI, which can realize buck/boost, inversion and power conditioning in a single stage with improved reliability. Joel Anderson et al [13] suggested that quasi-Z-source Inverters are similar to the Z-Source inverters but have several advantages, including in some combination, lower component ratings, reduced source stress, reduced component count and simplified control strategies. The different pulse width modulation techniques for Z-source inverter are presented in [14]. Traditional inverters are known to produce an output voltage which is lower than the DC source voltage was discussed in [15].

2. SEVEN LEVEL CASCADED QUASI-Z-SOURCE INVERTER

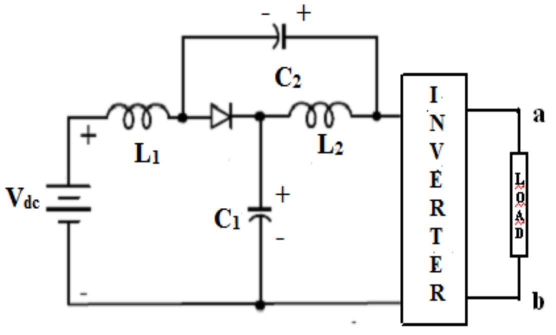

Fig.1. Voltage Fed Quasi-Z-Source Inverter

Fig.1 show the voltage fed qZSI. With the qZSI and ZSI, the unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing the shoot-through state. This network will effectively protect the circuit from damage when the shoot-through occurs and by using the shoot-though state, the (quasi-) Z-source network boosts the dc-link voltage. The major differences between the ZSI and qZSI are the qZSI draws a continuous constant dc current from the source while the ZSI draws a discontinuous current and the voltage on capacitor C_2 is greatly reduced. The dependence of control variables voltage on C_2 is much less than that on C_1 during operating and this feature leads to lower manufacture cost The continuous and constant dc current drawn from the source with this qZSI make this system especially well suited for PV power conditioning systems.

In addition, there are some unique merits of the qZSI when compared to the ZSI:

(1) The two capacitors in ZSI sustain the same high Voltage; while the voltage on capacitor C_2 in qZSI is lower, which requires lower capacitor rating;

(2)The ZSI has discontinuous input current in the boost mode; while the input current of the qZSI is continuous due to the input inductor L_1, which will significantly reduce input stress;

(3) For the qZSI, there is a common dc rail between the source and inverter, which is easier to assemble and causes less EMI problems.

Fig.2 shows the topology of the proposed single phase Quasi-Z-source seven level cascaded Inverter, consisting of a split inductors (L_1 and L_2) and two capacitors (C_1 and C_2) are connected with the input DC sources and switches. The diode D will effectively protect the circuit from damage when the shoot-through occurs and by using the shoot-though state, the (quasi-) Z-source network boosts the dc-link voltage. Comparing with the normal Z-source inverter, the impedance are arranged so as to form the represented structure of qZSI. The proposed Quasi- Z-source based seven-level cascaded inverter is controlled with their AC outputs transiting between the seven distinct voltages. They are: $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$. To obtain the seven levels, the required switching scheme is given in Table.1.

The presented qZSI is expected to perform better, since performance limitations commonly associated with dead-time delay which was avoided. The qZSI network is responsible for the voltage boost up. The inversion is performed by supplying PWM signals to the switches of the circuit in a certain fashion so as to produce seven levels at the output. Inductors L_1 and L_2 have the same values and Capacitors C_1 and C_2 have the same values. QZSI network is a symmetrical network. The operating states of the qZSI are shoot through zero state and non shoot through zero state. In this proposed inverter the number of bridges required is 3 hence it consists of 12 switches.

$$N = \frac{(m-1)}{2} = 3.$$

where; m= Number of levels

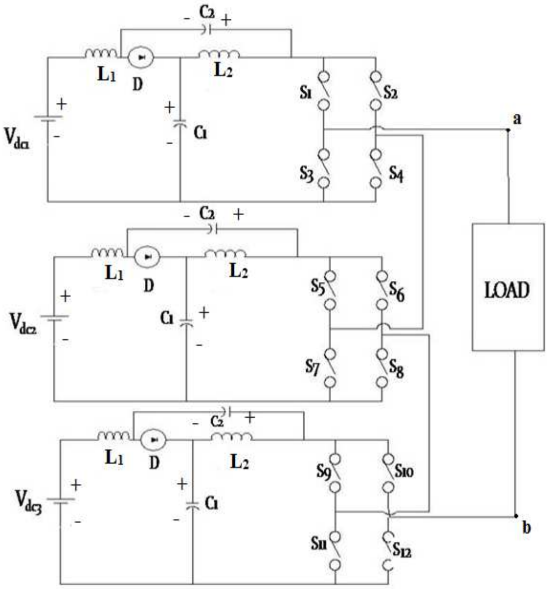

Fig.2. Seven Level Cascaded Quasi-Z-Source Inverter

TABLE I
SWITCHING SCHEME FOR SEVEN LEVEL CMLI

S_1	S_2	S_3	S_4	S_5	S_6	S_1’	S_2’	S_3’	S_4’	S_5’	S_6’	V_{ab}
1	0	0	1	1	0	0	1	1	0	0	1	+3 V_{dc}
1	0	0	1	1	0	0	1	1	0	1	0	+2 V_{dc}
1	0	0	1	0	1	0	1	1	0	1	0	+1 V_{dc}
1	0	1	0	0	1	0	1	1	0	1	0	0
0	1	1	0	0	1	1	0	1	0	0	1	-1V_{dc}
0	1	1	0	0	1	1	0	0	1	0	1	-2V_{dc}
0	1	1	0	0	1	1	0	0	1	1	0	-3V_{dc}

3. MULTIICARRIER SINE PULSE WIDTH MODULATION STRATEGIES

To synthesize multilevel output AC voltage using different levels of DC inputs, semiconductor devices must be switched ON and OFF in such a way that desired fundamental is obtained with minimum harmonic distortion. There are different types of approaches for the selection of switching techniques for the multilevel inverters. Among all the PWM methods for cascaded qZSI, carrier based PWM methods and space vector methods are often used but when the number of output levels is more than five, the space vector method will be very complicated with the increase of switching states. So the carrier based PWM method is preferred under this condition in qZSIs. This paper focuses on carrier based PWM strategies which have been extended for use in qZSI by using multiple carriers. Multicarrier PWM strategies have more than one carrier that can be triangular waves or sawtooth waves and so on. The carrier waves can be either bipolar or unipolar. In this paper, the bipolar multi-carrier PWM technique is considered. The modulating/reference wave of multicarrier PWM technique is sinusoidal in this paper but it can be trapezoidal also. In this paper, various multicarrier PWM strategies like Phase disposition (PD), Phase opposition disposition (POD), Alternative phase opposition disposition (APOD), Variable Frequency (VF) and Carrier Overlapping (COPWM) are proposed for single phase seven levels cascaded qZSI.

For an *m*-level inverter using bipolar multicarrier technique, (*m*-1) carriers with same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and placed at zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched ON. Otherwise, the device switched OFF. In this paper, the frequency ratio $m_f = 21$ and modulation index m_a is varied from 0.8 to 1.

$m_f = f_c / f_m$ except for VFPWM
$m_a = 2A_m / (m-1) Ac$ except for COPWM

3.1 Phase Disposition (Pd) Pwm Strategy

The Principle of PDPWM technique is to use the several carriers with single modulating waveform. In phase disposition all the carriers are in phase and the carriers are disposed so that the bands they occupy are contiguous. The modulation wave is centered in the middle of the carrier set. Fig.3 shows the multicarrier arrangement for PDPWM technique for m_a= 0.8 and m_f = 21.

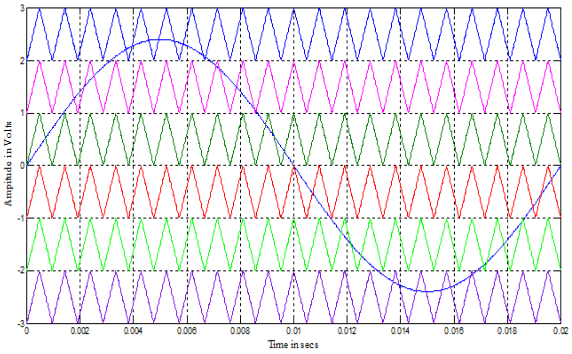

Fig.3 Carrier Arrangement For PDPWM Strategy

3.2 Phase Opposition Disposition (Pod) Pwm Strategy

With the PODPWM method the carrier waveforms above the zero reference value are in phase.

The carrier waveforms below zero are also in phase but are 180 degrees phase shifted from those above zero. Fig.4 shows the multicarrier arrangement for PODPWM method for m_a= 0.8 and m_f =21.

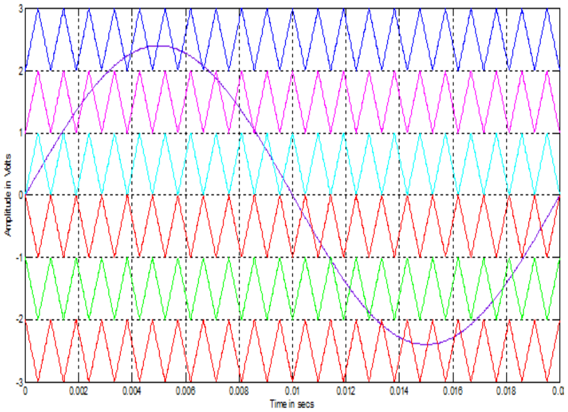

Fig.4 Carrier Arrangement Of PODPWM Strategy

3.3 Alternative Phase Opposition Disposition (Apod) Pwm Strategy

This method requires each of the six carrier waves for a seven level inverter to be phase displaced from each other by 180° alternately. Fig.5 shows the multicarrier arrangement for APODPWM method for m_a= 0.8 and m_f =21.

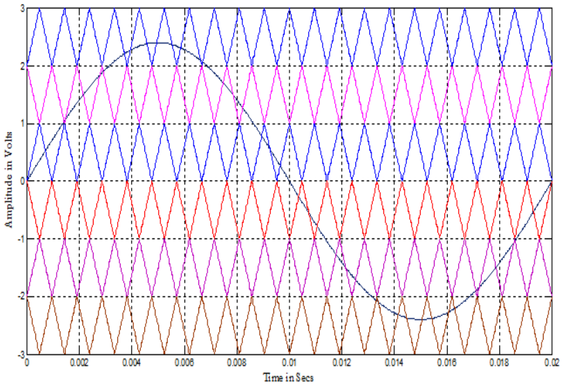

Fig.5 Carrier Arrangement For APODPWM Strategy

3.4 Variable Frequency (Vf) Pwm Strategy

The number of switchings for upper and lower devices of chosen Embedded Z-source inverter is much more than that of intermediate switches in constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM technique is used as illustrated in Fig.6, in which the carrier frequency of the intermediate switches is properly increased to balance the number of switchings for all the switches.

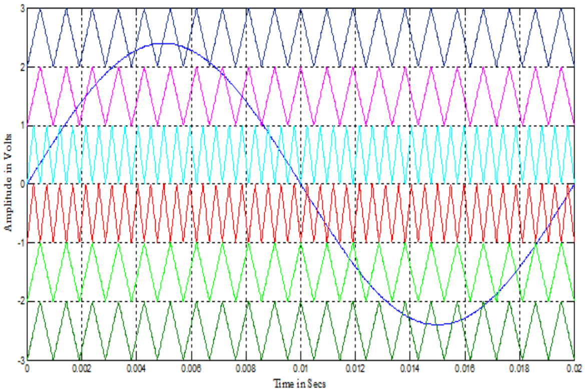

Fig.6 Carrier Arrangement For VFPWM Strategy

3.5 Carrier Overlapping (Co) Pwm Strategy

In the carrier overlapping strategy, *m-1* carriers are disposed such that the bands they occupy overlap each other, the overlapping vertical distance between each carrier is $A_c/2$ (A_c=1.6).The reference waveform is centred in the middle of the carrier signals. The amplitude modulation index ma is defined as follows:

$$m_a = A_m/2A_c$$

The vertical offset of carriers for seven-level inverter with COPWM technique is shown in Fig.7.

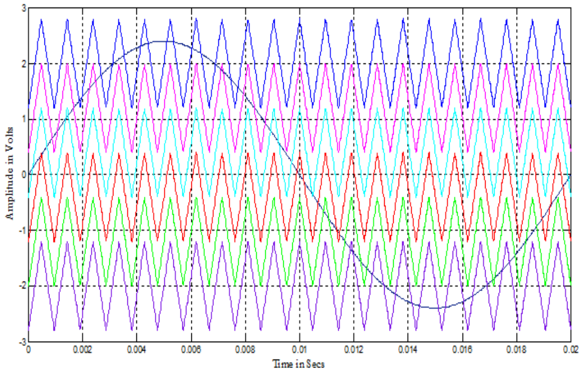

Fig.7 Carrier Arrangement For COPWM Strategy

4 SIMULATION RESULTS

The seven level cascaded qZSI is modeled in SIMULINK using Power System block set. Switching signals for quasi Z-source multilevel inverter are developed using multicarrier sinusoidal PWM techniques. Simulations are performed for different values of m_a ranging from 0.8–1.

Figs.8–17 show the simulated output voltage of quasi Z-source multilevel inverter with their corresponding FFT plots shown for only one sample value of m_a = 0.8. Fig.19 shows a graphical comparison of % THD for various techniques for different modulation indices.

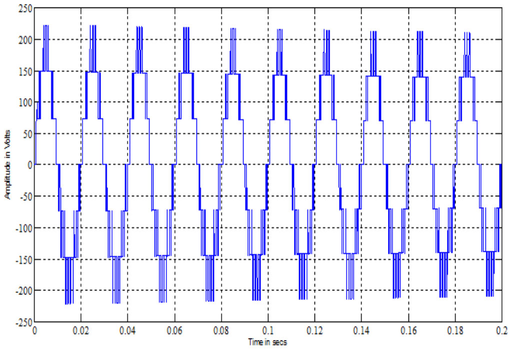

Fig.8 Output Voltage Generated By PDPWM Strategy

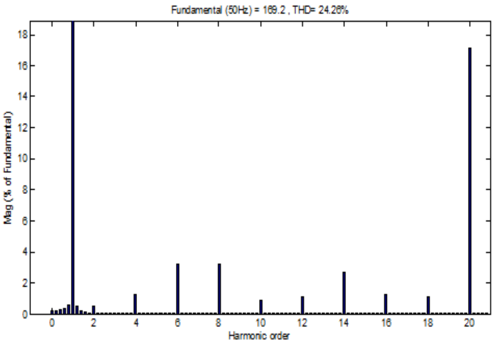

Fig.9 FFT Plot For Output Voltage Of PDPWM Strategy

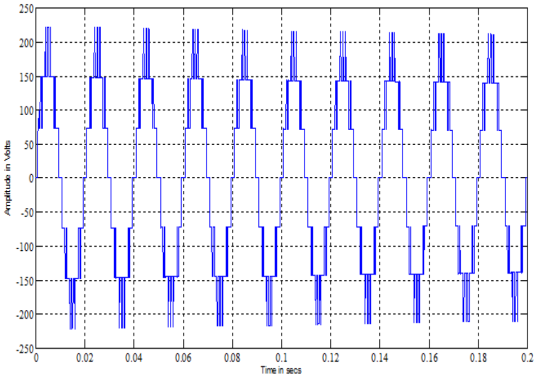

Fig.10 Output Voltage Generated By PODPWM Strategy

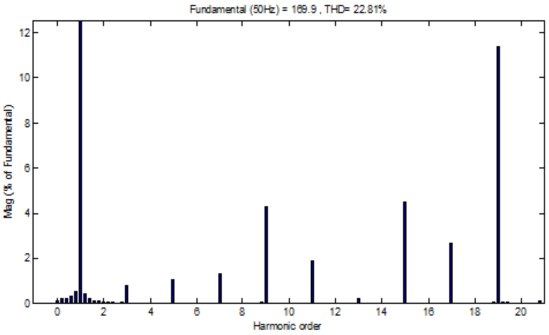

Fig.11 FFT Plot For Output Voltage Of PODPWM Strategy

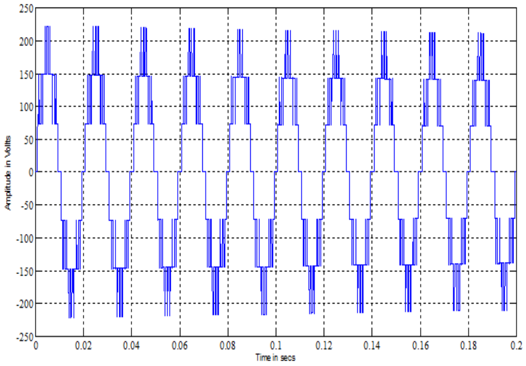

Fig.12 Output Voltage Generated By APODPWM Strategy

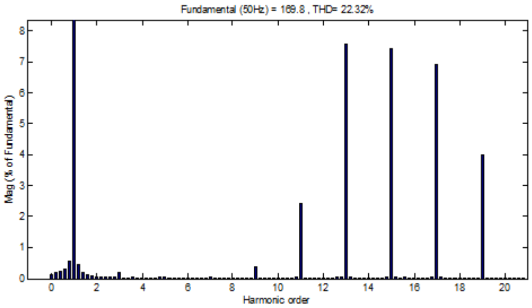

Fig.13 FFT Plot For Output Voltage Of APODPWM Strategy

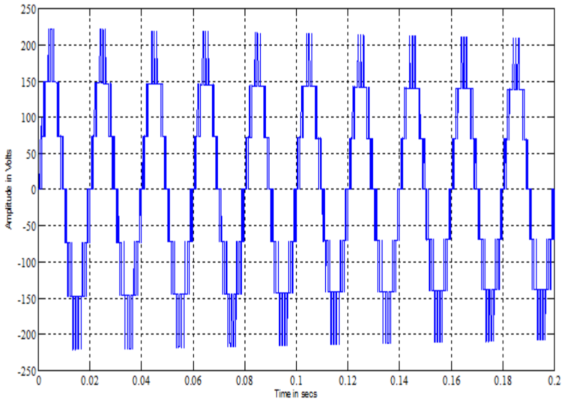

Fig.14 Output Voltage Generated By VFPWM Strategy

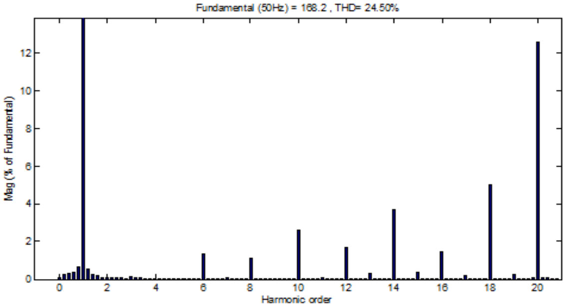

Fig.15 FFT Plot For Output Voltage Of VFPWM Strategy

m_a	PD	POD	APOD	VF	CO
1	1.413	1.414	1.414	1.413	1.413
0.95	1.414	1.414	1.413	1.414	1.414
0.9	1.414	1.413	1.414	1.414	1.414
0.85	1.414	1.413	1.414	1.414	1.414
0.8	1.414	1.414	1.413	1.414	1.414

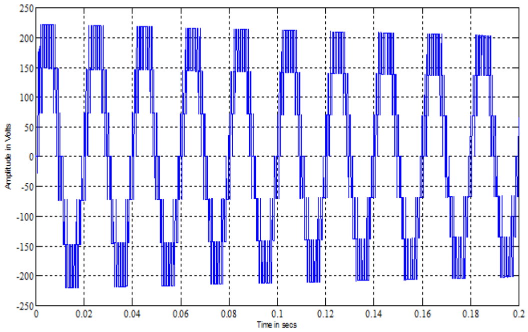

Fig.16 Output Voltage Generated By COPWM Strategy

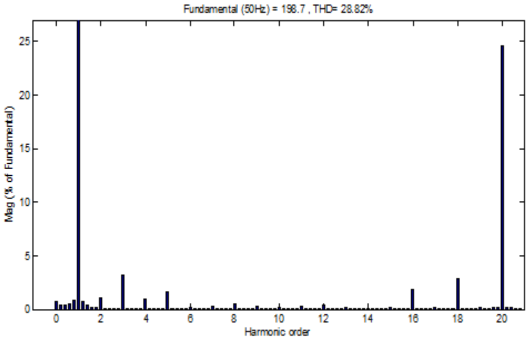

Fig.17 FFT plot for Output Voltage of COPWM strategy

Table Ii

%Thd For Different Modulation Indices

Table Iii: % Distortion Factor For Different Modulation Indices

m_a	PD	POD	APOD	VF	CO
1	17.85	15.94	18.42	17.85	22.37
0.95	20.20	18.32	20.92	20.20	22.98
0.9	22.48	21.09	22.35	22.48	24.53
0.85	23.64	22.42	22.31	22.64	26.45
0.8	24.26	22.81	22.33	24.26	28.82

Table Iv: V_{rms} (Fundamental) For Different Modulation Indices

m_a	PD	POD	APOD	VF	CO
1	149.1	149.7	140.9	149.1	161.5
0.95	141.7	143.3	141.6	141.7	157.9
0.9	134.1	135.5	133.4	134.1	152.2
0.85	127	127.2	127.5	127	146.5
0.8	119.6	120.2	120.1	119.6	140.5

The corresponding %THD is measured using the FFT block and their values are listed in Table 2. Table 3 shows the Distortion Factor (DF) of the output voltage of chosen MLI. Table 4 displays the V_{RMS} of fundamental inverter output (a measure of DC bus utilisation). Table 5 display the corresponding Crest Factor (CF). The following parameter values are used for simulation: $V_{dc1}=V_{dc2}=V_{dc3}=50V$, $C_1=C_2=400\mu F$, $L_1=L_2=500\mu H$, *RL* load(R=10KΩ & L=1mH) $f_c=1050Hz$ and $f_m=50Hz$.

Table V: Crest Factor For Different Modulation Indices

For $m_a=0.8$, it is observed from Figs. (9, 11, 13, 15 and 17), the harmonic energy above 3% is present in (i) 6th, 8th and 20th orders in PDPWM technique. (ii) 1st, 9th, 15th, 17th and 19th orders in PODPWM technique. (iii) 1st, 13th, 15th, 17th and 19th orders in APODPWM technique. (iv) 1st, 10th, 14th, 18th and 20th order in VFPWM technique. (v) 1st and 20th orders in COPWM technique. (vi) Dominant lower side band harmonic (20th order) is present in PDPWM, VFPWM and COPWM techniques.

m_a	PD	POD	APOD	VF	CO
1	0.6088	0.2028	0.0684	0.2793	0.8830
0.95	0.5158	0.1291	0.1291	0.2055	0.7292
0.9	0.3970	0.0947	0.0672	0.1315	0.6671
0.85	0.2558	0.0813	0.0664	0.0710	0.5789
0.8	0.1897	0.0994	0.0693	0.0699	0.4419

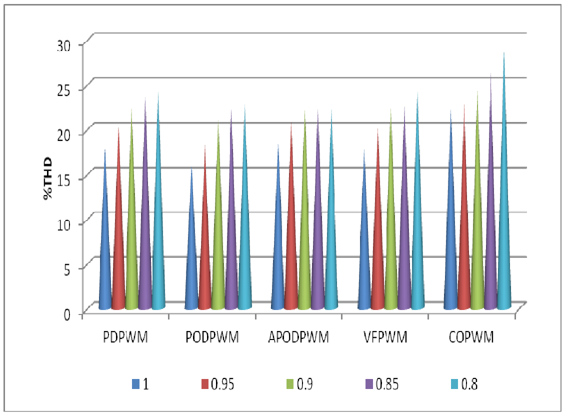

Fig.18 %THD Vs M_a

Of the five strategies developed, PODPWM technique provides output with relatively minimum distortion (Table 2), APODPWM technique has low %DF (Table 3), COPWM technique provides relatively higher RMS output voltage (Table 4) and CF is almost same for all the techniques (Table 5).

5. CONCLUSION

In this paper, various multicarrier PWM techniques for chosen Quasi-Z-source cascaded seven level inverter have been developed and simulation results are presented for different modulation indices ranging from 0.8-1. Various performance factors like %THD (a measure of closeness in shape between a waveform and its fundamental component), DF, V_{RMS} of fundamental and CF (used to specify peak current rating of the devices) have been evaluated, presented and analysed. It is observed that the PODPWM technique provides lower THD (Table 2). The maximum DC bus utilization is achieved in COPWM strategy (Table 4). Appropriate PWM techniques may be employed depending on the performance measure required in a particular application.

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