



NOVEL HARMONIC ELIMINATION TECHNIQUE FOR CASCADED H-BRIDGE INVERTER USING SAMPLED REFERENCE FRAME

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ABSTRACT

This paper proposes SWARM Intelligence based algorithm for selective harmonic elimination using SSVPWM in modified H-bridge multilevel inverter. This algorithm uses sampled reference frame to generate reference sine signal. The computation time is less as compared to that of sector identification algorithms. Also, SWARM intelligence based algorithm doesn't require any look-up table potentiometer connected to ADC channel of this dsPIC which decides the V/F ratio and the keypad connected to PORT C which decides the harmonic order that has to be eliminated. The hardware setup for the proposed method for 5-level inverter has been developed successfully for 2.2Kw Induction motor. The experimental result shows that this method can effectively reduce the selective harmonic in modified cascaded H-Bridge Multilevel inverter.

Keywords: *Swarm Space Vector Pulse Width Modulation (SSVPWM), Artificial Neuro Fuzzy Inference System (ANFIS), Selective Harmonic Mitigation Pulse Width Modulation (SMHPWM), Selective Harmonic Pulse Width Modulation (SHPWM), Total Harmonic Distortion (THD), Fast Fourier Transform (FFT), Interrupt Service Subroutine (ISR).*

1. INTRODUCTION

Artificial intelligence has become an optimization tool for solving problems having no known solution [1]. This algorithm is used for eliminating harmonics in multilevel inverter [2, 3, 4]. This inverter uses single battery source [5, 6] to obtain n-level output to drive the electric vehicle. Selective harmonic elimination is preferred to eliminate the lower order harmonics in high power drives with low cost DSP based SVPWM generation for H-bridge inverter using sampled frame [7,8]. Many genetic algorithms are proposed to solve the complex problems with unknown result [9, 10, 11] and it also increases computation time to solve more iteration even high end DSP controller [12] requires more time to solve.

The proposed sampled reference frame algorithm will reduce the computation time of the processor considerably. A SVPWM scheme based on the above principle has been used where the switching time for the inverter legs is directly determined by sampled voltages. The harmonic waveform notch insertion is determined by Fourier series expansion. The sampled voltage T_s is obtained by maximum and minimum values of phase voltage [13].

The implementation of this algorithm not only reduces the online computation time but also reduces the harmonics to satisfy the grid codes EN50160 and CIGREWG 36-05 without any additional filters. The algorithm proposed [14] is not suitable for electric vehicle applications where battery voltage (DC link voltage) is not uniform [15, 16]. This proposed system uses the neuro fuzzy optimization to reduce harmonic destruction by

selecting optimum firing angle. Also this system operates at very high frequency, so side band frequencies are shifted to higher band.

In this paper the above related issues were addressed using dsPIC platform running at 20MHz. The whole program is driven by ISR. The motor control PWM module in the dsPIC is used to generate SVPWM for the proposed 5-Level inverter for the 2.2KW Induction motor and has been tested successfully.

2. PROPOSED SYSTEM

H-bridge inverter using single source H-Bridge Multilevel inverter is shown in Figure 1 with the single DC source is proposed to test this algorithm.

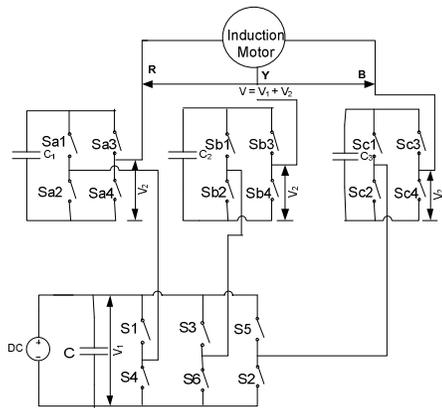


Figure 1: Circuit Diagram Of Proposed System

The overall block diagram of the proposed system is shown in Figure 2.

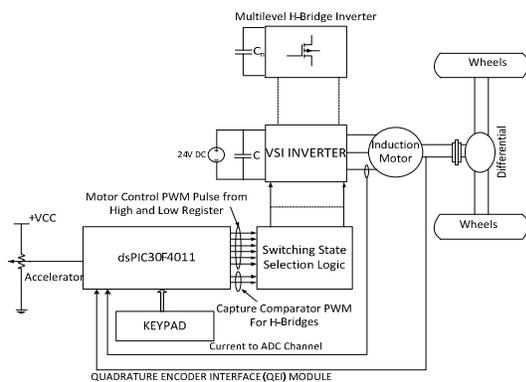


Figure 2: Block diagram of proposed system

The proposed algorithm uses only sampled amplitude of the reference phase voltages to produce reference sine signal. On the other hand the conventional algorithm requires sector identification and trigonometric functions which

require more machine cycle for computation. To improve the performance and reduce the machine cycle the purpose algorithm has been introduced. The generated third harmonic sine wave then add to carrier wave with different offset as shown in Figure 3 which decides the harmonic order to be eliminated.

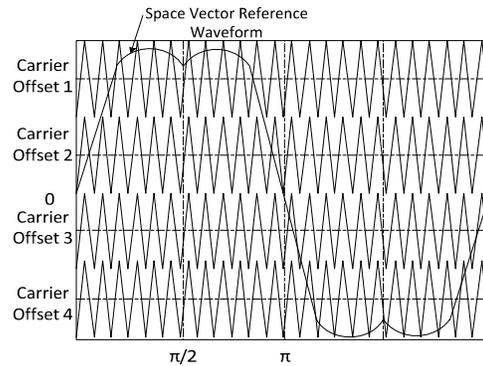


Figure 3: Offset Has Added To Triangle Carrier With Modified Sine Wave

3. GENERATING REFERENCE SIGNAL FOR SVPWM USING SAMPLED PHASE VOLTAGE

The sampled frame algorithm requires only amplitude of phase voltages. By calculating maximum, minimum and middle vales from phase voltages the effective time period is calculated illustrated in Figure 4.

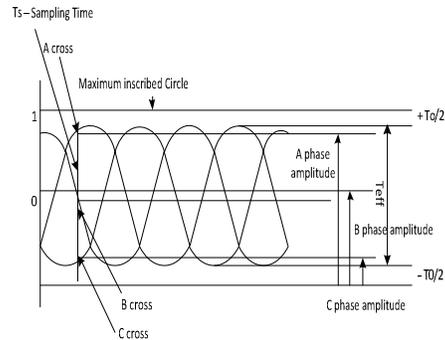


Figure 4: Effective time calculation for given sampling time

This does not require any sector information or sector time calculation.

$$V_a \left(\frac{T_s}{V_{dc}} \right) V_b \left(\frac{T_s}{V_{dc}} \right) V_c \left(\frac{T_s}{V_{dc}} \right) \quad (1)$$

Where V_a, V_b and V_c are the phase voltages, T_s Sampling time, V_{dc} DC link voltage.

By the above expression find out T_{max} and T_{min}

$$T_{max} = \max(T_{as}, T_{bs}, T_{cs}) \quad (2)$$

$$T_{min} = \min(T_{as}, T_{bs}, T_{cs}) \quad (3)$$

T_{max}, T_{min} -Maximum and minimum amplitude of phase voltage for the sample time of T_s

$$T_{eff} = T_{max} - T_{min} \quad (4)$$

T_{eff} Effective time

$$T_0 = T_s - T_{eff} \quad (5)$$

T_0 zero vector component for the samples time of

T_s Offset is required to shift T_0 to positive

$$T_0 = T_s - T_{eff} - T_{min} \quad (6)$$

$$T_{off} = \left[\frac{T_0}{2} - T_{min} \right] \quad (7)$$

Gating pulse for phases a, b and c is

$$T_{ga} = T_{as} + T_{off} \quad (8)$$

$$T_{gb} = T_{bs} + T_{off} \quad (9)$$

$$T_{gc} = T_{cs} + T_{off} \quad (10)$$

T_{off} Decides the carrier offset voltage amplitude, the effective pacing of T_{off} is done by SWARM intelligence algorithm has depicted in Figure 5.

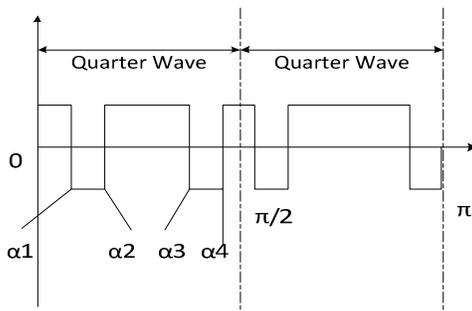


Figure 5: A_1, A_2, A_3, A_4 Firing Angle Of Notches Introduced In Quarter Wave

Placing of optimum firing angle is done by solving and Fourier series expression:

$$V_n = \frac{2V_d}{n\pi\sqrt{2}} \left[2(\cos n\alpha_1 - \cos n\alpha_2 + \cos n\alpha_3 - \dots) - 1 \right] \quad (11)$$

The above equation (9) can be solved and can be rewritten as

$$V_n(\text{rms}) = \frac{1}{\sqrt{2}} \frac{4V_{dc}}{\pi} \frac{1}{2} \left[\int_0^{\alpha_1} \sin(n\theta) d\theta - \int_{\alpha_1}^{\alpha_2} \sin(n\theta) d\theta + \int_{\alpha_2}^{\alpha_3} \sin(n\theta) d\theta - \int_{\alpha_3}^{\pi/2} \sin(n\theta) d\theta \right] \quad (12)$$

The generalized expression for selective harmonic equation can be modified for the required notches i.e. $\alpha_1, \alpha_2, \alpha_3$ and α_4 . From 0 to α_1 the notch lies in positive side from α_1 to α_2 the notch lies in negative side.

From α_2 to α_3 the notch lies in positive side. This extends up-to Quarter wave symmetry.

From $\frac{\pi}{2}$ to π the notches will be symmetrical.

Finally equation (10) can be written as

$$V_n(\text{rms}) = \frac{1}{\sqrt{2}} \frac{4V_{dc}}{\pi} \frac{1}{2} \left[\int_0^{\alpha_1} \sin(n\theta) d\theta - \int_{\alpha_1}^{\alpha_2} \sin(n\theta) d\theta + \int_{\alpha_2}^{\alpha_3} \sin(n\theta) d\theta + \int_{\alpha_3}^{\alpha_4} \sin(n\theta) d\theta \right] \quad (13)$$

Above equation is for only half wave symmetry that is from 0 to $\frac{\pi}{2}$. By writing equation 11 two

times full wave symmetry 0 to π can be obtained.

In this proposed work harmonic amplitude of 5th order, 7th order, 11th order and 13th order have been eliminated. To find the optimum firing angle for $\alpha_1, \alpha_2, \alpha_3$ and α_4 equation 11 is further reduced. Amplitude of the fundamental voltage in rms:

$$V_{rms} = 0.45 V_{dc} \left[2 \left(\begin{matrix} \cos \alpha_1 & -\cos \alpha_2 \\ +\cos \alpha_3 & -\cos \alpha_4 \end{matrix} \right) - 1 \right] \quad (14)$$

To reduce 5th, 7th, 11th and 13th order harmonics the above equation can be written as:

$$5^{\text{th}} \text{ order amplitude} \rightarrow 0 = \left[\begin{matrix} \cos 5\alpha_1 & -\cos 5\alpha_2 \\ +\cos 5\alpha_3 & -\cos 5\alpha_4 \end{matrix} \right] - 0.5 \quad (15)$$

$$7^{\text{th}} \text{ order amplitude} \rightarrow 0 = \left[\begin{matrix} \cos 7\alpha_1 & -\cos 7\alpha_2 \\ +\cos 7\alpha_3 & -\cos 7\alpha_4 \end{matrix} \right] - 0.5 \quad (16)$$

$$11^{\text{th}} \text{ order amplitude} \rightarrow 0 = \left[\begin{matrix} \cos 11\alpha_1 & -\cos 11\alpha_2 \\ +\cos 11\alpha_3 & -\cos 11\alpha_4 \end{matrix} \right] - 0.5 \quad (17)$$



$$13^{th} \text{ order amplitude} \rightarrow 0 \left[\begin{pmatrix} \cos 13\alpha_1 & -\cos 13\alpha_2 \\ +\cos 13\alpha_3 & -\cos 13\alpha_4 \end{pmatrix} - 0.5 \right] \quad (18)$$

4. SWARM OPTIMIZATION ALGORITHM

Many algorithms have been proposed to solve the above equations to reduce the harmonics to standard grid code which is tabulated in Table 1. The proposed SWARM optimization algorithm has been proposed to solve the equation along with the sampled reference frame SVPWM. This facilitates the reduction of harmonics within the grid code. Finally there are five equations and four unknowns. By solving the equation $\alpha_1, \alpha_2, \alpha_3$ and α_4 will be obtained. This is done by SWARM optimization which involves three steps.

- 4.1 Knowledge Base Generation
- 4.2 SWARM Training
- 4.3 Fine Tuning

4.1 KNOWLEDGE BASE GENERATION

The switching angles are maintained at $\theta_0 < \theta_1 < \theta_2 < \theta_3 < \theta_4, \dots, \theta_{n-1} < \frac{\pi}{2}$, upto Quarter wave

4.2 SWARM Training

The system consists of an adaptive network and ANFIS that aid in the elimination of harmonics that are generated by the electric vehicle and hybrid electric vehicle. The neural network to be utilized for the system is in Figure. 6 ANFIS consists of five fuzzy layers namely product layer, normalized layer, defuzzy layer, and total output layer. The dataset will be needed to train the network. This can be made capable by taking R_a as the reference dataset and extracting the patterns from R. The R dataset K^{th} class satisfies the R_a dataset in same class. This form is one of the training elements in training dataset R^{train} . In the same way, this process is performed for all the patterns present in R and therefore the total training dataset is formed and shown in Table 2.

4.3 Fine Tuning

Generally the ANFIS output is not accurate i.e., the switching angle generation and the corresponding voltage and THD are not equal. So it is required to increase the performance and

accuracy of the system by using tuning process. In this tuning process the constant elements like THD^T and they V^T are taken into account. The tuning process is described below.

Step 1 : Finding the Error harmonic (E_1)

$$E_1 = 0.5(THD^T - THD)^2$$

Where, THD^T is feedback Distortion value, THD is reference Distortion value.

Step 2 : Finding the error voltage E_2

$$E_2 = 0.5(V^T - V_{ph})^2$$

Where, V^T is target voltage, V_{ph} is phase voltage.

Step 3: Calculate the average error voltage E_{avg}

$$E_{avg} = 0.5(E_1 + E_2)$$

Step 4: Determine the new switching angle from the error voltage E_{avg}

$$\theta^{new} = [E_{avg} * \gamma * \theta^{old} * r] + \theta^{old}$$

θ^{new} is new switching angle, the tuning constant ($\gamma = 0.2$), r is random numbers selected within the range

θ^{old} is the value of switching angle calculated.

Step 5: Check the firing angle that lies within the limit

$$\theta_i < \theta_{i+1} < \theta_{i+2} < \dots < \theta_{i+n}; i > 0$$

If not within the limit do the following, $\theta_i^{new} > \theta_{i+1}^{new}$ is the error value, $i > 0$

Recover the firing angle θ_{i+1}^{new} with following relation,

If $\theta_i^{new} < \theta_{i+1}^{old}$ true θ_{i+1}^{old} process to next steps.

If false, $\theta_{i+1}^{new} = \theta_i^{new} + r$,

Where, $r = 0, 1$ (Random numbers).

Repeat the loop 4 and 5 until optimum result obtained. The total system has been controlled by dsPIC30F4011. The potentiometer connected in PORTA decides the V/F profile of drive. Once the speed profile has been processed then controller waits for harmonic selection command by pressing appropriate key in keyboard connected to PORTC. Speed command has been given to quadrature encoder interface which is embedded in the controller for speed. Current sensor ACS714 senses the drive current. This system had employed by inner current limit and outer speed limit control which improves the dynamic response.

5. CONTROL ALGORITHM

The control flowchart of the proposed algorithm is shown in Figure 7. This algorithm involves only normal arithmetic operation. Because of this, the execution time of the proposed method is very less.

This proposed system has been tested in MATLAB environment and the optimization is applied by training and generating through trained fuzzy set for 3rd and 5th order harmonic.

The simulation results depicted in figure 8 shows the 3rd order harmonics waveform injection which has 100% THD and the 3rd and 5th order harmonic waveform superimposed in the fundamental waveform.

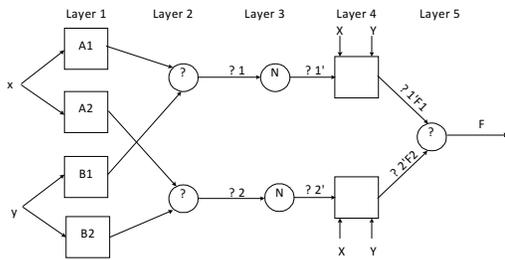


Figure 6: The Structure Of Proposed SWARM Algorithm Technique

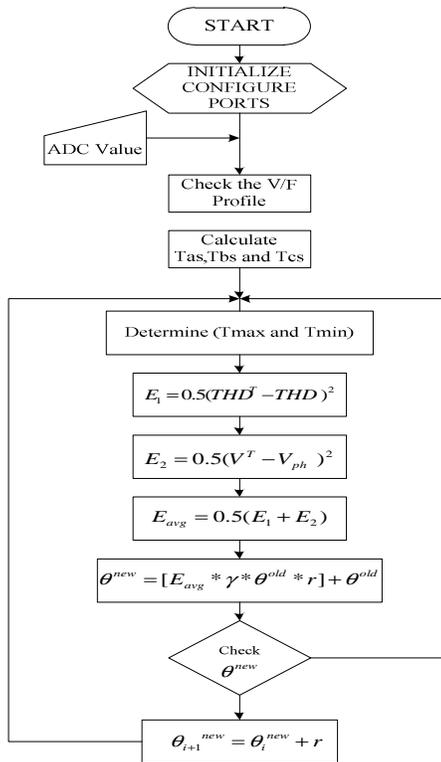


Figure 7: Block Diagram Of SWARM Algorithm Flow Chart

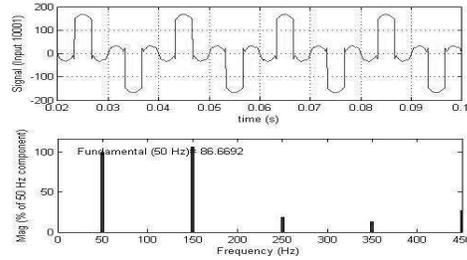


Figure 8: FFT Window Of Third Order Harmonic Injection Waveform In MATLAB

Figure 9 illustrates 48% and 5th order has 100% THD.

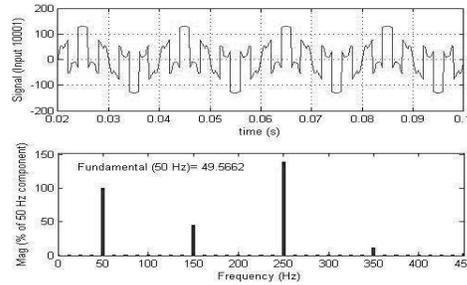


Figure 9: FFT Window Of Fifth Order Harmonic Injection Waveform In MATLAB

Figure 10 shows switching angle obtained from MATLAB for given four notches.

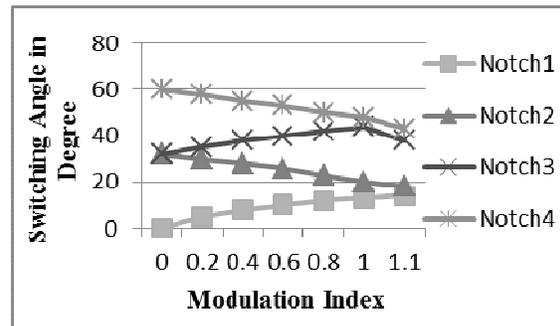


Figure 10: Comparison Of Optimum Switching Angle And Modulation Index

6. EXPERIMENTAL RESULT

Table 3 shows the experimental parameters. The hardware for 5-level MOSFET H bridge cascaded multilevel inverter topology is shown in Figure.11 with dsPIC working environment has been developed.

Table3: Experimental Parameters

HARDWARE SPECIFICATIONS	
Motor Rating	2.2 Kw
Current	5 A
Voltage	415 V
Speed	1500 Rpm
Controller	dsPIC30F4011
MOSFET	IRF548N
Switching Frequency	20KHz
Inverter Topology	Cascaded H-Bridge
Clock Speed	20MHz

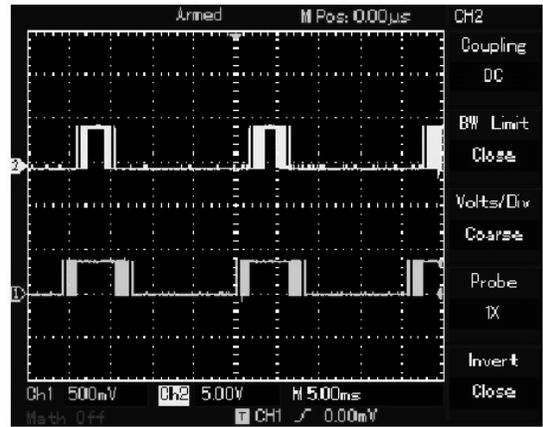


Figure13: Gating Pulse Of Y Phase Positive And Negative Half Cycle

Figure 14 shows the switching selection logic which desires the conduction time period of MOSFET of VSI and H bridge inverter. Figure 15 shows the booster driver IR2110.

The proposed inverter operates at the switching frequency of 20 kHz.

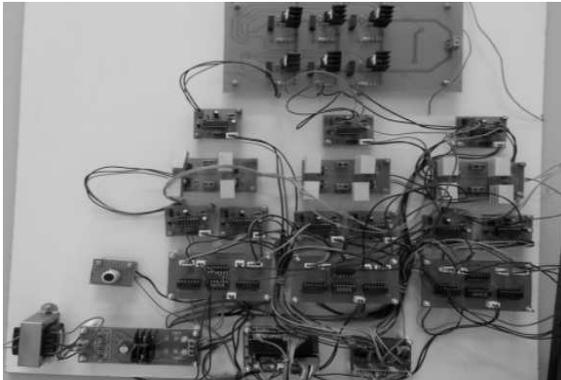


Figure 11: Laboratory Model Of Proposed Hardware

The output waveforms depicted in Figure 12 and 13 show the notches that are introduced in switching pulses.

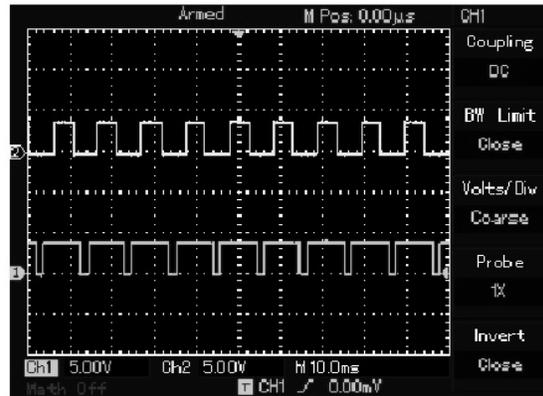


Figure14: Output Of Switching State Selective Logic

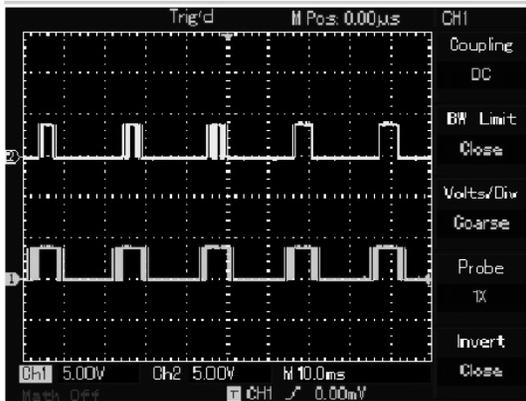


Figure 12: Gating Pulse Of R Phase Positive And Negative Half Cycle

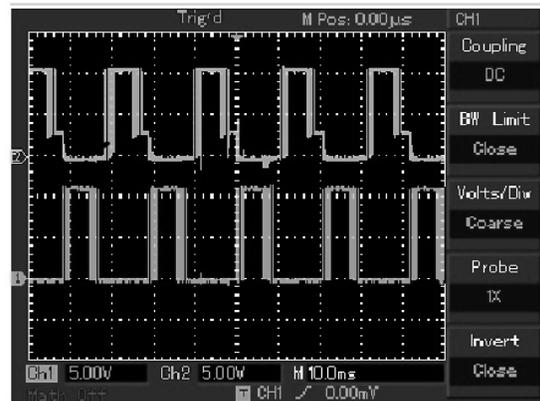


Figure 15: Outputs From Booster Strip

Comparison graph illustrated in Figure 15 shows the distortion factor and harmonics order for the proposed algorithm with standard grid code.

The graphical data displays the distortion factor. The THD value of SSPWM value is small as compared to SMHPWM and SHPWM algorithm. The simulation is carried for 3rd, 5th, 7th and 11th harmonic order and hardware is tested in 3 phase 3.3Kw induction motor. The Table 4 depicted the comparison of hardware and simulation results.

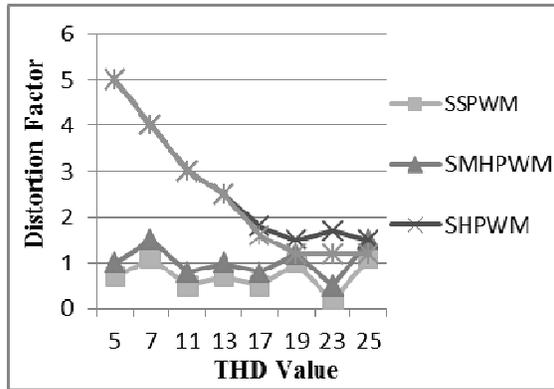


Figure 16: Comparisons Of Different Switching Schemes

Table 4: Comparisons of simulation and hardware.

TOTAL HARMONIC DISTORTION IN %			
ORDER	STANDRD IEC 61000- 3-6	MATLAB	PRACTICA L
5	5	4.3	4.4
7	4	5.2	3.7
11	3	3.5	3.1
13	2.5	1.4	1.2

However, there are some deviations due to unstable simulation results caused by untrained dataset. A negative notch introduced in PWM signal for the elimination of 3rd order harmonics

is illustrated in Figure 12 and 13. These PWM signal is boosted using IR2110, MOSFET driver. The output of the proposed five level inverter topology without harmonic elimination is illustrated on Figure 16, with distorted load current waveform. The FFT window is depicted in Figure 15. The load current waveforms are shown in Figure 17 and the five level voltage load voltage waveform after

implementing the proposed SWARM algorithm is depicted in Figure 18.

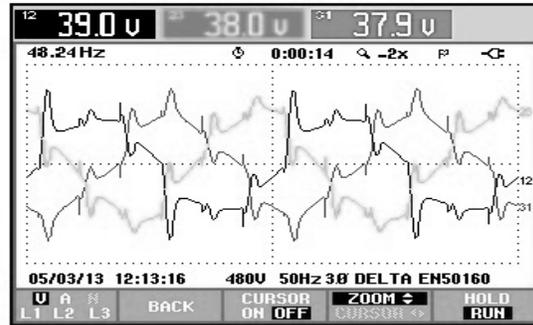


Figure 17: Current Waveform Without Mitigation Technique

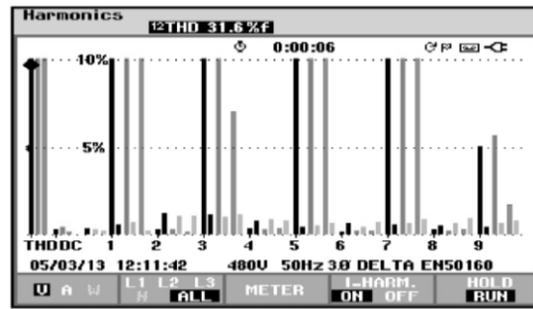


Figure 18: FFT Window Without Harmonic Mitigation

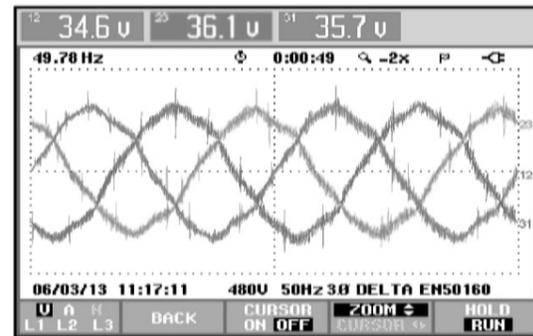


Figure 19: Current Waveform With Mitigation Technique

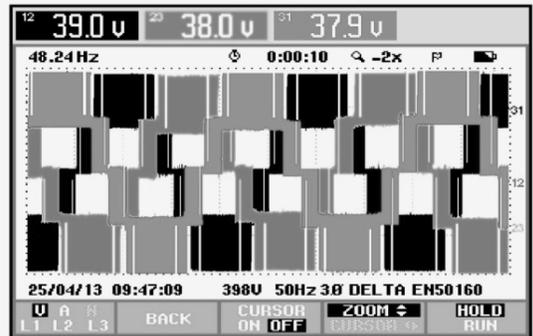


Figure 20: Load Voltage Waveform

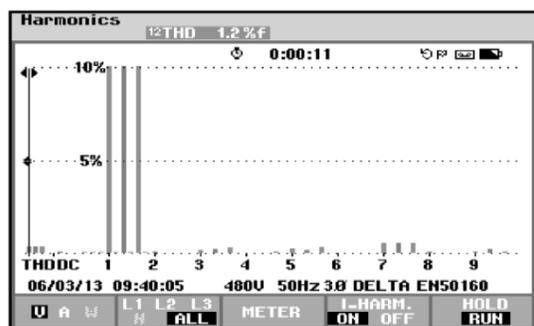


Figure 21: FFT Window of proposed system

Figure 19 illustrates the FFT window with fundamental frequency with 100% of its amplitude. The low order harmonics of 3rd, 5th, 7th and 9th order are totally eliminated.

7. CONCLUSION

In this paper selective harmonic elimination has been achieved using values of sampled phase voltages in dsPIC30F4011 environment for the cascade H bridge multilevel inverter for harmonic order of 3, 5, 7 and 11 and the final THD value is only 1.2% which is very less compared to SMHPWM.

This proposed method uses user selectable harmonic elimination option. Also the switching frequency of inverter is about 20 kHz which results in less EMI and THD within the range of harmonic standards EN 50160, CIGREJWGC4.07 and IEC 61000-3-6 from both individual harmonics and THD point of view. The closed loop system increase dynamic response by employing inner current limit and outer speed limit control. This method does not have any restrictions for higher levels and topologies. The proposed system can be used or distributed electrical system such as electric tractions, solar inverter and wind energy generation system.

REFERENCES:

- [1] Ahamad M. Ibrahim. Fuzzy logics for Embedded Systems Applications. 3rd ed. USA: ELSIVER Science; 2003.
- [2] Mahmoud Gaballah, Mohammed El-Bardini. "Low cost digital signal generation for driving space vector PWM inverter", *Ain Shams Engineering Journal*, Vol.4, No.7, 2013, pp. 1-12.
- [3] Ayong Hiendro, "Multiple Switching Patterns for SHEPWM Inverters Using Differential Evolution Algorithms", *International Journal of Power Electronics & Drive System*, Vol.1 No. 6, 2011, pp. 94-104.
- [4] Ray Rup Narayan, Chatterjee Debashis, Goswami Swapan Kumar. "An application of PSO technique for harmonic elimination in a PWM inverter", *Application Soft Computing*, Vol 4, No. 5, 2009, pp. 1315-1320.
- [5] Zhong Du, Burak Ozpineci, Leon M. Tolbert, John N. Chiasson. "DC-AC Cascaded H-Bridge Multilevel Boost Inverter with No Inductors for Electric/Hybrid Electric Vehicle Applications", *IEEE Transaction Industrial Electronics*, Vol.7, No.45, 2009, pp.963-970.
- [6] Zhong Du, Leon M. Tolbert, John N. Chiasson. "A Cascade Multilevel Inverter Using a Single DC Source", *IEEE Proceedings on Industrial Application*, Vol.4, No.32, 2006, pp. 963-970.
- [7] K. Sivakumar, Anandarup Das, Rijil Ramchand, Chintan Patel, K. Gopakumar, "A Hybrid Multilevel Inverter Topology for an Open-End Winding Induction-Motor Drive Using Two-Level Inverters in Series With a Capacitor-Fed H-Bridge Cell", *IEEE Transaction Industrial Electronics*, Vol.10, No. 57, 2010, pp. 87-95.
- [8] R.S. Kanchan, M.R. Baiju, K.K. Mohapatra, P.P. Ouseph and K. Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltage's", *IEEE Transaction Electrical Power Applications*, Vol.5, No. 152, 2005, pp. 297-309.
- [9] F. Valdez, P. Melin, O. Castillo, "An improved evolutionary method with fuzzy logic for combining Particle Swarm optimization and Genetic Algorithms". *Applied Soft Computing*, Vol.11, No.11, 2011, pp.2625-2632.
- [10] Cristian Musardo, Giorgio Rizzoni, Fellow, and Benedetto Staccia, A-ECMS: An Adaptive Algorithm for Hybrid Electric Vehicle Energy Management, *European Journal of Control*, Vol.11 (Issue 11): 509-524, January 2005.
- [11] Parekh Rakesh, "V/F control of 3-phase induction motor using space vector modulation", *Microchip Technology Inc*, 2005.
- [12] J. Sun, S. Beineke, and H. Grotstollen, "DSP-based real-time harmonic elimination of PWM inverters", *Power Electronics Specialists Conferences*; Vol.5, No. 12, 1994, pp- 679-685.
- [13] Marzoughi A, Imaneini H, "An optimal selective harmonic mitigation for cascaded H-bridge converters", *Environmental and Electrical Engineering Conferences*; Vol.11, No. 119, 2012, pp. 752-757.



- [14] Alinaghi Marzoughi, Hossein Imaneni, “An optimal selective harmonic mitigation technique for high power converters”, *International Journal of Electrical Power & Energy Systems* Vol. 1, No. 49, 2013, pp. 34–39.
- [15] F. Swift and A. Kamberis, “A new Walsh domain technique of harmonic elimination and voltage control in pulse width modulated inverters”, *IEEE Transaction Power Electronics*, Vol. 7, No. 8, 1993, pp. 170-185.
- [16] F. Valdez, P. Melin, O. Castillo, “An improved evolutionary method with fuzzy logic for combining Particle Swarm optimization and Genetic Algorithms”. *Applied Soft Computing*, Vol. 3, No. 11, 2011, pp. 2625-2632.