Journal of Theoretical and Applied Information Technology
20th December 2013. Vol. 58 No.2

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

FULL ON-CHIP CMOS LOW DROPOUT VOLTAGE REGULATOR WITH -41 dB AT 1 MHZ FOR WIRELESS APPLICATIONS

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ABSTRACT

A high PSRR full on-chip and area efficient low dropout voltage regulator (LDO), exploiting the nested miller compensation technique with active capacitor (NMCAC) to eliminate the external capacitor and improve the high performance. A novel technique is used to boost the important characteristic for wireless applications regulators PSRR. The idea is applied to stabilize the Low dropout regulator. The proposed regulator LDO works with a supply voltage as low as 1.8 V and provides a load current of 50 mA with a dropout voltage of 200 mV, the PSR of LDO is -60 dB at a frequency of 60 KHz and -41dB at a frequency of 1 MHz. It is designed in 0.18 µm CMOS technology and the active area on chip measures 0.043 mm^2.

Keyword: *Low Dropout Regulator (LDO); MOSCAP; NMCAC; Active Feedback; High PSR; System On Chip.*

1. INTRODUCTION

In the last generation of power management system a switching power converter (SWPC) is followed by a Low Drop-out (LDO) voltage regulator to increasing battery life of portables applications, suppress the ripples at output of the SWPC and provide a clean voltage supply at its output. Due to the increase in operating frequencies, high switching frequencies in SWPC are required for fast transient response in addition to allowing for the use of smaller passive components to reduce area and coast. In the other words, the LDO should have a high Power supply rejection (PSR) up to these few MHz frequencies [1], [8].

Different techniques have been reported to implement LDOs with high PSR at low frequencies. Cascading two pass transistors using drain extended FET transistors [2], and using a voltage subtractor stage with a diode-connected transistor driving the gate of the pass transistor [3] were among the techniques used. Reference [4] was the first to achieve high PSR up to 10MHz frequency through using a cascade of NMOS and PMOS transistors together with a charge pump to bias the NMOS transistor. However, the circuit maximum load current was only 5mA with large drop-out voltage (0.6V). That is in addition to the added complexity and power consumption of the charge pump. A feed-forward ripple cancellation technique was used in [5], [1] to achieve better PSR up to 10MHz. This technique has a limitation on load current to be only 25mA for good PSR due to having a fixed gain of the feed-forward ripple cancellation path that relies on the ratio of resistors. This ratio can be designed to provide the required cancellation over a narrow load current range.

To avoid the problem of integrated a large capacitor for Miller compensation and improve a high PSR and fast transient response, one of the possible solutions is the use of MOS capacitor [6], [9]. Because the MOS capacitors called MOSCAPs have larger capacitance per unit area [6], [7]. However, the main problem in largely used MOSCAPs in analog applications is due to linearity issues. This is because of different regions of MOSFET experiences when its gate-bulk voltage varies. For small bias voltages, the transistor is working in depletion region, thereby leaving the capacitor a function of the gate-bulk voltage. This degrades overall performance and mostly adds complexity to the design of analog circuits [10], [11]. In the saturation region of CMOS transistor, the variation capacitance of the MOSCAP with a VBS=0 is neglected [6], [7].

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

In this paper, we present a modified NMC with a NMOS source follower stage at PMOS transistor gate to charge rapidly the gate power PMOS capacitance and improve high PSRR. The CMOS capacitor (MOSCAP) is used as a miller capacitor instead of MIMs capacitors or MOM capacitors to reduce the area occupied by the Miller capacitance without influencing stability and realize the full on-chip capacitor LDO with a high performance.

2. PROPOSED LDO

The proposed LDO, shown in Figure 1(a), is composed of two gain stages, a power PMOS transistor and the feedback resistor network. The first stage is the error amplifier (EA). The second is a NMOS gain stage. Cm1, Cm2 are the on-chip active MOS capacitances. Rf1 and Rf2 construct the active feedback resistive network. RL and CL model the equivalent load resistance and load capacitance at the output of LDO. CL is the interconnection lines parasitic capacitor, and typically up to 100 pF. The n-well resistor has a high value for its voltage coefficient, which affect the accuracy in the ICs [6]. Weak inversion region MOS transistors are used as a feedback network resistor instead of conventional n-well resistors in order to lowers quiescent current and save silicon area.

3. ERROR AMPLIFIER

The design of error amplifier (EA) is more complex, when a high performance is required to guarantee the stability and transient response, a specific topology is necessary. To move the dominant pole at the output of E.A to low frequencies, low output impedance is designed. To charge rapidly the capacitance seen at the gate of pass transistor (may be as large as 50 pF), EA must provide a sufficient output current [2], [12]. On the contrary, the EA itself should provide very low power dissipation, and its bias currents must be kept as low as possible. In this paper, the proposed EA is the folded cascode amplifier which offers better performances such as high gain, enough load current to drive the power transistor PMOS and improved PSRR characteristic of LDO.

3.1 MOSCAP Compensation Network

In the full on-chip LDO, the load capacitor modelled at drain of pass transistor is determined by the interconnection lines and typically up to 100 pF. This capacitive value is too small to set a dominant pole at the output node of on-chip LDO [13], [7]. Therefore, the compensation must be achieved through the miller effect. In [14], the Miller compensation technique is applied to compensate a two-stage Op Amp. As a result, the dominant pole is placed at the output of first stage and moved to low frequencies. The second pole is moved away from the origin of the complex frequency plane. Due to the feedforward path through the Miller capacitor, an undesirable zero occurs on the positive real axis of the complex frequency plane. These approaches require a large compensation capacitor and a high gain of second stage to ensure stability. Moreover, it is difficult to integrate a large capacitor on-chip LDO.

In the recent design of the system on-chip applications, a capacitor MOSCAP was used instead of the MIM or MOM capacitor in Miller compensation. The problem with exploiting MOSCAPs in analog applications is due to the linearity issues [6].This is because of different regions a MOSFET experiences when its gate-bulk voltage varies.

In the proposed structure, the gate-bulk voltage of MOSCAP is controlled and determined by the designer as demonstrated in eq. (2). The MOSCAP is working in the accumulation region, where the capacitance is not dependent on the gate bulk voltage.

The DC potential at the gate and bulk of MOSCAP C_{m1} are given by

$$V_{gCm1} = \frac{1}{\lambda_N}\left(\frac{B_2}{B_1}\frac{\beta_{14}}{\beta_4} - 1\right)$$
$$V_{bCm1} = V_{out}$$
$$V_{gbCm1} = \frac{1}{\lambda_N}\left(\frac{B_2}{B_1}\frac{\beta_{14}}{\beta_4} - 1\right) - V_{out} \quad (1)$$

For keeping the value of capacitor C_{m2} independent to its gate- bulk voltage, the following condition must be respected by the designer

$$\lambda_{NCm1}(V_{out} + V_{TN}) \geq \left(2 * \frac{B_2}{B_1}\frac{\beta_{14}}{\beta_4} - 1\right) \quad (2)$$

Same as in eq. (2), the gate-bulk voltage of compensation capacitor C_{m2} is controlled by the following condition

$$\lambda_{NCm2}(V_o + V_{TN}) \geq \left(2 * \frac{B_3}{B_2}\frac{\beta_{14}}{\beta_{11}} - 1\right) \quad (3)$$

Where B1, B2 and B3 are the current gain of current mirrors M4-M14, M16-M17 and M16-M18 respectively and β4, β11, β12 and β14 are the transconductance parameters of transistors M4, M11, M12 an M14 respectively. Ibias is the start-up current of the circuit. From eq. (2), the gate-bulk voltage is independent of the load in the regulation mode. In the worst case, when Iload increases instantaneously, from eq. (2), the bulk voltage of pass element drops in time or the load capacitor C_L and compensation capacitor MOSCAP dischargers to supply the extra current demanded at the output.

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20th December 2013. Vol. 58 No.2

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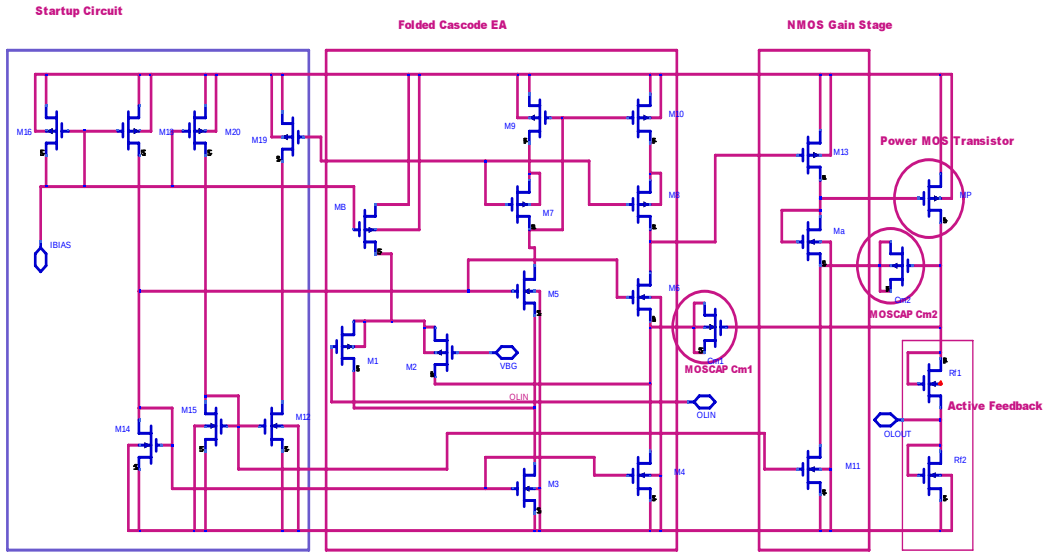
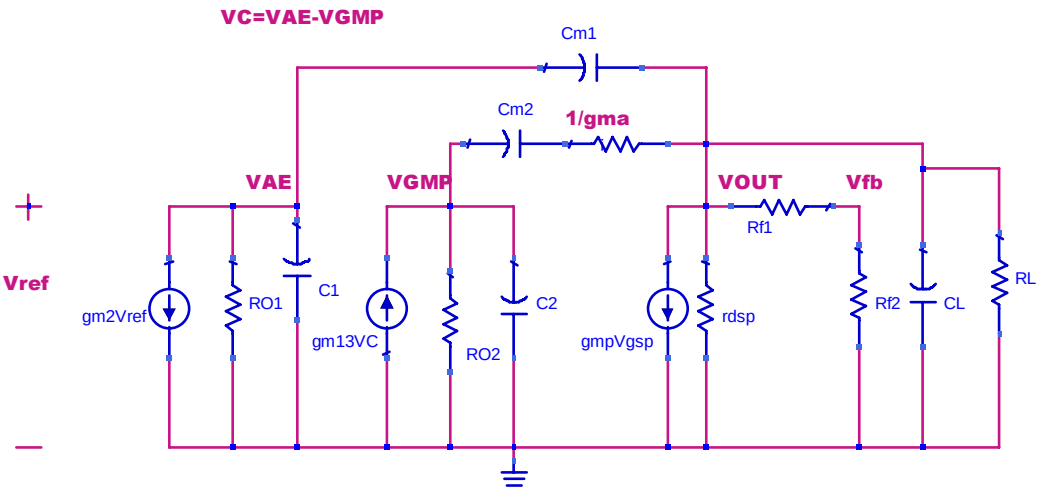
As a result, the current gain of current mirror M4-M14 is decreased and the gate voltage of MOSCAP drops verifying the condition of the gate-bulk voltage V_{gbcm1} >0.74V as given in eq. (2).

3.2 Stability Analysis

The compensation technique used in this structure places the dominant pole at low frequencies and moves the parasitic poles to high frequencies. The LHP zero is created by the compensation capacitance and improves the phase margin in time when the RHP zero is placed at high frequencies. The small signal of the proposed LDO is in Figure 1(b). g_{mp}, g_{m2}, g_{ma} and g_{m13}, represent the transconductance of transistors MP, M2 of error amplifier, the NMOS diode and M13 of source follower respectively. g_{dsp}, g_{ds2}, and g_{ds13} represent the conductance of transistors MP, M2 of error amplifier and M13 of source follower respectively. C1, C2, R_{O1} and R_{O2} are the output capacitors and resistors of EA and source follower stage.



a)



(b)

Figure 1: Proposed LDO a) schematic of CMOS LDO b) small signal of proposed LDO

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Assuming that g_{ma}<<g_{mp}, and C_{m1}, Cm2 and C_L>>C_I, C_{EA}, the small signal loop gain is given by.

$$T(s) = T(0) * \frac{(1+b_1S+b_2S^2)}{\left(1+\left(S/p_{-3dB}\right)\right)(1+a_1S+a_2S^2)} \quad (4)$$

With

$$T(0) = g_{m2}g_{m13}g_{mp}R_{O1}R_{O2}R_{out}\left(R_{F1}/R_{F1}+R_{F2}\right) \quad (5)$$

Where the dominant pole is at

$$p_{-3db} = \frac{1}{g_{m2}g_{mp}R_{O1}R_{O2}R_{out}C_{m1}} \quad (6)$$

And

$$b_1 = \frac{C_{m2}}{g_{ma}},\ b_2 = -\frac{C_{m1}C_{m2}}{g_{m2}g_{mp}}, a_1 = R_LC_L + C_{m2}\left(\frac{1}{g_{m2}}+\frac{1}{g_{ma}}\right), a_2 = \frac{C_{m2}C_L}{g_{m2}g_{mp}} \quad (7)$$

Assuming that g_{ma} is small and the non-dominant poles are widely spaced, then the roots of the second-order polynomial in the denominator in eq. (4) are rewritten as

$$P_{nd1} \approx -\frac{1}{R_LC_L + C_{m2}\left(\frac{1}{g_{m2}}+\frac{1}{g_{ma}}\right)},$$
$$P_{nd2} \approx \frac{g_{mp}}{C_{m2}} \quad (8)$$

In the NMCAC LDO, the dominant pole is unchanged, but the non-dominant poles are pushed to high frequencies. From the polynomial in the numerator of eq. (4) and assuming that the approximation in eq. (7) the two zero are expressed as

$$Z_{LHP} \approx -\frac{g_{ma}}{C_{m2}},$$
$$Z_{RHP} = \frac{g_{m2}g_{mp}}{g_{ma}C_{m1}} \approx \frac{g_{mp}}{C_{m1}} \quad (9)$$

Increasing the load current, the RHP zero and non-dominant pole formed at the output of LDO move to higher frequencies, while the LHP zero is independent of the load current and moved to high frequencies by increasing the current in the NMOS gate stage. From Eq. (7, 9), the damping factor is derived as

$$\varsigma = \frac{1}{2}\left(R_LC_L + C_{m2}\left(\frac{1}{g_{m2}}+\frac{1}{g_{ma}}\right)\right)\sqrt{\frac{g_{m2}g_{mp}}{C_{m2}C_L}} \quad (10)$$

In the NMCACR LDO, a small g_{ma} enhances the damping factor without influencing the dc loop gain and without increasing C_{m2}. the damping factor is controlled by g_{ma} instead of gm2. From eq. (9) with $(W/L)_a$=5, the Z_{LHP} is placed at 11MHz as presented in fig. 4.

3.3 Power Supply Rejection

The main concept of achieving a better PSR for an LDO relies on providing a path for the ripples appearing at the input of the LDO to be replicated at the gate of the pass transistor. The most literature focuses in its analytic of the PSRR on parameters and devices transmit and control the ripple from the supply to the output of the system neglecting the effect of the parasitic capacitances at the output of error amplifier and its high output stage gain. In this work, a diode M_a is connected at gate of the pass transistor to control damping factor and enhancing PSR.

The small signal model of PSRR is shown in figure 2. A small signal input voltage v_{dd} will induce an output voltage v_{out}. The PSRR can be seen to be

$$PSRR = \frac{v_{out}}{v_{dd}} = \frac{(g_{mp}-g_{dsp})(A_p+SC_p)-(g_{dsp}+SC_c)(g_{ds13}+SC_{gsp})}{a_0(1+a_1S^1+a_2S^2+a_3S^3)} \quad (11)$$

Where

$$A_p = g_{m13} + g_{ds13} + g_{ma}(1-A_{c2}),$$
$$C_p = C_{gs13} + C_{gsp} + C_{gdp},$$
$$C_c = A_{c2}C_{m2} + C_{gdp},$$
$$A_{c2} = \frac{r_{ds11}g_{ma}}{1+r_{ds11}g_{ma}} \quad (12)$$

Assuming that A_{EA}>>R_L, gm_{13}, the dc gain of PSRR can be expressed as

$$PSRR|_{DC} \approx \frac{(g_{mp}-g_{dsp})A_p-g_{dsp}g_{ds13}}{g_{mp}A_{EA}g_{m13}} (13)$$

As can be seen from eq. (13), the dc gain of PSRR is controlled by the NMOS gain stage performance. At low frequency, in low load condition, g_{mp} decreases, and also the gain of EA decreases.

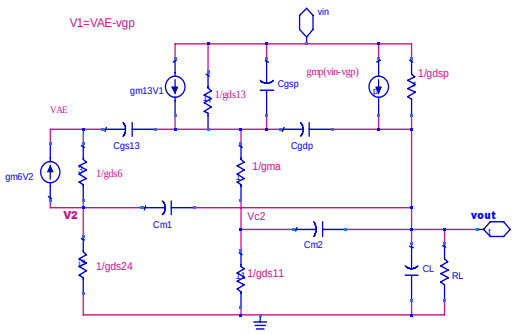

Figure 2: Small signal model of enhanced PSRR.

From eq. (13), g_{mp} in numerator and denominator hence $PSRR|_{DC}$ is not heavily affected by the transconductance variation of power

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transistor and is controlled by the gain of M13 and Ma. At full load condition, an increase in g_{mp} and gain of EA, enhance the $PSRR|_{DC}$.

In case of having the gate of MP transistor connected to the output of the EA without the NMOS gain stage as in [21]; $PSRR|_{DC}$ can be expressed as:

$$PSRR|_{DC} \approx \frac{g_{mp}}{R_L} \quad (14)$$

As the load current decreases, also the transconductance of MP decreases, the gain of PSRR and the performance of LDO is affected.

From eq. (11), the PSRR drops at two breakpoints Z_1 and Z_2. Assuming that $Z_1 << Z_2$, $g_{ds13} << g_{mp}$, Cp is about 24 pF and Cc is about 15 pF, at moderate frequency, the degradation gain of PSRR is starting at breakpoint zero (Z_1) and given by:

$$Z_1 = -\frac{A_p}{C_p} \quad (14)$$

And

$$Z_2 = \frac{g_{mp}C_p - g_{ds13}C_c - g_{dsp}C_{gsp}}{C_c C_{gsp}} \quad (15)$$

From eq. (14), the first break point Z_1 at moderate frequency is not influenced by different load conditions and can be pushed to high frequency by increasing the transconductance of transistor M_{13} M_a, or decreasing the gain of divider NMOS Ma-M11 at gate Power PMOS transistor. As can be seen from eq. (15), the negative time constant formed by C_{m2} and C_{gsp} is subtracted from the time of the second zero. Consequently, the second zero moves to higher frequencies resulting in higher roll-off PSRR.

4. SIMULATION RESULTS

The proposed regulator LDO has been realized in 0.18 µm CMOS technology. The layout of the IC LDO is shown in Fig. 9 with an active chip area of 241 µm×187 µm, which is dominated by Power MOS transistor. The on-chip MOS capacitors occupy a small area on chip. The simulation of the proposed LDO was performed with Spectre. The loop-gain simulation has been performed with a total on-chip compensation capacitor C_{total}=24 pF, and the output capacitor C_L (up to 100 pF). The proposed LDO is stable with a good phase margin of approximately 82° at full load as shown in Fig. 4. At low load, the loop's gain drops to the low value of 39 dB and a phase margin is of 67°.

Fig. 5, Shows the simulation of PSRR at 50 mA load current. The impedance inserted at the gate of power MOS transistor by the NMOS gain stage and transistor M_a enhances the PSRR, and its value is -61 dB in the range of [0-60KHz]. As depicted in Fig. 5, when a simple NMOS gain stage is inserted at gate of power transistor the PSRR at 1 MHz is about -36 dB and when the novel technique is applied the PSRR at 1MHz is -41.7 dB.

The line regulation simulation of the proposed LDO is shown in Fig. 6. Fig 6(a) shows the AC line regulation for supply voltage change from 2 to 2.5 V. The AC line regulation is about 4 mV with a settling time of 2 µs. Fig 6(b) shows the transient response simulation of the proposed LDO with load current switching between 100 µA and 50 mA. The variation of output is about 110 mV with a settling time of 3 µs for 0.005% accuracy.

Another important characteristic of LDO is the DC load regulation as shown in Fig. 8(b), when the load current goes from 0 mA to 50 mA, the variation of the output voltage is 0.6mV/mA. In the worst case (Load current increases from 0 to 50 mA), the output voltage variation is about 67 mV.

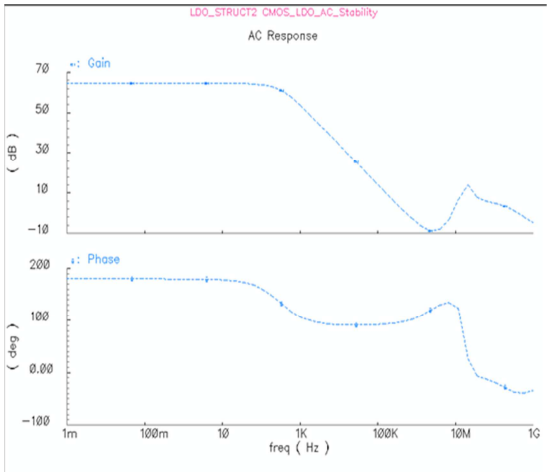

Figure 3: Simulation Result Of Proposed LDO Frequency Response.

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ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

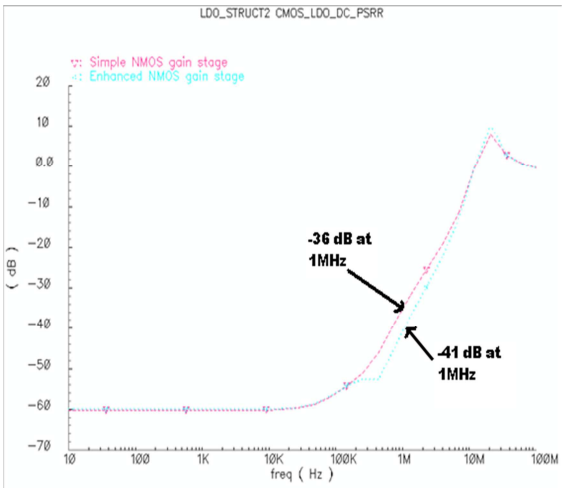


Figure 4: PSRR simulation performance of the proposed full on-chip LDO.

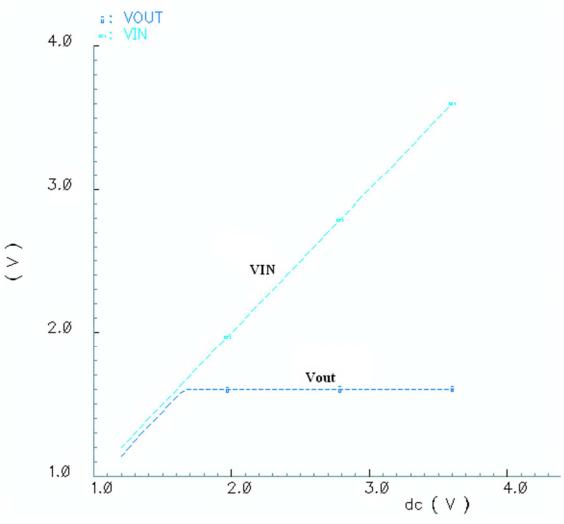
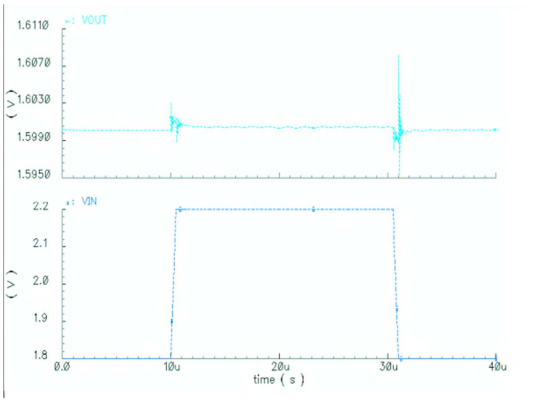
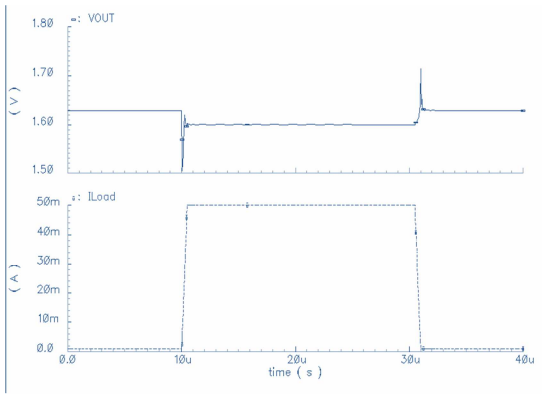


Figure 6: DC line regulation simulation.



(a)



(b)

Figure 5: Transient response of proposed LDO a) AC line regulation b) AC load regulation.

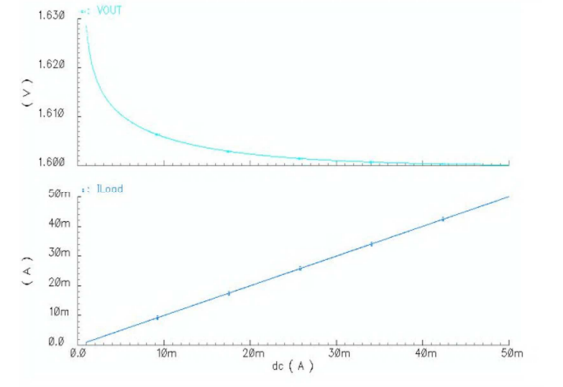


Figure 7: DC line regulation simulation.

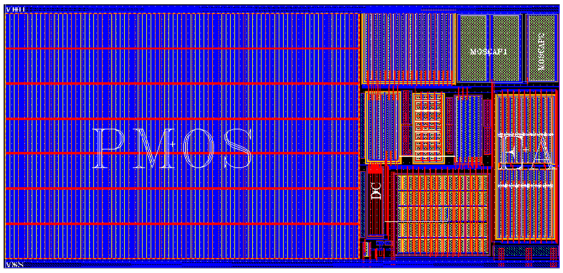


Figure 8: Layout of proposed LDO

ISSN: 1992-8645 www.jatit.org E-ISSN: 1817-3195

Table 1.Performances and comparison with other works

Parameter	[5]	[16]	This work
CMOS Technology (µm)	0.13	0.18	0.18
VIN (V)	>1.15	1.2-1.5	1.8-3.6
VOUT (V)	1	1	1.6
Drop-out (mV)	>0.15	300	200
Compensation (pF) Cap	N/A	41	24
ILmax (mA)	25 mA	50	50
Line regulation (mV/mA)	N/A	0.024%	0.26
Load regulation (mV/mA)	0.048	0.7 mV/4 mA	0.6
Settling time (µs)	N/A	1.6	2 (ACLN[1]) 3 (ACLD[2])
PSSR(dB)	-60dB@100KHz -67 dB@1MHz	-70 @ 1 KHz -37 @ 1 MHz	-61 @100 Hz -41 @1MHz
Active chip area (mm^2)	0.0495	0.1044	0.045

1. AC line regulation
2 AC load regulation

5. CONCLUSION

In this paper, a full on chip CMOS LDO using a modified NMC technique has been presented. The regulator circuit design features an active compensation technique, which guarantees the stability through the full load current rage with high PSRR of -60 dB up to 100 KHz and -41 dB at 1MHz. The high performance is independent of the off-chip capacitor. The detailed analysis of the proposed structure is revealed to justify the performance of the technique utilized. The simulations prove the results theory.

The proposed LDO is capable of providing 50 mA with a drop-out voltage of 200 mV at VDD of 1.8 V. The stability is achieved by using the MOSCAP compensation capacitor in the accumulation region. The active area is reduced by 40 % compared to the state-of the-art designs using technologies with the same feature size. The proposed regulator is mainly used as a regulating power source for wireless applications, RFID and charge pumps.

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